Compact Model for Short Channel Effects in Source/Drain Engineered Nanoscale Double Gate (DG) SOI MOSFET

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Objectives/Simulations

- Study the impact of Source/Drain Extension (SDE) region design on Short channel effects (SCEs):
- Analytical model for Threshold voltage and Subthreshold slope

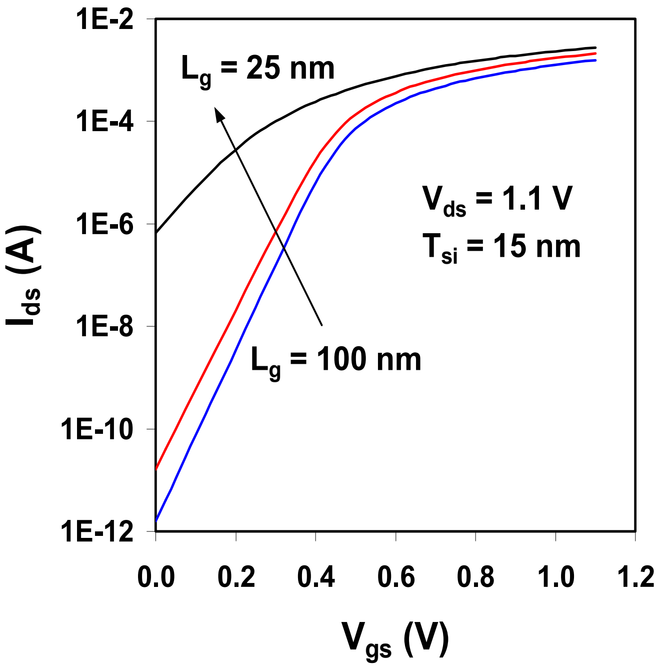
Simulations:

- Symmetric self-aligned DG MOSFETs.
- HP 65 nm node: L_g = 25 nm, T_{ox} = 1.3 nm (SiO_2), V_{ds} = 1.1V.
- Midgap gate workfunction: φ_m = 4.72 eV.
- Spacer widths (s): (0.25)L_g, (0.50)L_g, (0.75)L_g and (1.00)L_g.
- S/D doping gradient at edge of gate (d): 1 – 6 nm/decade.
- 2D simulations: ATLAS
- Default models

Short Channel Effects

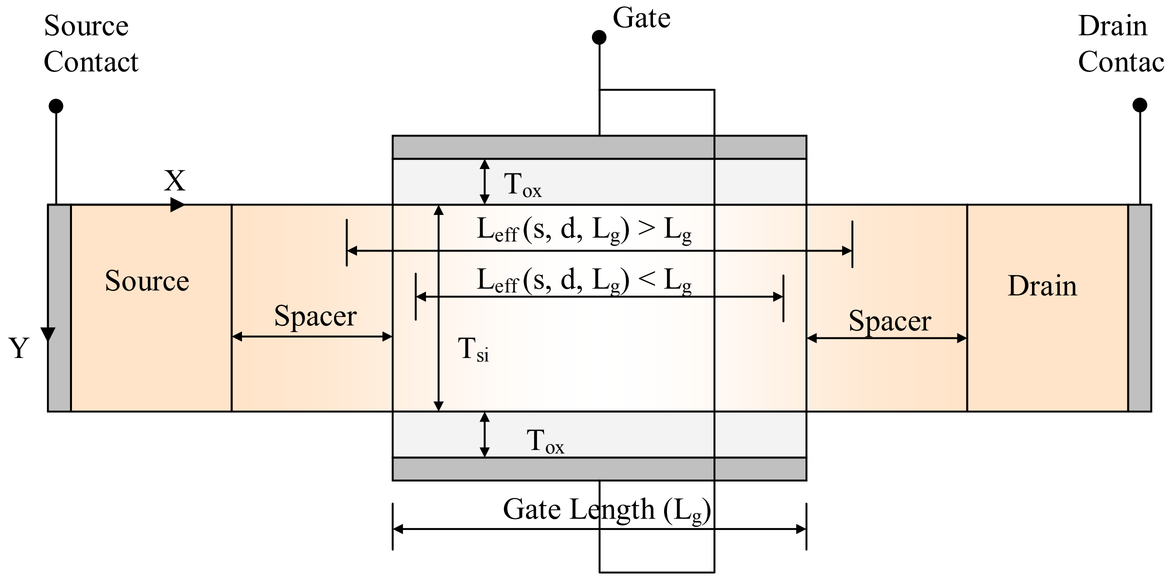
- Reduction in L_g (~ 25 nm) results in an increase of SCEs causing V_{th} and S-slope degradation.

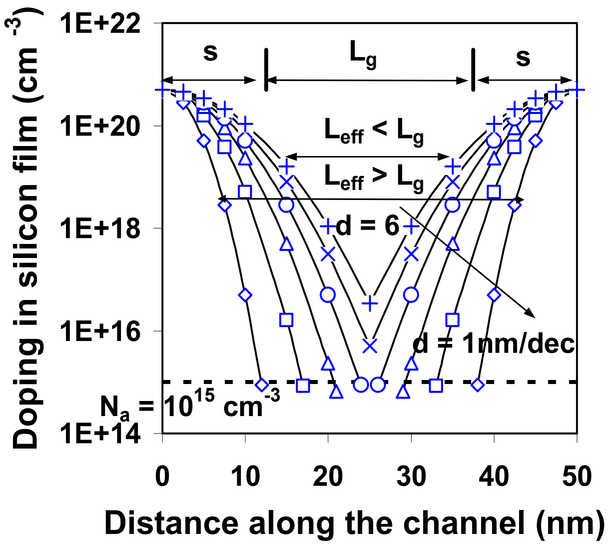
- Possible solutions:
- Reduction in T_{si} and T_{ox}
  - T_{si}: Fabrication challenge < 10nm
  - T_{ox}: Already around 1 nm (High-κ materials)
  - Doping: Degradation in mobility



- Option:
- Engineering Source/Drain Extension (SDE) regions in sub 25 nm devices.

Source/Drain Extension Region Design





- SDE region engineering through the variation of spacer s along with lateral source/drain doping gradient (d) results in the modulation of L_{eff}.
- Larger values of spacer (s) along with smaller values of gradient (d) results in a longer L_{eff}.
- Smaller values of spacer (s) along with larger values of gradient (d) results in a shorter L_{eff}.

Analytical Model

Poisson’s equation for SDE region design

$$\frac{\partial^2\psi(x,y)}{\partial x^2}+\frac{\partial^2\psi(x,y)}{\partial y^2}=\frac{q}{\varepsilon_{si}}\left(N_a \boxed{-N_{SD}e^{\frac{-x^2}{\sigma^2}}-N_{SD}e^{\frac{-(L_g+2s-x)^2}{\sigma^2}}}\right)$$

Solution is mathematically complex

$$\Big\Downarrow$$

Approximation

$$\frac{\partial^2\psi(x,y)}{\partial x^2}+\frac{\partial^2\psi(x,y)}{\partial y^2}=\frac{q}{\varepsilon_{si}}(N_a)$$

SUCH THAT

$$L_g \Longrightarrow \boxed{L_{eff}}$$

The effect of SDE regions can be considered in the effective channel length.

Analytical Model

$$\frac{\partial^2 \psi(x,y)}{\partial x^2} + \frac{\partial^2 \psi(x,y)}{\partial y^2} = \frac{q}{\varepsilon_{si}}(N_a)$$

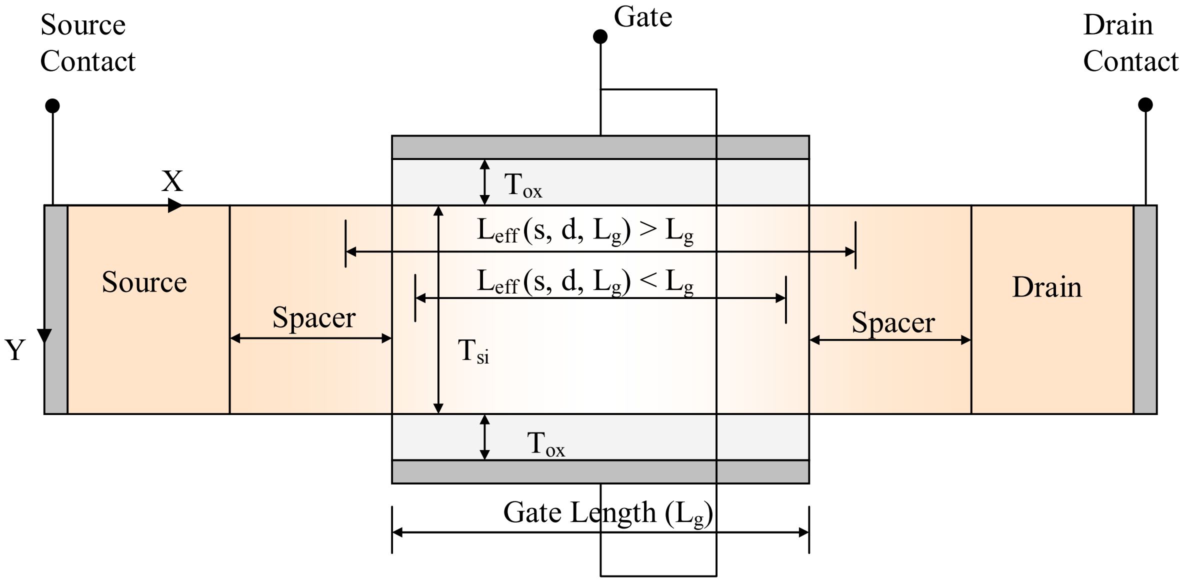
Poisson’s equation is solved using the superposition principle

$$\psi(x,y) = U(y) + V(x,y)$$

- U(y) is the long channel solution to the 1D Poisson’s equation
- V(x,y) is the short channel solution to the 2D Laplace equation

$$\frac{\partial^2 U(y)}{\partial y^2} = \frac{q}{\varepsilon_{si}}(N_a) \qquad \frac{\partial^2 V(x,y)}{\partial x^2} + \frac{\partial^2 V(x,y)}{\partial y^2} = 0$$

Boundary Conditions



- Field at the top Si/SiO$_2$ interface

$$\left.\frac{\partial\psi(x,y)}{\partial y}\right|_{y=0} = \frac{C_{ox}}{\varepsilon_{si}}\left(\psi(x,y=0) - V'_{gs}\right)$$

- Field at the bottom Si/SiO$_2$ interface

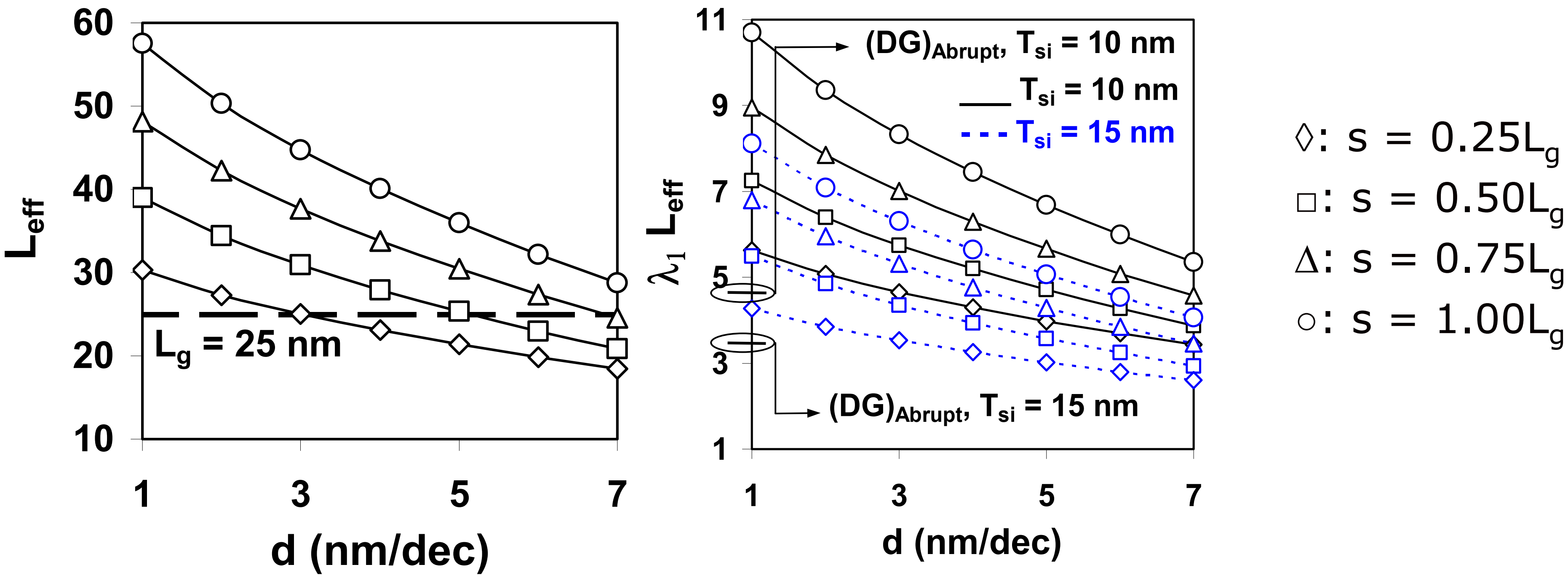
$$\left.\frac{\partial\psi(x,y)}{\partial y}\right|_{y=t_{si}} = \frac{-C_{ox}}{\varepsilon_{si}}\left(\psi(x,y=T_{si}) - V'_{gs}\right)$$

- Potential at the source and drain end

$$\psi(x=0,y) = V_{bi}$$
$$\psi(x=L_{eff},y) = V_{bi} + V_{ds}$$

L_{eff} represents SDE region design

Effective Channel Length Variation



- λ_1 is first eigenvalue in solution of $\varepsilon_{si}/\varepsilon_{ox}\tan(\lambda T_{ox})\tan(\lambda T_{si}/2) = 1$
- Suppressed SCEs ($\lambda_1 L_{eff} > 4$) requires increased L_{eff} with larger s along with smaller d
- Combinations of s and d that yield $\lambda_1 L_{eff} > 4$ can be identified .

Effective Channel Length (L_{eff}) Definition

- L_{eff} is a function of L_g, spacer (s) and doping gradient (d)

$$L_{eff} = \underbrace{L_g}_{\text{Contribution of } L_g \text{ to } L_{eff}} + \underbrace{2\left(s - \sigma\sqrt{\ln\left(N_{SD}/\eta_{SD}\right)}\right)}_{\text{Contribution of SDE regions to } L_{eff}}$$

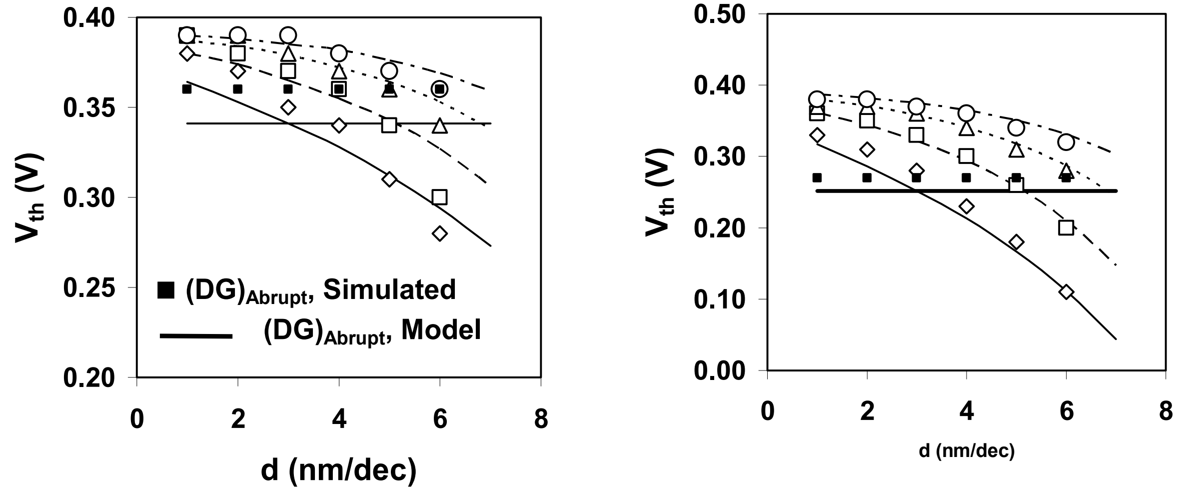
- σ is function of s and d whereas η_{SD} is a function of L_g and s.

$$\sigma = \sqrt{2(s)(d)/2.303} \qquad \eta_{SD} = 2.25\times10^{19}\ln\left(\frac{L_g}{s}\right) + 1.5\times10^{19}$$

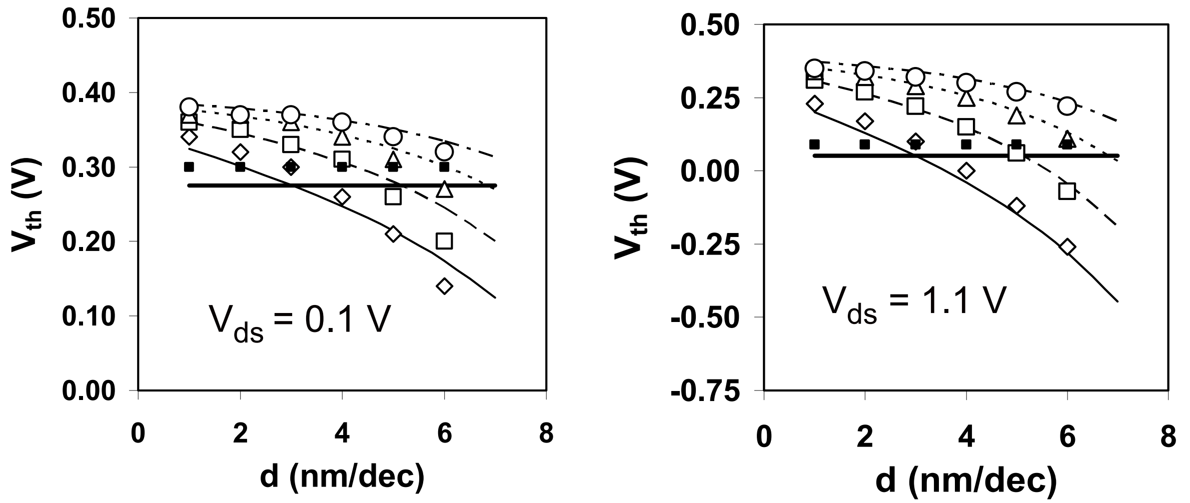
- The parameter σ signifies the roll-off of the source/drain Gaussian profile in the lateral direction. Doping gradient (d = 1 – 6 nm/dec) is defined <u>at the gate edge</u>. for a given spacer such that

$$d = \left| d\log\left(N_{SD}(x)\right)/dx \right|^{-1}$$

V_{th} comparison - Model vs 2D simulation



T_{si} = 10 nm



T_{si} = 15 nm

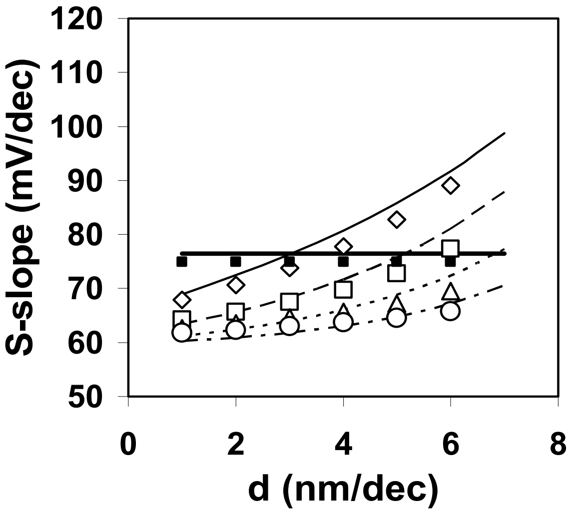
◊: s = $0.25L_g$

□: s = $0.50L_g$

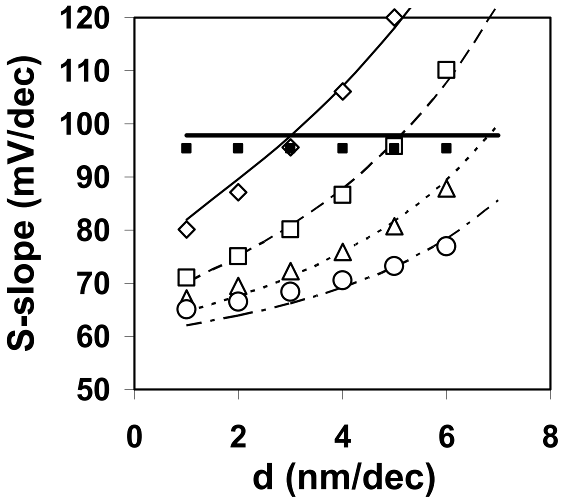
Δ: s = $0.75L_g$

○: s = $1.00L_g$

S-slope @ s, d, T_{si}



T_{si} = 10 nm



T_{si} = 15 nm

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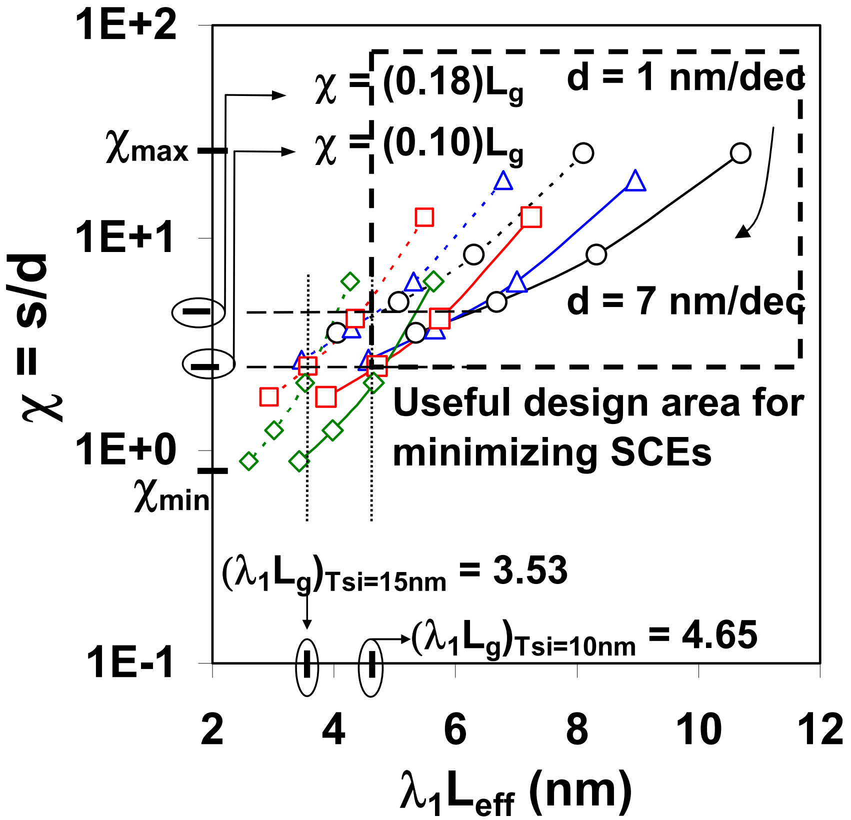
Spacer-to-Gradient Ratio s/d

- Useful design area for minimizing SCEs.

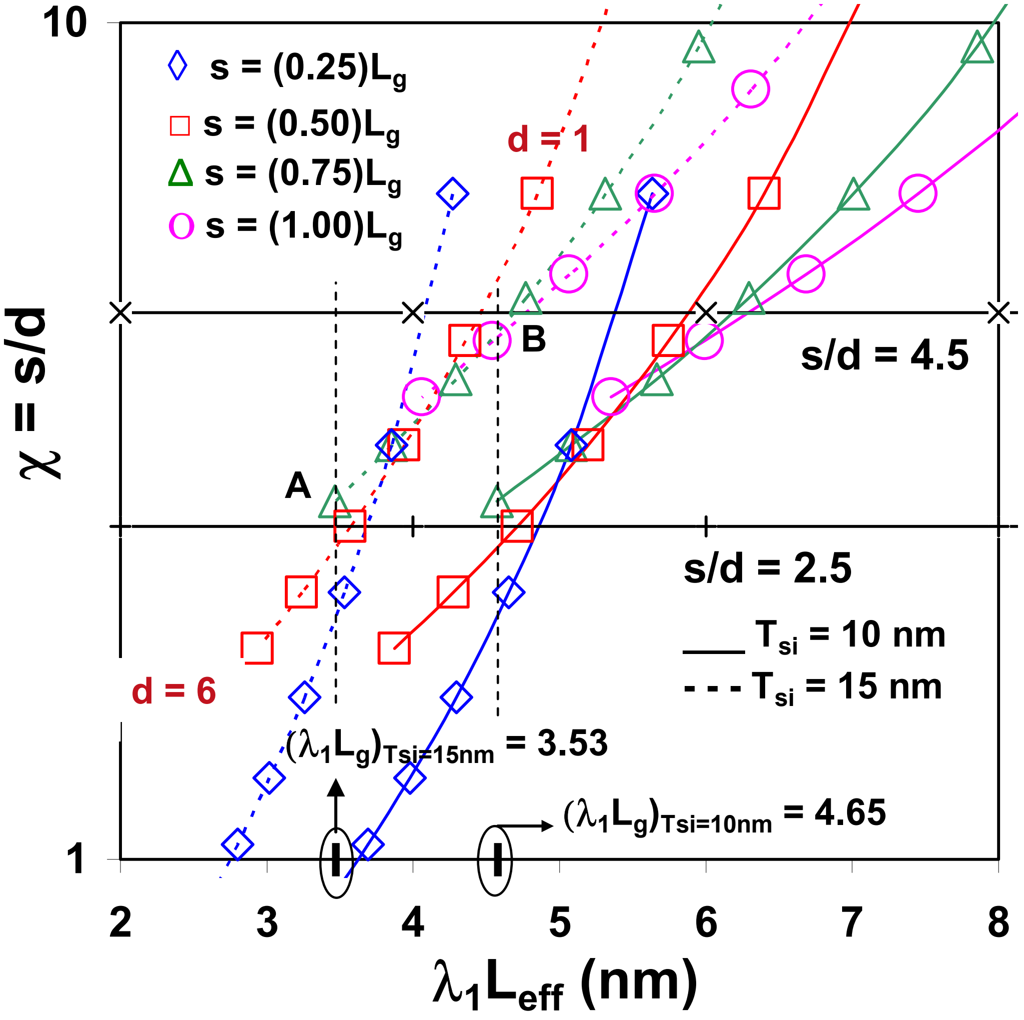
- If χ = s/d >> 4.5 this would lead to suppressed SCEs as $\lambda_1 L_{eff}$ >> 4, but longer L_{eff} will lower I_{on}.

- In an optimal design, the minimum value of χ (eg. $\chi \sim 5$) that results in $\lambda_1 L_{eff} \cong 4$ should be selected to reduce SCEs.



- The proposed compact model aids in selecting range of s/d, guiding the design trade-off between acceptable SCEs and parasitic series resistance.

Spacer-to-Gradient Ratio s/d

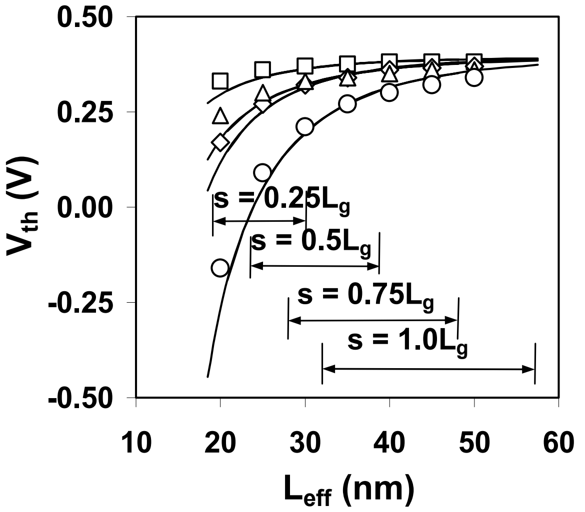


—————— $T_{si} = 0.4L_g$

- - - - - - - - $T_{si} = 0.6L_g$

d ranges from 1 – 6 nm/dec

S-slope, Threshold Voltage variation with L_{eff}

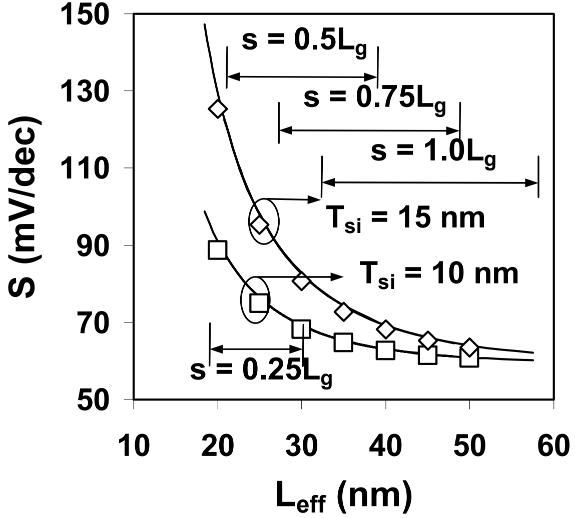


Δ: T_{si}=15nm, V_{ds}=50 mV

○: T_{si}=15nm, V_{ds}=1.1 V

□: T_{si}=10nm, V_{ds}=50 mV

◊: T_{si}=10nm, V_{ds}=1.1 V



□: T_{si}=10nm, V_{ds}=50 mV

◊: T_{si}=15nm, V_{ds}=50 mV

- The range of L_{eff} corresponding to the variation of d from 1 to 6 nm/decade is represented by horizontal lines for four different spacers. The shortest L_{eff} corresponds to s = 0.25L_g and d = 6 nm/dec whereas the longest L_{eff} represents s = L_g and d = 1 nm/dec.

High – κ Gate Dielectrics – V_{th} and S-slope

d = 5 nm/dec	**S-slope (mV/dec) Vds = 50 mV, s = 0.5Lg**	
ε_κ	Simulated	Model
3.9	65.70	65.67
10	74.44	77.48
25	85.60	90.38
d = 5 nm/dec	**Vth (V) @ Vds = 50 mV, s = 0.5Lg**	
ε_κ	Simulated	Model
3.9	0.331	0.343
10	0.326	0.338
25	0.292	0.298

- SDE region engineering can be effectively used to minimize Short Channel Effects in DG devices with high - κ gate dielectrics.

Conclusions

- An analytical model for SCEs in nanoscale DG SOI MOSFETs incorporates the effect of SDE region engineering through variation of doping gradient d and spacer width s.

- Two new scaling parameter – effect channel length L_{eff} and spacer-to-gradient ratio s/d have been defined and their significance established.

- Spacer-to-gradient ratio lying between 2.5 ($T_{si}/L_g = 0.4$) and 4.5 ($T_{si}/L_g = 0.6$) seems to be optimal for reducing short channel effects in without compromising on current.

- s/d ratio uniquely determines the doping density at the edge of the gate and approximates twice the number of decades of doping across the spacer.

- The model is applicable to high - κ dielectrics and scalable to shorter gate lengths

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