

An Explicit Quasi-Static Charge-Based Compact Model for Symmetric DG MOSFET

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Outline

- The Double-Gate (DG) MOSFET
- Derivation of the explicit compact model
- Model validation vs. 2D simulations
- Compact modeling with VHDL-AMS
- Conclusion

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How can we follow Moore's law?

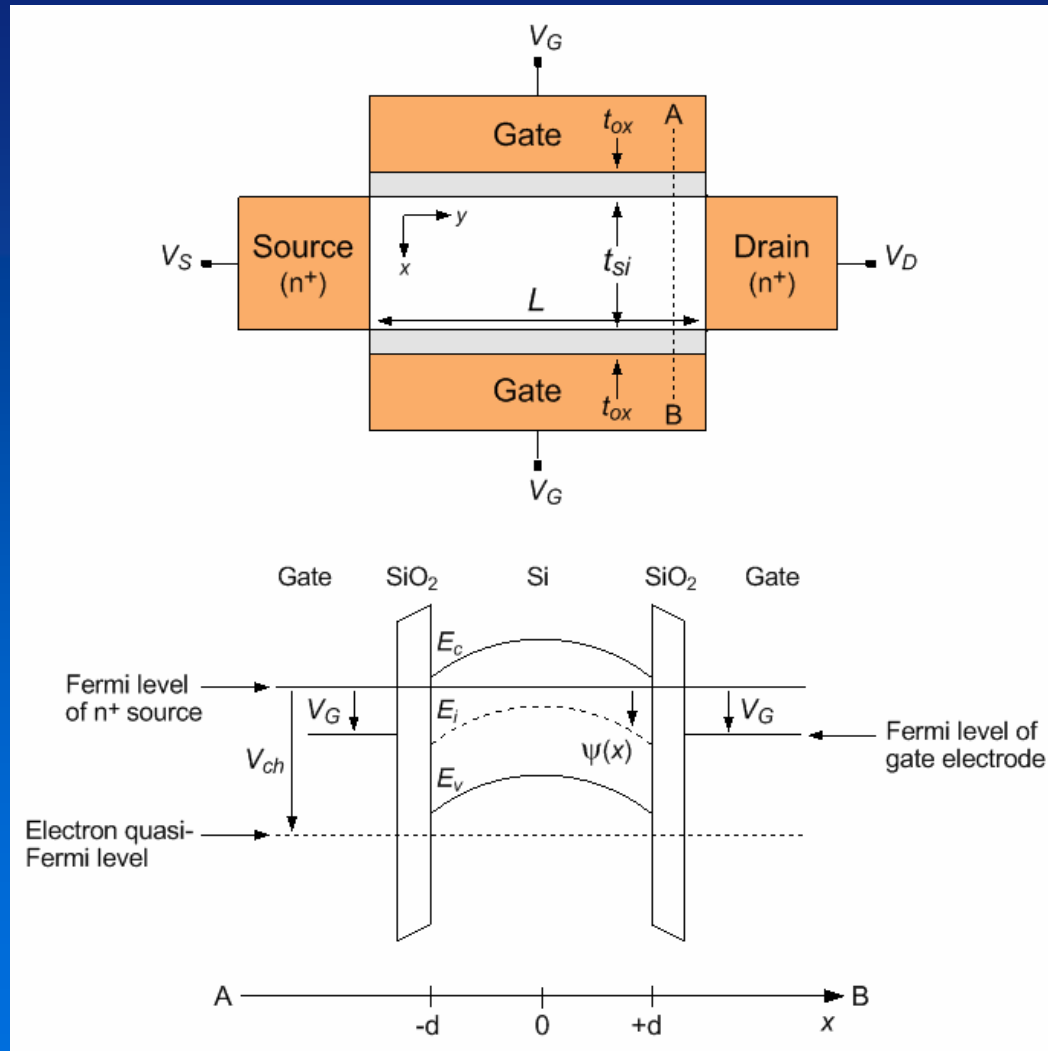
→ *By moving to DG MOSFETs*

DG might be the unique viable alternative to build nano-MOSFETs when $L_g < 50$ nm

Because:

- Better control of the channel from the gates
- Reduced short-channel effects
- Better I_{on}/I_{off}
- Improved sub-threshold slope (60 mV/decade)
- No discrete dopant fluctuations
- Typical values: $t_{ox} = 1-2$ nm, $t_{Si} = 10$ nm, $L_g = 25-100$ nm

DG MOSFET structure



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Taur's approach [1]

- *No more charge sheet approximation concept*
- Analytical solution for charges and current
- However,
 - the model is not explicit (iterations needed)
 - no simple analytical solution for g_m/I_d characteristic and for transcapacitances at $V_{ds} \neq 0$

[1] Y. Taur, X. Liang, W. Wang and H. Lu, "A Continuous, Analytic Drain-Current Model for DG MOSFETs," *IEEE Electron Device Letters*, vol. 25, no. 2, pp. 107-109, 2004.

Our new approach

- *An EKV-like formulation* [2]
- Based on a normalization of charges and current as in EKV (but with 2 gates):

$$Q_0 = 4 \cdot C_{ox} \cdot U_T$$

$$I_s = 4 \cdot \mu \cdot C_{ox} \cdot U_T^2 \cdot W / L$$

$$q_{int} = e \cdot n_i \cdot t_{si} / Q_0$$

[2] J.-M. Sallese, F. Krummenacher, F. Prégaldiny, C. Lallement, A. Roy and C. Enz, "A design oriented charge-based current model for symmetric DG MOSFET and its correlation with the EKV formalism," *Solid-State Electronics*, vol. 49, pp. 485-489, 2005.

Charge and current derivation

- Mobile charge density vs. potentials

$$v_g^* - v_{ch} - v_{to} = 4 \cdot q_g + \ln q_g + \ln \left(1 + q_g \cdot \frac{C_{ox1}}{C_{si}} \right)$$

- + drift-diffusion approximation =

$$i = -q_m^2 + 2 \cdot q_m + \frac{2}{\alpha} \cdot \ln \left(1 - \frac{\alpha \cdot q_m}{2} \right) \Big|_{q_{ms}}^{q_{md}} \quad \text{with} \quad \alpha = \frac{C_{ox1}}{C_{si}}$$

- ...and for $t_{si} \gg 1 \text{ nm}$, this reverts to the EKV MOSFET model relationships:

$$i \approx -q_m^2 + q_m \Big|_{q_{ms}}^{q_{md}}$$

An explicit model?

□ However,
$$v_g^* - v_{ch} - v_{to} = 4 \cdot q_g + \ln q_g + \ln \left(1 + q_g \cdot \frac{C_{ox1}}{C_{si}} \right)$$

is not an explicit relationship...

□ So, $i=f(q_m)$ needs to be solved numerically

→ this requires at least several iterations

□ This is not desirable for circuit simulation!

→ **solution: numerical inversion algorithm** [3]

[3] F. Prégaldiny, F. Krummenacher, B. Diagne, F. Pêcheux, J.-M. Sallese and C. Lallement, "Explicit modelling of the double-gate MOSFET with VHDL-AMS," *Int. Journ. of Numerical Modelling*, vol. 19, pp. 239-256, 2006.

Numerical inversion algorithm

- We can rewrite the relationship between charge and potentials as

$$v = 4 \cdot q + \ln[q \cdot (1 + \alpha \cdot q)] \quad (1)$$

- Then, we consider 2 cases: $q \gg 1$ and $q \ll 1$

→ $q \gg 1$: using a first-order series expansion of $\ln[q(1+\alpha q)]$ around q_t and after some maths, we get

$$q = \frac{1}{4} \cdot \{v - \ln[q_0 \cdot (1 + \alpha \cdot q_0)]\} \quad (2)$$

→ $q \ll 1$: the logarithmic term becomes dominant. We can rewrite (1) as

$$v = \ln q + 4 \cdot e^{\ln q} + \ln(1 + \alpha \cdot e^{\ln q}) = \ln q + \frac{1}{F_w(\ln q)}$$

Numerical inversion algorithm

where $F_w(\ln q) = \frac{1}{4 \cdot q_t \cdot e^{\Delta \ln q} + \ln(1 + \alpha \cdot q_t \cdot e^{\Delta \ln q})}$ with $\Delta \ln q = \ln q - \ln q_t$

Then, using a first-order series expansion around $\Delta \ln q = 0$ and after some maths, we get

$$v = 4 \cdot q_0 + \ln[q \cdot (1 + \alpha \cdot q)]$$

which yields

$$q = \frac{e^{(v-4 \cdot q_0)}}{\frac{1}{2} + \sqrt{\frac{1}{4} + \alpha \cdot e^{(v-4 \cdot q_0)}}} \quad (3)$$

- The final step is the combination of both previous cases. For this, we need to define a *transition potential* v_t which simply corresponds to $q=q_t$

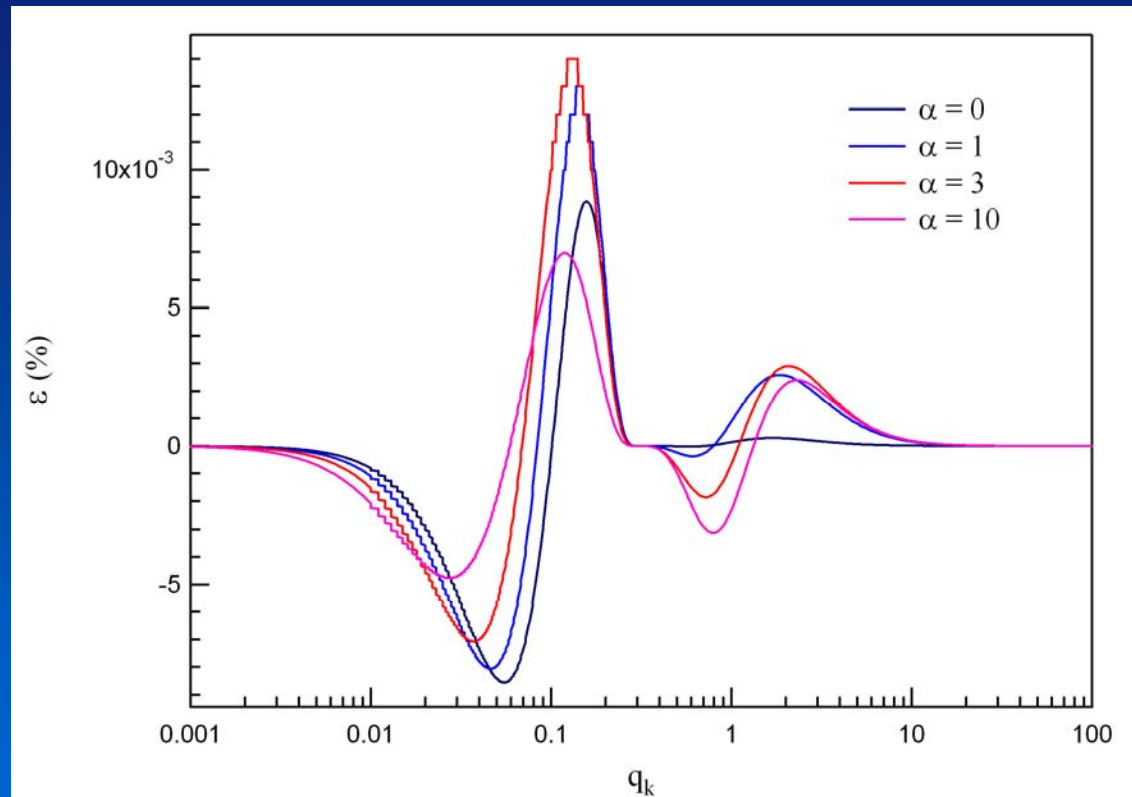
Numerical inversion algorithm

- For each case ($q \gg 1$ and $q \ll 1$), we compute the function δ that linearizes the difference expression between q and q_0
- At last, we obtain an explicit relationship for the mobile charge density, given by

$$q = q_0 \cdot [1 + \delta \cdot (1 + k \cdot \delta)]$$

- Accuracy of the algorithm: checked for realistic values of the “factor form” $\alpha = C_{ox1}/C_{si}$

Error due to the numerical inversion



□ Maximum error is lower than 0.014%

→ Explicit approximation well-suited for a compact model

→ Computation time reduced by more than a factor of 1000

Small signal parameters

- $i \approx -q_m^2 + q_m \left| \frac{q_{md}}{q_{ms}} \right|$ means that the formulation of the current model reverts to the classical charge sheet approximation for bulk and SOI MOSFETs...

... but with the mobile charge q_m corresponding to the DG devices!

- This implies two important points:
 - (trans)capacitances can be derived in the same way as bulk MOSFET ones
 - we can easily obtain a fully analytical form of the g_m characteristic, and hence g_m/I_d as well

(Trans)capacitances derivation

- Capacitances evaluation requires to calculate source and drain charges

$$Q_S = \int_S^D Q_i(x) \cdot (1-x) \cdot dx$$

$$Q_D = \int_S^D Q_i(x) \cdot x \cdot dx$$

- So the integral should have an analytical solution

$$C_{ij} = dQ_i / dV_j$$

Capacitances derivation

- We have to simplify the i vs. q_m relationship

$$i = -q_m^2 + 2 \cdot q_m + \frac{2}{\alpha} \cdot \ln \left(1 - \frac{\alpha \cdot q_m}{2} \right) \Big|_{q_{ms}}^{q_{md}} \quad \longrightarrow \quad i = -q_m^2 + 2 \cdot q_m \Big|_{q_{ms}}^{q_{md}} = i_f - i_r$$

where i_f and i_r are the forward and reverse normalized current

- Then, using a new normalization we can define

$$i_0 = -q_0^2 + q_0 \Big|_{q_{0s}}^{q_{0d}} = i_{f0} - i_{r0}$$

which is exactly the EKV formulation derived for bulk MOSFET. *So, the results of [4] may be applied here:*

→ *Definition of new normalized variables χ_f and χ_r*

→ *Capacitances are expressed as a function of both χ_f and χ_r*

[4] J.-M. Sallese and A.-S. Porret, "A novel approach to charge-based non-quasi-static model of the MOS transistor valid in all modes of operation," *Solid-State Electronics*, vol. 44, pp. 887-894, 2000.

Capacitance matrix

- The whole capacitance matrix may be fully determined from 4 components :

$$C_{dg}, C_{sg}, C_{ds}, C_{sd}$$

- For instance, the C_{dg} capacitance is given by

$$\frac{C_{dg}}{C_{OX}} = -\frac{1}{15} \cdot \left[\frac{4\chi_f^3 + 6\chi_r^3 + 28\chi_f^2\chi_r - 10\chi_f^2}{(\chi_f + \chi_r)^3} + \frac{-15\chi_f\chi_r + 22\chi_f\chi_r^2 - 5\chi_r^2}{(\chi_f + \chi_r)^3} \right]$$

Capacitance matrix

- The other capacitances are then expressed as a function of C_{dg} , C_{sg} , C_{ds} and C_{sd}

$$C_{ss} = -C_{sg} - C_{sd}$$

$$C_{dd} = -C_{dg} - C_{ds}$$

$$C_{gd} = +C_{sd} + C_{ds} + C_{dg}$$

$$C_{gs} = -C_{sd} + C_{ds} - C_{sg}$$

$$C_{gg} = +C_{sg} - C_{dg}$$

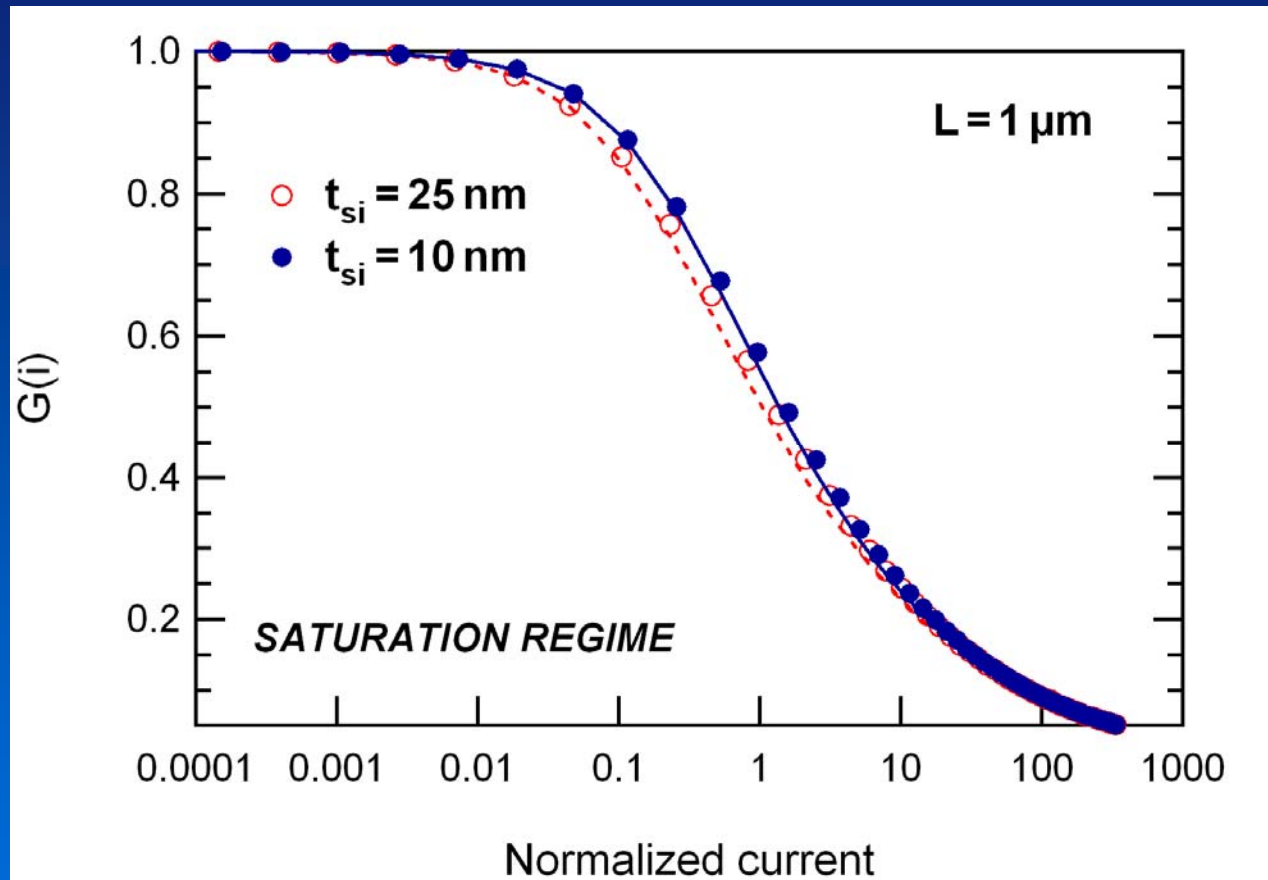
Transconductance to current ratio

- $G(i) = g_m / I_d$ evaluated in saturation
- An approximate form may be analytically obtained

$$G(i) \stackrel{\text{sat}}{=} \frac{-1}{i} \cdot \frac{di}{dv_s} = \frac{-U_T}{I_d} \cdot \frac{dI_d}{dV_s}$$
$$\approx \left\{ \left(\frac{1}{2} + \sqrt{\frac{1}{4} + i} \right) + 1 + \frac{2}{\alpha \cdot \left(\frac{1}{2} - \sqrt{\frac{1}{4} + i} \right)} \cdot \ln \left[1 + \frac{\alpha}{2} \cdot \left(-\frac{1}{2} + \sqrt{\frac{1}{4} + i} \right) \right] \right\}^{-1}$$

$G(i)^{-1}$ as derived
for bulk MOSFETs

Transconductance to current ratio



Dots: exact (implicit) solution (Taur et al., *IEEE EDL*, vol. 25, p. 107, 2004)

Lines: explicit solution (Prégaldiny et al., *IJNM*, vol. 19, p. 239, 2006 +
Sallese et al., *SSE*, vol. 49, p. 485, 2005)

Small geometry effects

- Decrease of threshold voltage Δv_{to} with increasing drain voltage: **DIBL**

→ Analytical modeling: $\Delta v_{to} = -\gamma \cdot D(v_g) \cdot v_{ds}$

→ The normalized gate charge becomes

$$q_g = f(v_g - \Delta v_{to}, v_{ch})$$

- Mobility degradation

→ Model for vertical-field dependence: μ_{\perp}

→ Full model (\parallel and \perp field dependence): μ_{eff}

→ Mobility models based on explicit expression of q_g

Denormalization of the drain current

- The drain current, in A, may be expressed as

$$I_d = \beta \cdot i$$

with

$$\beta = 4 \cdot \mu_{\text{eff}} \cdot C_{ox1} \cdot U_T^2 \cdot \frac{W}{L}$$

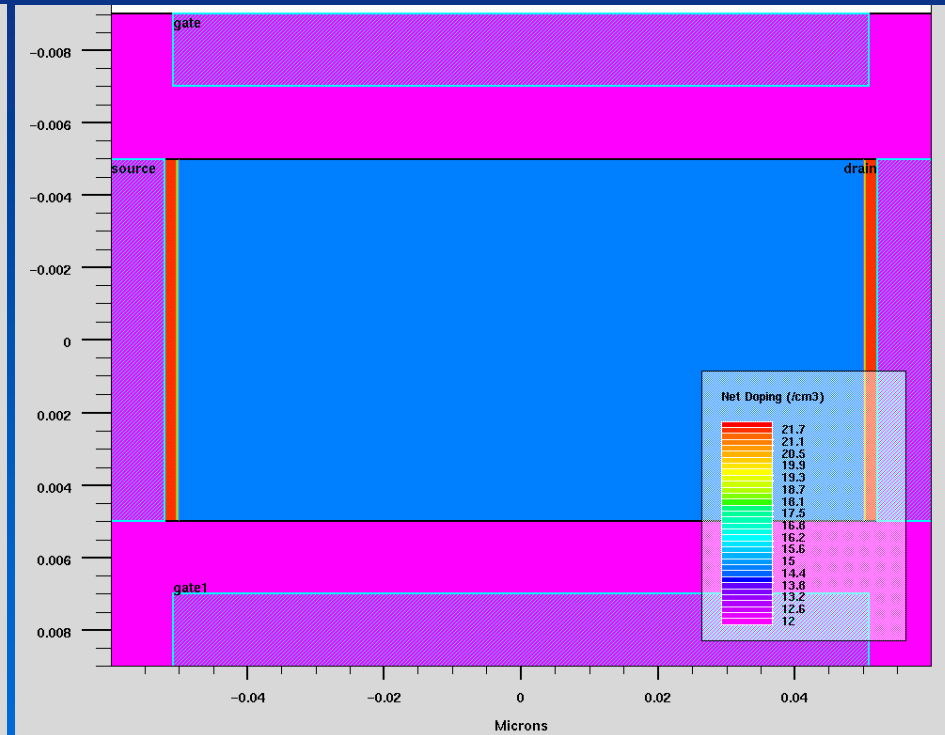
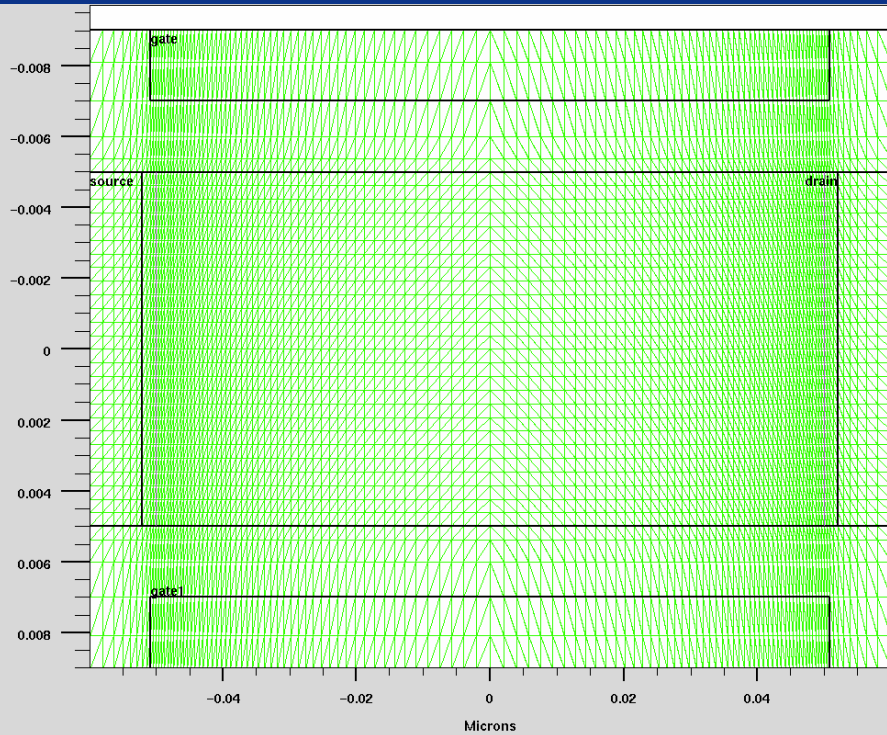
- Model valid for DG devices with
 - channel length down to 100 nm
 - silicon layer (body thickness) down to 10 nm

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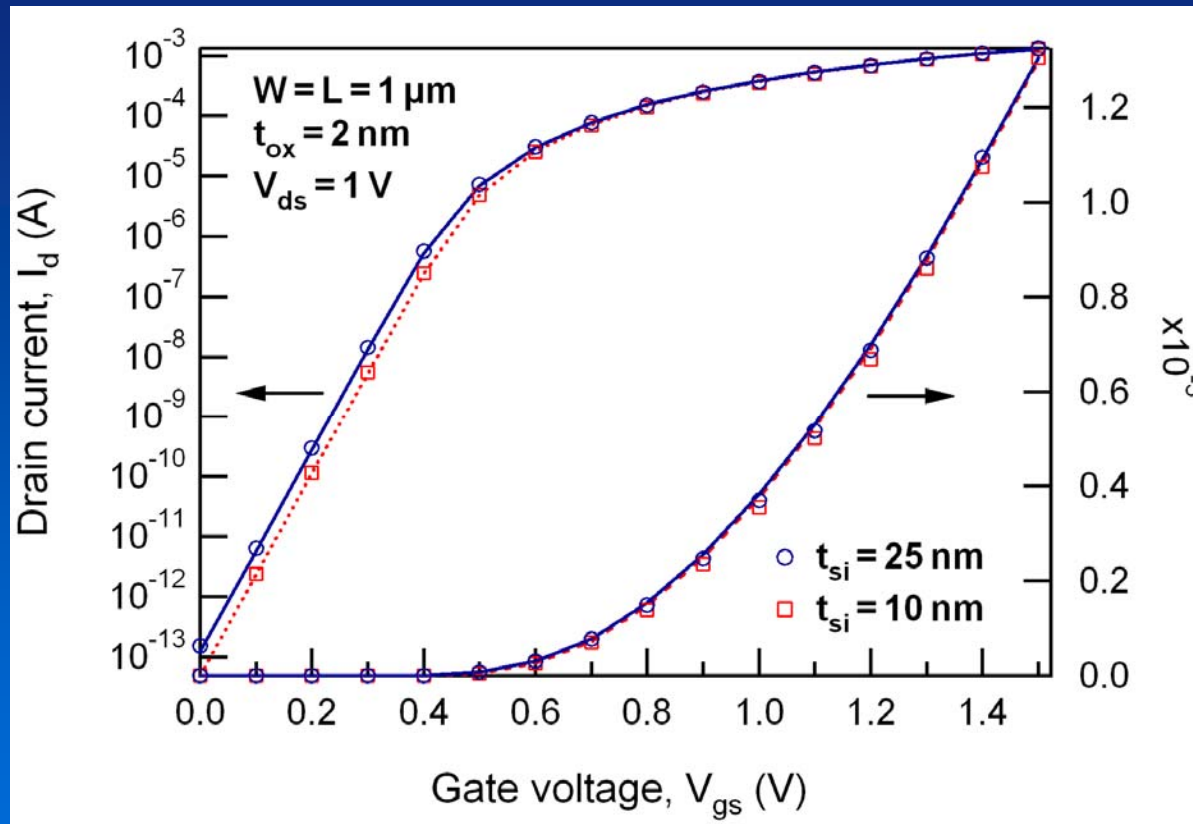
The 2D simulations

Structures developed under Atlas (Silvaco)



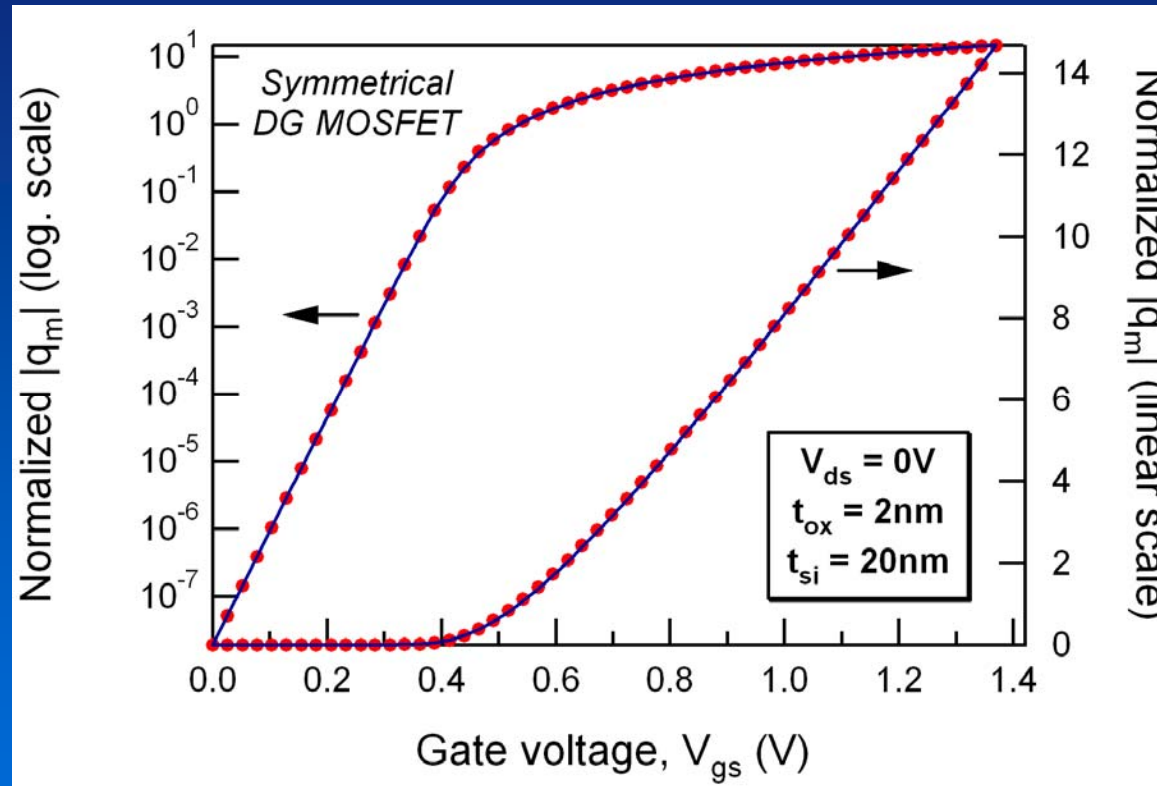
$$t_{ox}=2\text{nm} - t_{si}=10 \Rightarrow 50\text{nm} - L=100\text{nm} \Rightarrow 1\mu\text{m}$$

Model vs. 2D simulations



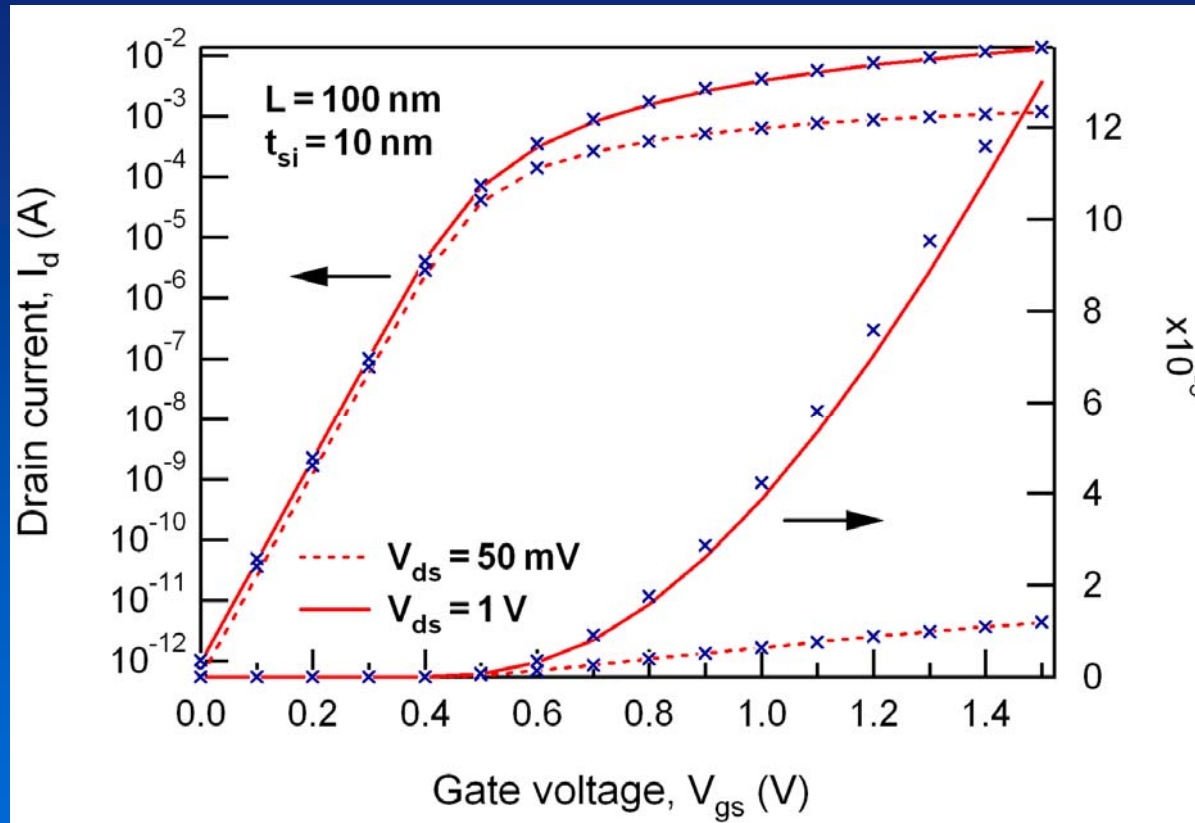
- ▶ Drain current I_d as a function of V_{gs} for different t_{si}

Model vs. exact Taur's formulation



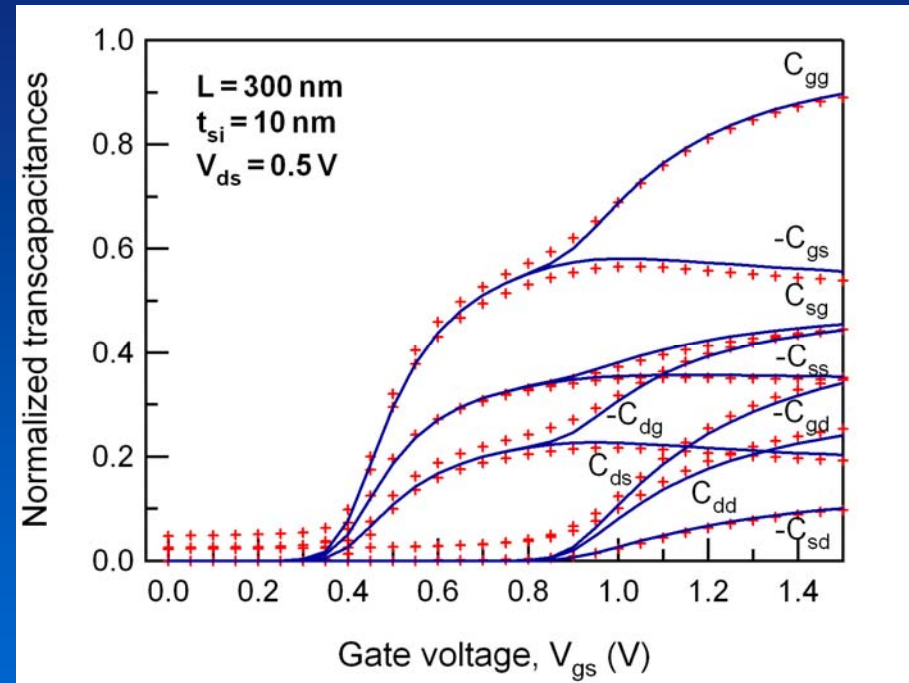
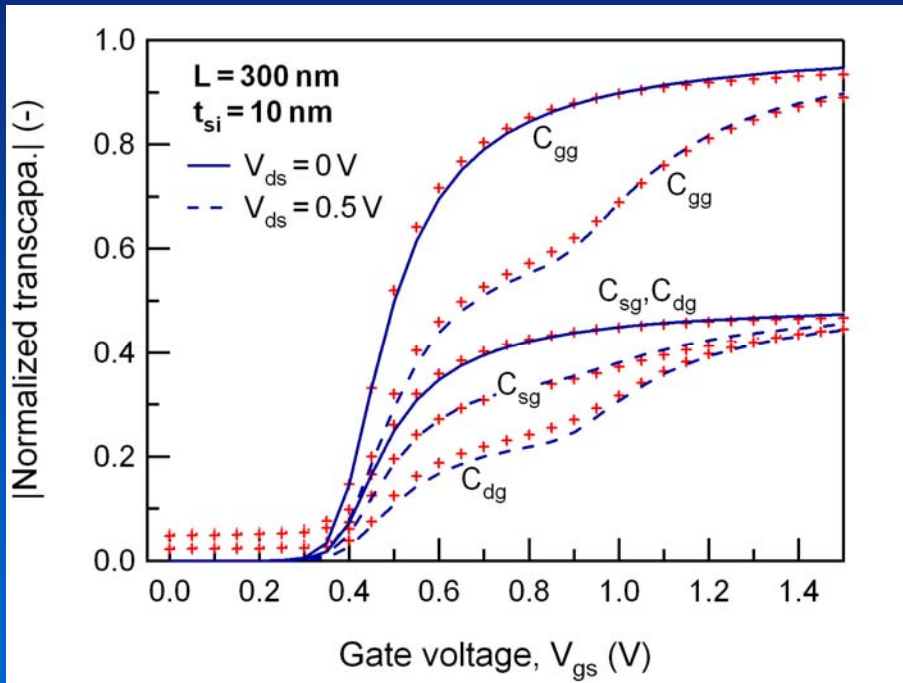
- ▶ Normalized inversion charge density as a function of V_{gs}
Symbols: Taur's model ; lines: our analytical model

Model vs. 2D simulations



- ▶ Drain current I_d for a short-channel device
Symbols: 2D results ; lines: our analytical model

Model vs. 2D simulations



► Transcapacitance matrix as a function of V_{gs} at different V_{ds}

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VHDL-AMS code: *the structure*

ENTITY:

- parameters
- terminals

```
entity dg_mosfet is
    generic (W    :real :=1.0e-6;  -- Gate width
             L    :real :=100.0e-9; -- Gate length
             .../...          ); -- Other parameter
    port (terminal g1,g2,d,s :electrical);
end;
```

ARCHITECTURE:

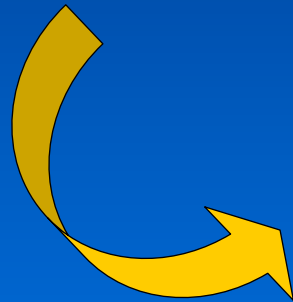
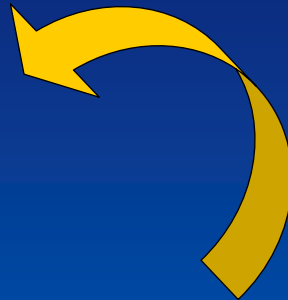
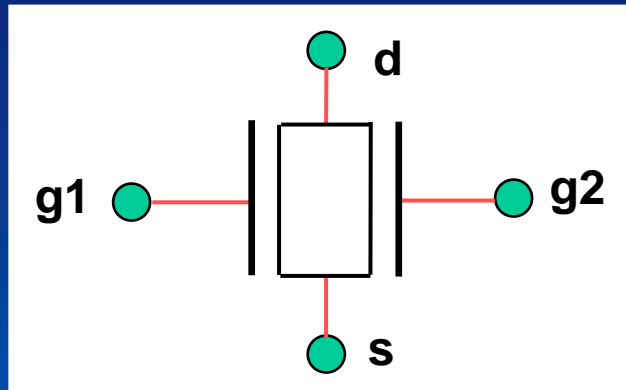
- quantities
- functions

Computation of:

- charges,
- drain current,
- capacitances

```
architecture symmetric of dg_mosfet is
    -- Physical constants
    constant q    :real := 1.602e-19; .../...
    -- Operating conditions
    constant Tc   :real := 27.0;
    constant Tk   :real := Tc+ 273.0; .../...
    -- Quantities definitions
    quantity vg1 across g1 to electrical_ref; .../...
    -- Definition of the qi1n function
    pure function qi1n(vg,v :real) return real is
    .../...
    begin
    end qi1n;
begin
    -- Drain current
    ids == ... ;
    -- Capacitances
end;
```

VHDL-AMS code: *the entity*



```
library ieee;
use ieee.electrical_systems.all;

entity dg_mosfet is
    generic (W      :real :=1.0e-6; -- Gate width
            L      :real :=100.0e-9; -- Gate length
            tox1   :real :=2.0e-9; -- Gate oxide thickness
            tsi    :real :=10.0e-9; -- Silicon film thickness
            sigma  :real :=0.03; -- DIBL parameter
            mu0    :real :=0.1; -- Low-field mobility
            theta  :real :=0.08; -- Mobility parameter 1
            E0     :real :=8.0e5; -- Mobility parameter 2
            vsat   :real :=3.0e7); -- Mobility parameter 3

    port (terminal g1,g2,d,s :electrical);
end;
```

VHDL-AMS code: *the function qi1n*

To determine the normalized charge at both source and drain sides

```
-- Function definition  
  
pure function qi1n(vg,v :real) return real is  
  variable alpha, qt, pt, lnqt, .../..., da : real;  
begin  
  -- Precomputed parameters  
  alpha:=Cox1/Csi;  
  qt:=0.3;  
  pt:= 1.0 + alpha*qt;  
  lnqt:= log(qt); .../...  
  vtest:= vp - v;  
  
  if (vtest > vt) then  
    .../...  
    return -q0*(1.0+da+(1.0 + 0.13*da));  
  else  
    .../...  
    return -q0*(1.0+da+(1.0 + 0.35*da));  
  end if;  
end;
```

*Definition of
the function*

Computed with no iteration

VHDL-AMS code: *the architecture*

```
use ieee.math_real.all;

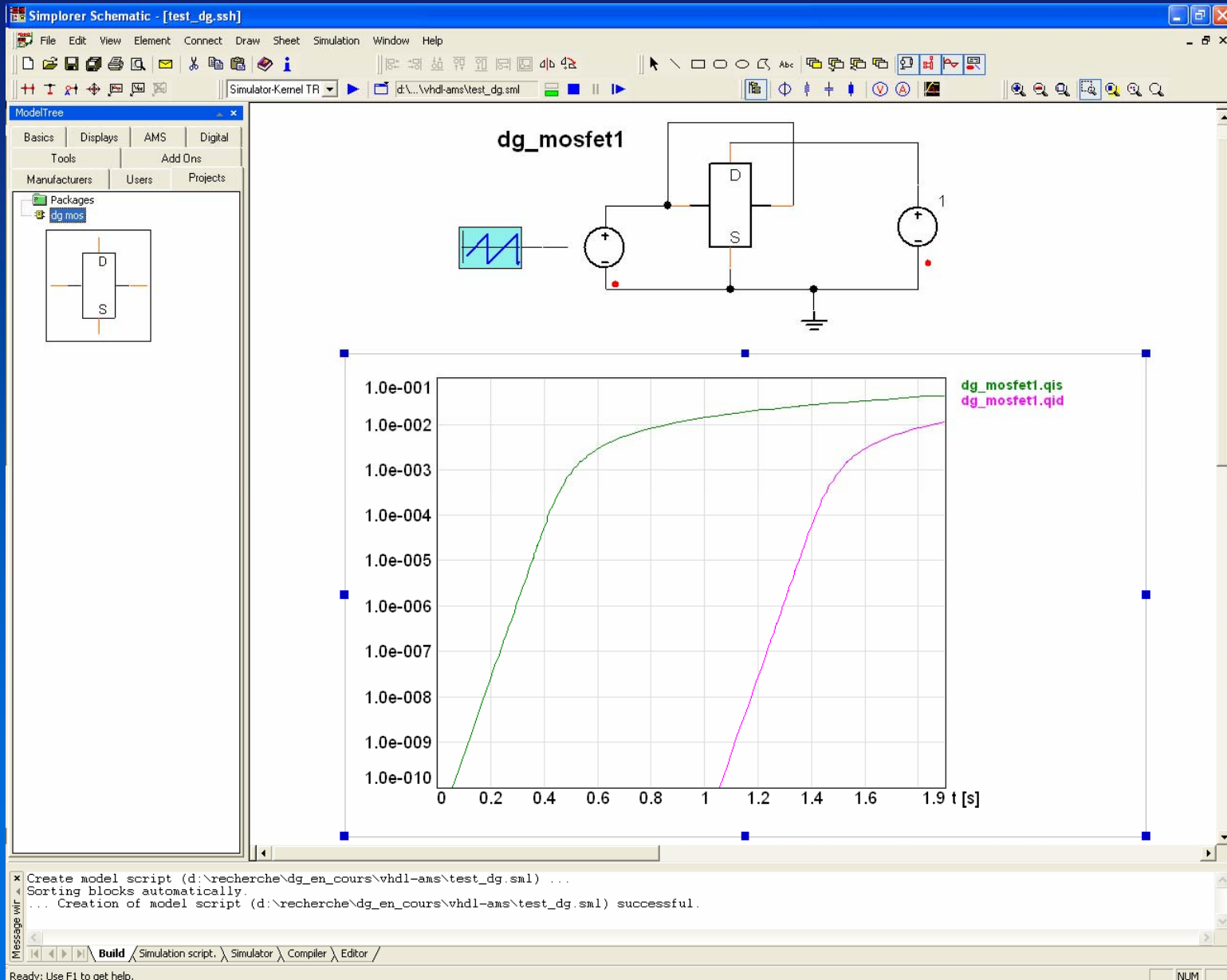
architecture symmetric of dg_mosfet is
    .../...
    quantity  vg1      across  g1   to  electrical_ref;
    quantity  vg2      across  g2   to  electrical_ref;
    quantity  vd       across  d    to  electrical_ref;
    quantity  vs       across  s    to  electrical_ref;
    quantity  ids      through  d    to  s;
    .../...
    quantity  vg1n, vg2n, vsn, vdn :real;
    quantity  Inf, Inr, Xf, Xr      :real;
    quantity  Csg, Cdg, .../..., Cgg :real;

    -- Definition of the qi1n function
    pure function qi1n(vg,v :real) return real is
    .../...
    begin
    end qi1n;
begin
    -- Normalized voltages
    vg1n == vg1/UT;  vg2n == vg2/UT;  vsn == vsn/UT;  vdn == vg1/UT;

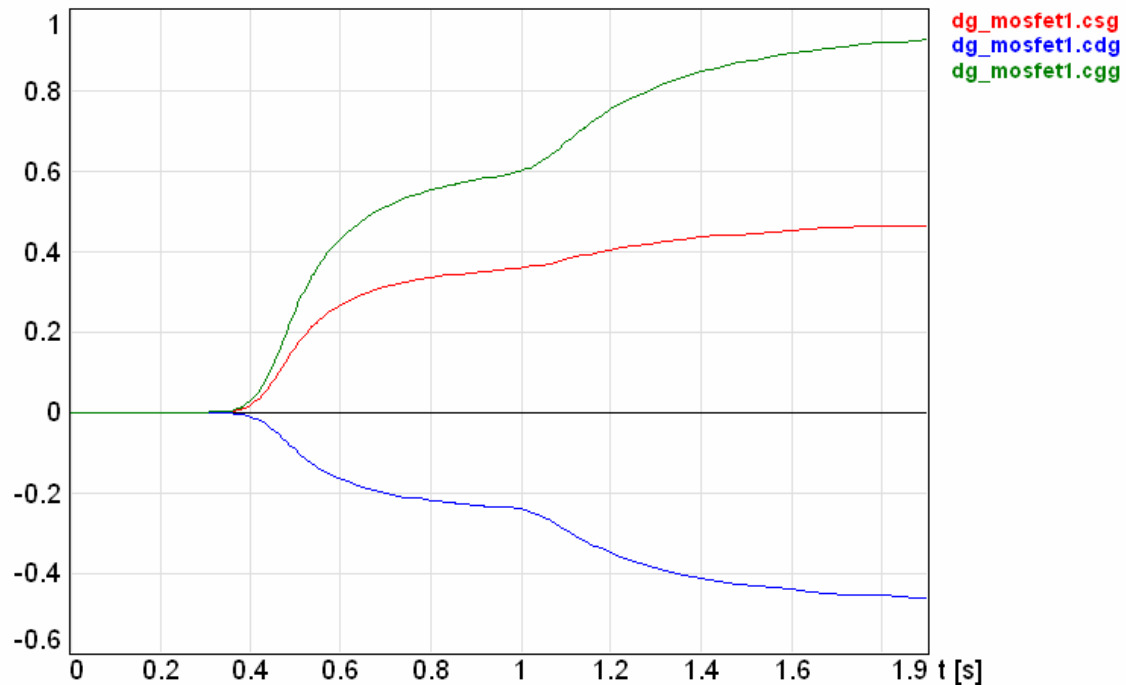
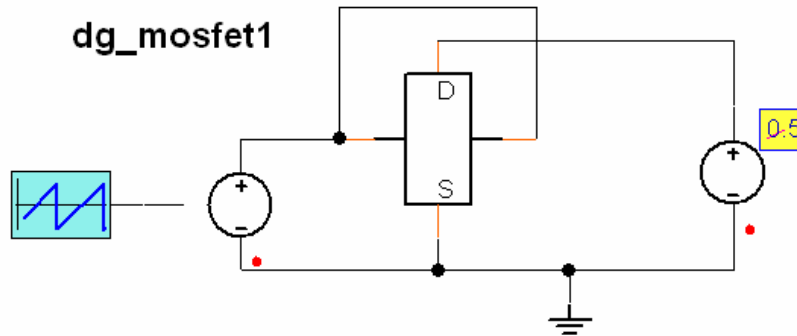
    -- Drain current
    ids == IDO*(-4.0*qi1n(vg1n,vdn)**2 + 4.0*qi1n(vg1n,vsn)**2 + ...);

    -- Capacitances
    Inf == ...;  Inr == ...;  Xr == ...;  Xf == ...;  Csg == ...;  Cdg == ...;  .../...;
end;
```

VHDL-AMS simulations



VHDL-AMS simulations



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Conclusion

- ❑ An explicit DC and AC quasi-static compact model for symmetric DG MOSFETs has been presented
- ❑ Computation time is no longer an issue
- ❑ All quantities in the model are expressed in terms of normalized variables → helpful for developing efficient design methodologies
- ❑ The model is well-suited for circuit simulation: translating the model in VHDL-AMS is straightforward
- ❑ **Forthcoming work:** QME, overlap capacitance and threshold voltage roll-off

Thank you !

Acknowledgments: Dr. Xing Zhou
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