Workshop on Compact Modelling

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Enhanced Junction Capacitance Modelling

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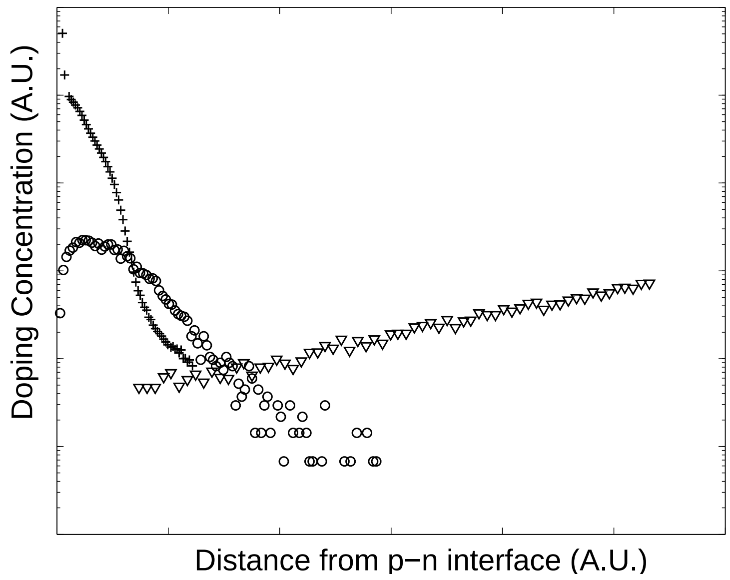
VCO design places focus on varactor modelling
Commonly used varactor is hyperabrupt junction

Standard junction capacitance model assumes a power-law doping profile

SIMS shows profile is sum of exponential profiles



New Methodology employing Verilog-A
Standard methodology for junction fields and voltages

- **Principle of Superposition to treat each individual exponential profile separately and then add results**
- **Use Gauss's Law to integrate over depletion region to determine D field**
- **Size of depletion regions in anode and cathode are related by continuity of D field at junction itself.**
- **Integrate a second time to get voltage drop from resulting field**

New Verilog-A Methodology

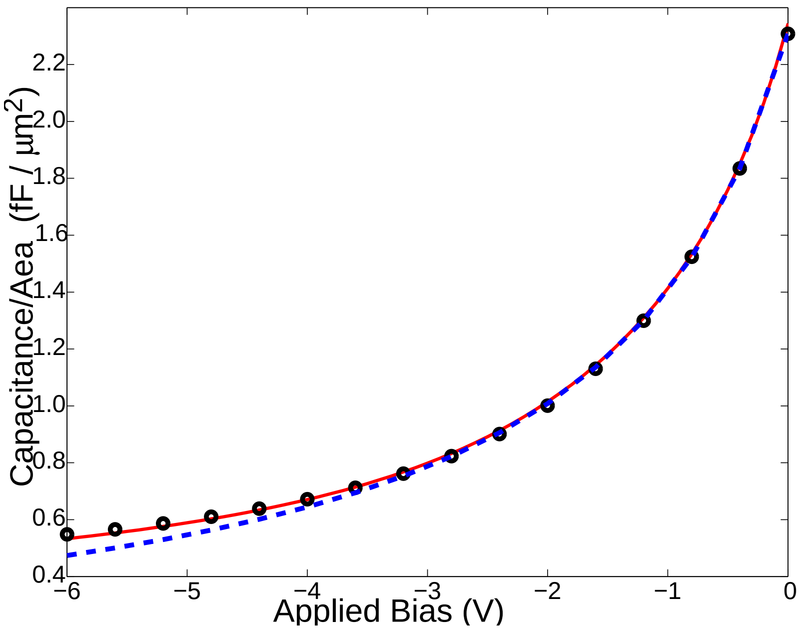
- **Sum of voltage drops should equal the built-in potential across the junction plus the applied bias**
- **Iteratively adjust depletion region size to satisfy this requirement about the voltages**
- **Find Q, "charge stored on plates," and employ Verilog-A *ddt* operator to get the current**

Results

- **Good fit to data over extended voltage range**
- **Parameters are physical and directly related to process parameters: amount of dopant and energy of implant**
- **Remaining parameter Vbi (built-in potential) can be adjusted with temperature to capture temperature effects**
- **May be issues with including proprietary process information within the model**

Results

Results versus Standard Model



Results over Temperature

-40C, 25C and 125C