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Analog Compact Modeling for a 20-120V HV CMOS Technology

HV CMOS transistor, Sub-circuit modeling, mismatch modeling.

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a leap ahead

Presentation Overview

- HV LDMOS transistor sub-circuit modeling
  - DC & AC modeling
  - Modeling of HV LDMOS parasitics
- Mismatch considerations for HV LDMOS

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State of the art Model Solutions

Sub-circuits (Macro model):

- Compatible to all simulators
- Higher simulation time, convergence

Compact Model with internal node:

- Node solved internally or from the simulator
- Higher simulation time, convergence

Compact Model:

- Combination of the low voltage MOS region with the high voltage drift region without internal node.
- Short computation time

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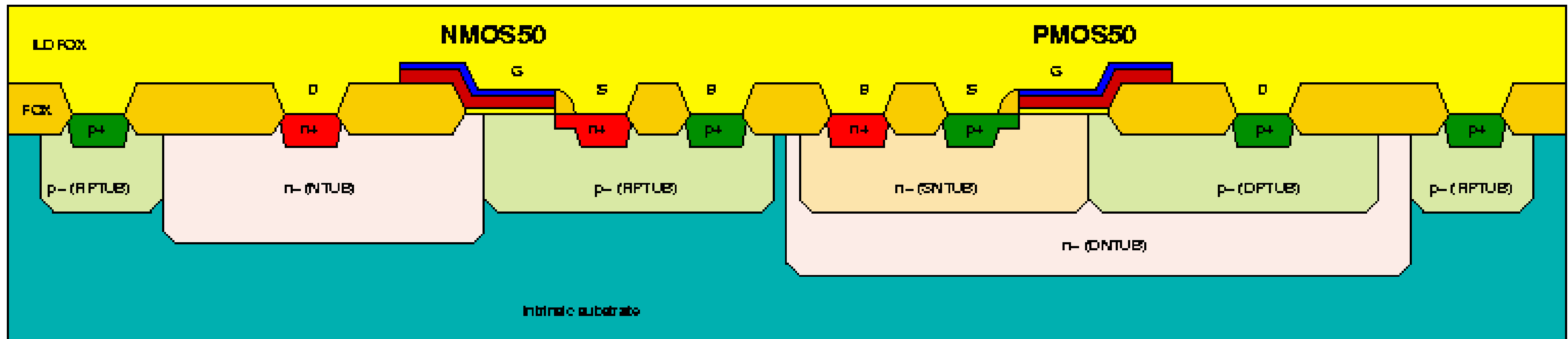
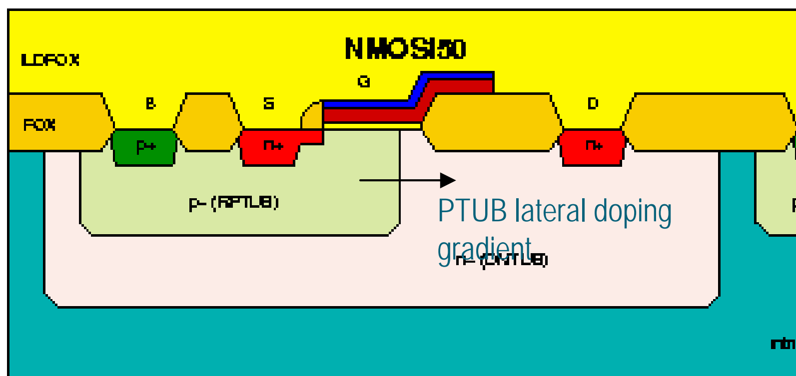
HV LDCMOS Device X-section

HV NMOS substrate based



HV NMOS isolated



automotive applications,

switching power supplies

and amplifiers

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HV LDMOS Transistor Model HV/analog Requirements

- DC & AC characteristic
  - Scalability of W & L, Quasi-Saturation, intr. & extr. caps
- Symmetrical and unsymmetrical, source & drain res and cap.
- Voltage up to 120V & Temperature behavior up to 180°C
- Noise Modeling (1/f, thermal)
- Capable of creating statistical models
  physical parameter sets (WC corner & MC)
- Substrate current modeling (diodes and bipolars)
- Device mismatch for LDMOS parameters

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Sub - circuit modeling overview

DC & AC modeling:

-M0 BSIM3v3 model (standard effects)

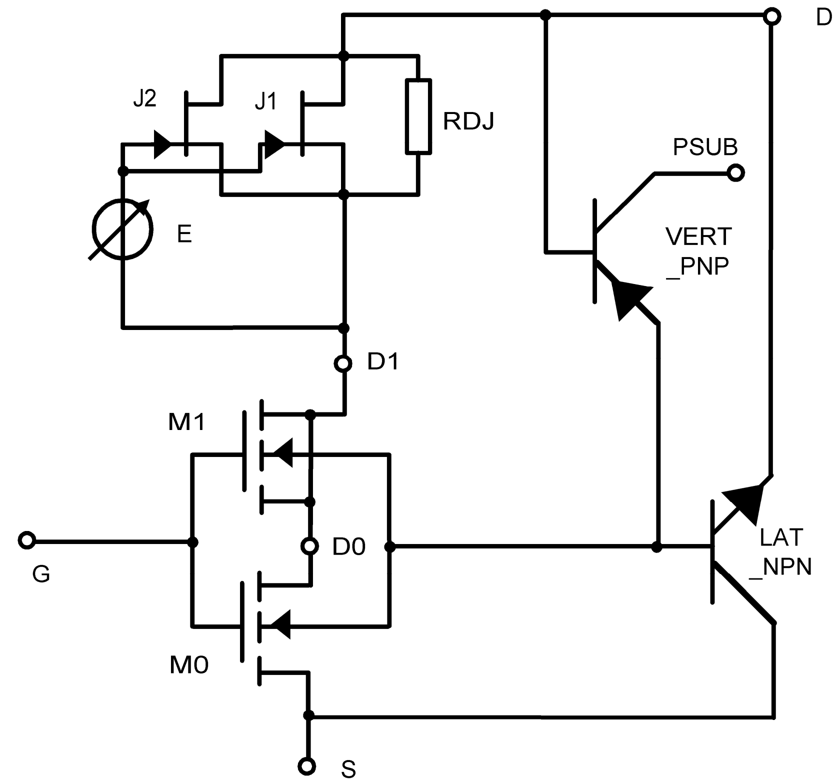
-M1 BSIM3v3 model (lateral doping effect & overlap caps)

-RDJ (RON for low current regime)

-J2 & J1 JFET (quasi saturation effect)

-E voltage source (length scalability)

-VERT_PNP & LAT_NPN (parasitic capacitances and substrate currents.



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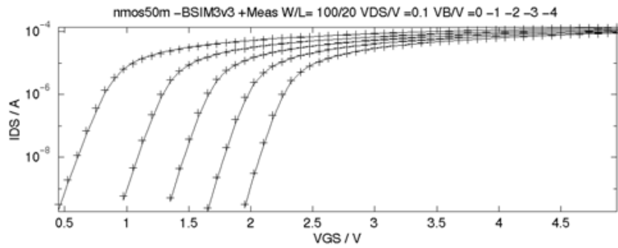
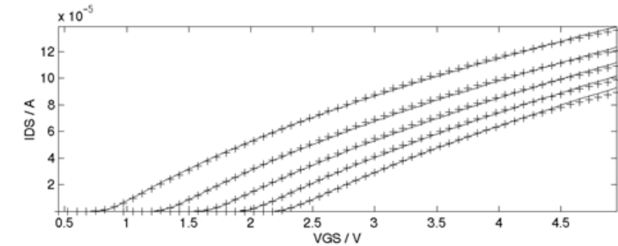
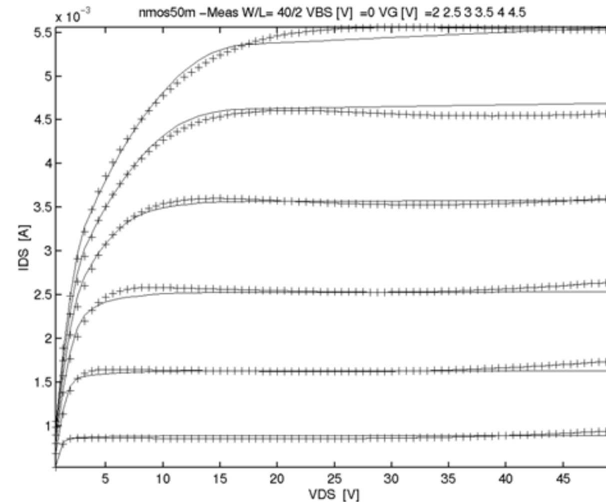
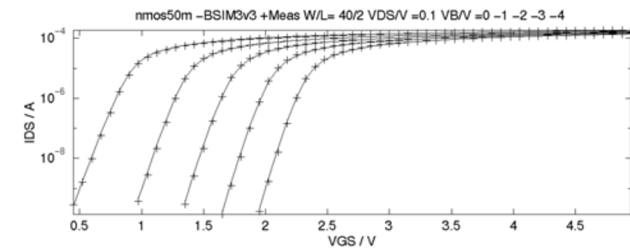
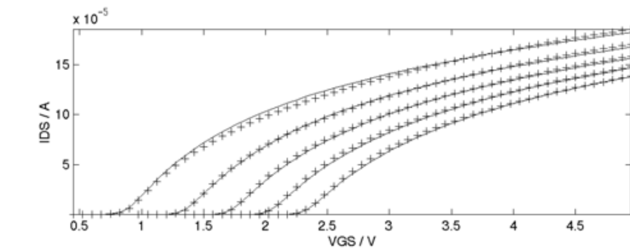
Results DC Model large and short device

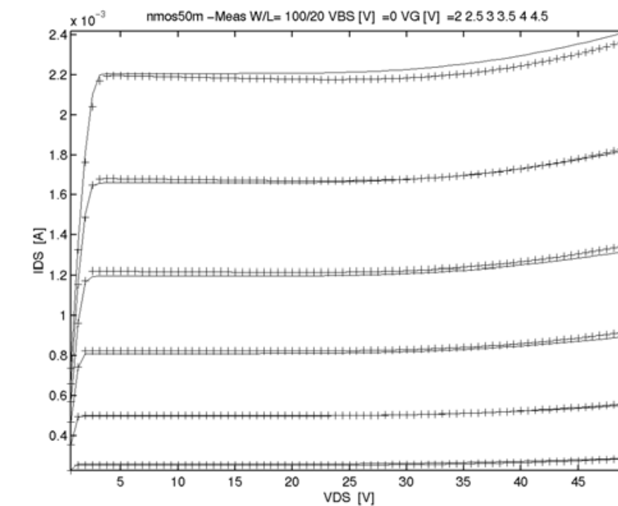












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Results AC Model

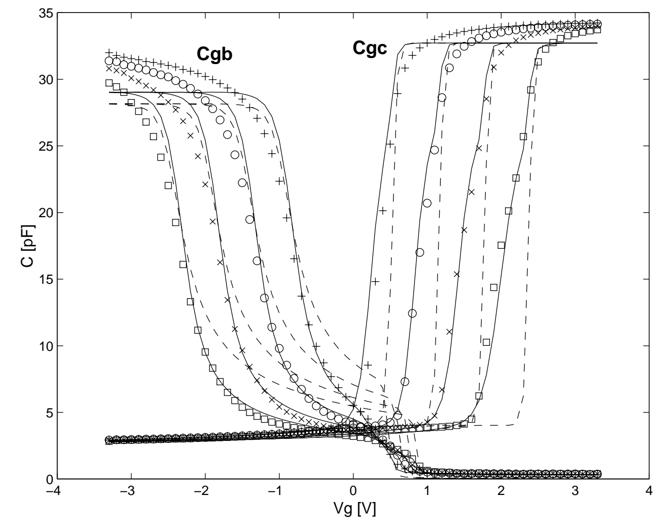
-Intrinsic capacitances are influenced by lateral-doping gradient in the p-type region under the gate oxide

-Gate above the less doped body adds a MOS capacitance in parallel

-Lateral doping gradient is taken into account by M1 with shortened source and drain

-M1 parameters can be adjusted without affecting the DC model.

-M1 is used for modeling the gate to source and the gate to drain overlap capacitance



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Presentation Overview

- HV LDMOS transistor sub-circuit modeling
  - DC & AC modeling ✓
  - **Modeling of HV CMOS parasitics**
- Mismatch considerations for HV CMOS

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HV MOS Parasitic Elements

-Usage of standard S/D diodes in MOS transistor model is not possible

-Bipolar effects occur, when parasitic diodes are forward biased and result in reasonable substrate currents.

-Model must include parasitic bipolar effects for substrate current description

-The parasitic diodes and BJT equations must be scalable by MOS- transistor width and length

-Number of devices should be low as possible. Avoided lateral bipolar for lower complexity.

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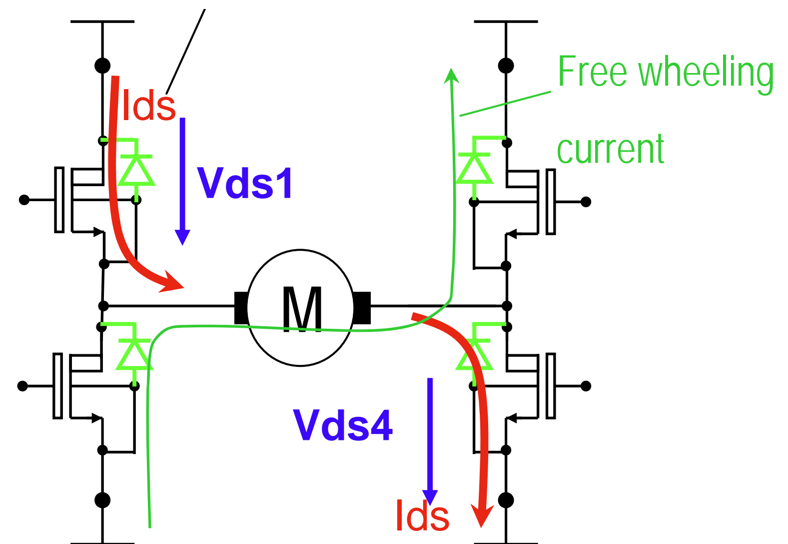
H- Bridge induces a parasitic substrate current

- Ids …. Forward current
- Free wheeling current ….

off motor and VGS =0 results in inductive current

- parasitic pnp transistor occurs.



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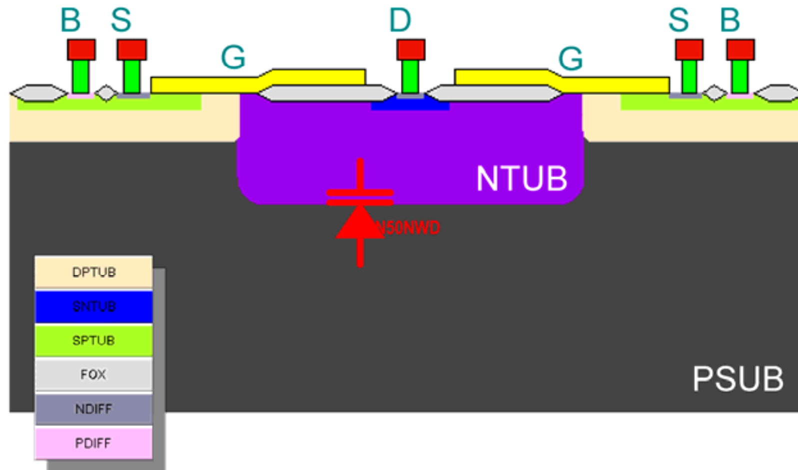
HV LDMOS Transistor parasitics

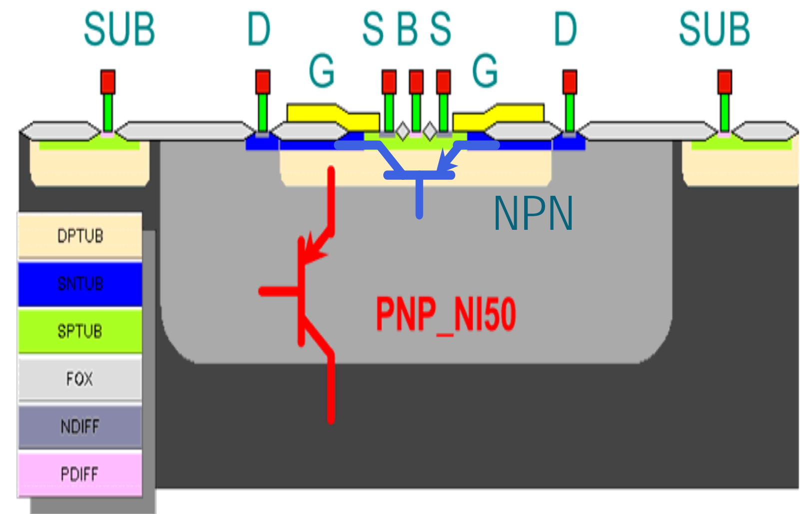


Additional parasitics:
Diode structure between MOS body and drain

Scaling parameters:
JS, JSW
CJ, CJSW

Instance parameters:

$$AREA = 2.75e-06 * (w + 16e-06)$$
$$PERIMETER = (11e-06 + w + 16e-06)$$



Additional parasitics:
PNP structure between MOS body (Emitter), MOS drain (Base) and substrate (Collector)

Used model:Gummel Poon

Scaling parameters:
IS, IKF, IBEI, BF
CJE, CJC

Instance parameter: $AREA = w * l$

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Parasitic Bipolar Transistor Scaling

-Models must be scalable for enabling the designer to select MOS devices of arbitrary length (L) and width (W).

-Parasitic bipolar scaling is assumed by the LDMOS device area.

-Therefore the area parameter of the parasitic bipolar transistor has to be a combination of MOS transistor length and width.

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Parasitic Bipolar Details

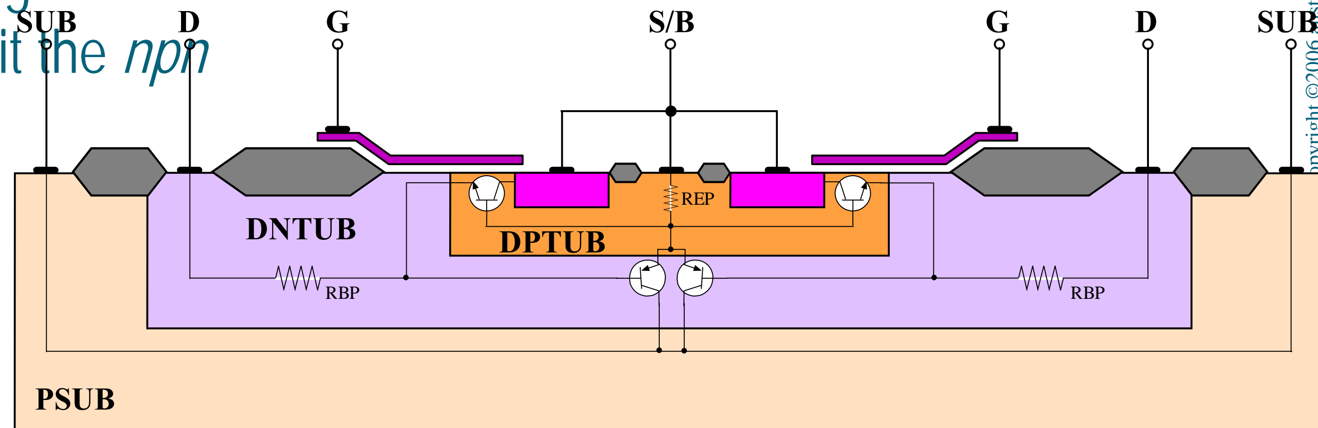
-Main goal: modeling of the substrate current

-substrate current is injected by the *pnp*

-lateral *npn* contributes only to the drain current i.e. to the base current of the *pnp*.

-this simplifies modeling and makes it possible to safely omit the *npn* from the subcircuit.

-the actual implementation of the lateral-*npn* device was omitted by taking its effect on the base current into account by a special scaling technique.



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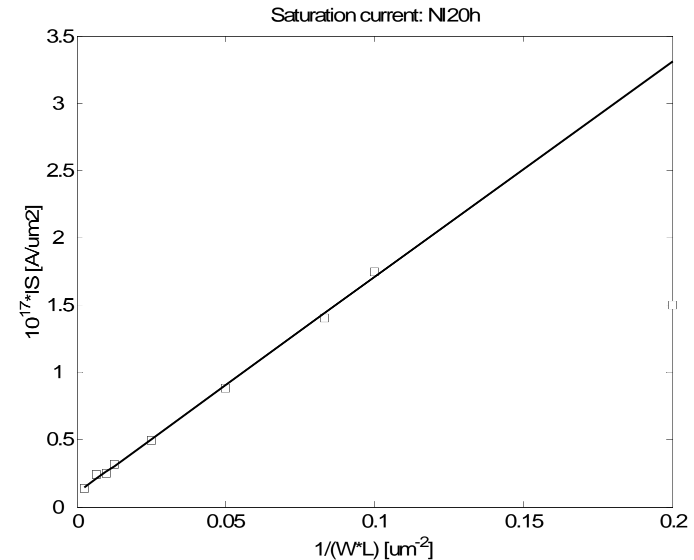
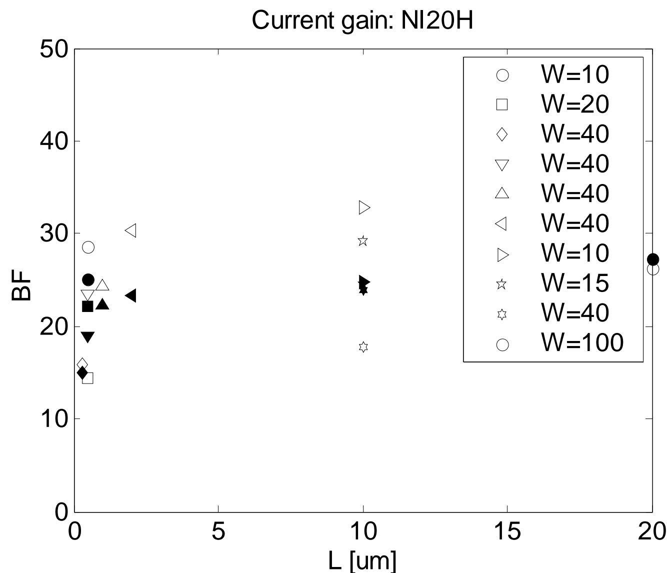
Scaling Results IS , IKF , ISE, BF

- Ideal linear dependence with the inverse *area* for IS, IKF, ISE
- Randomly dependency for BF
  - ibei of the lateral bipolar described with neutral base recombination affected base current

J. Lindmayer and C. Y. Wrigley, „Fundamentals of Semiconductor Devices,“





$$IS = IS_ + ISL_ \cdot \frac{1}{A}$$

$$BF = \frac{IS_ + IS_A \cdot \frac{1}{A}}{ibei_vl + \frac{1}{L^2} \cdot ibei_lat0 + \frac{1}{A} \cdot ibei0 - L^2 \cdot ibei_lat2}$$

$$ibei_lat(L) = \frac{ibei_lat0}{L} \frac{\frac{L}{\lambda}}{\tanh\left(\frac{L}{\lambda}\right)} \approx \frac{ibei_lat0}{L} + L \cdot ibei_lat1 - L^3 \cdot ibei_lat2$$

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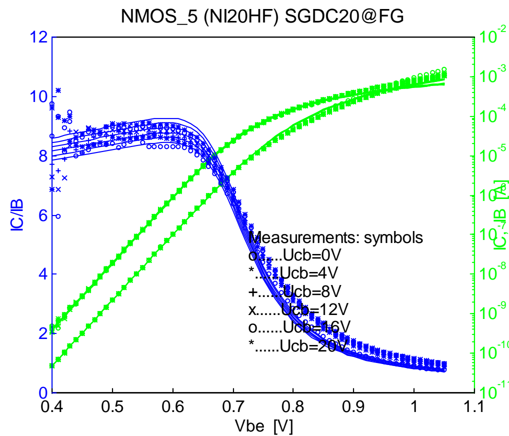
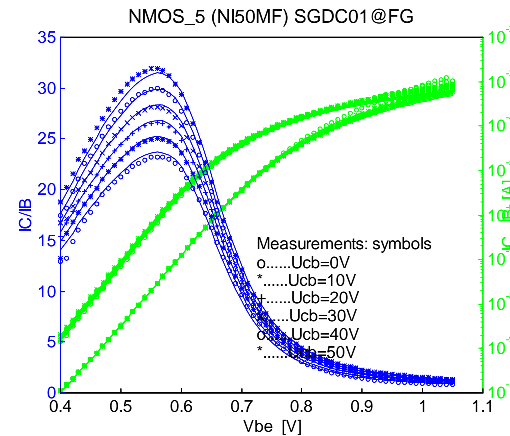
Results of parasitic bipolar models NMOSI20, NMOSI50

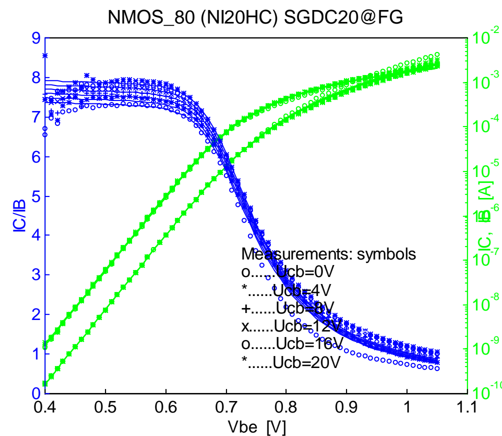
W/L=10/0.5



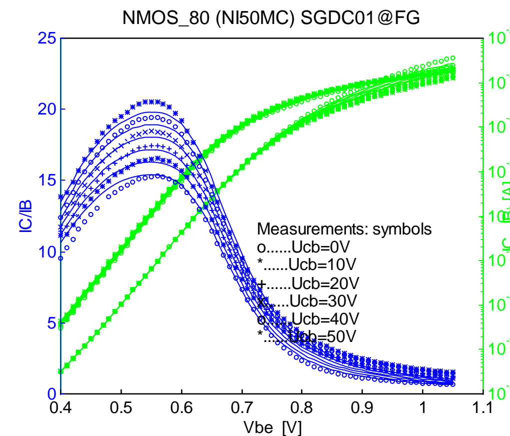
W/L=10/0.5



W/L=40/2



W/L=40/2



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Presentation Overview

- HV LDCMOS transistor modeling
  - DC & AC ✓
  - Modeling of HV LDMOS parasitics ✓
- **Mismatch considerations for HV LDMOS**

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Goal of Mismatch Characterisation

Characterisation and Modelling of HV-MOSFET MISMATCH

- Yield prediction during the design phase
- Improvement of the circuit robustness

NEEDED:

- Proper mismatch model (Voltage and Area dependency)
- Parameter extraction strategy
- Simulator implementation

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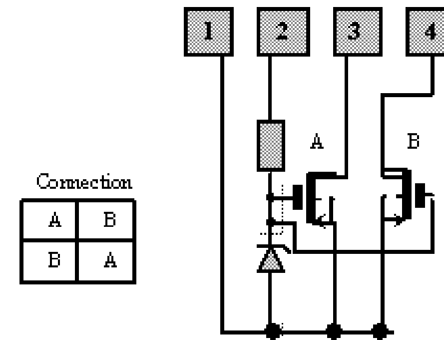
MOS Drain-current Mismatch

Matched transistor pair:

Pair of MOS transistors with identical layout close to each other

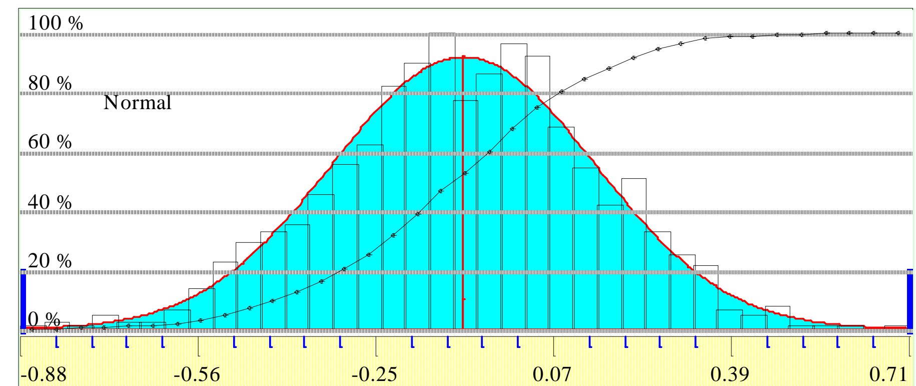


Measurement:

$$\Delta ID / ID = \frac{2 \cdot (ID_1 - ID_2)}{(ID_1 + ID_2)}$$

$$\sigma(\Delta ID / ID) = \sigma\left(\frac{2 \cdot (ID_1 - ID_2)}{(ID_1 + ID_2)}\right)$$

Measured data from production: ID - mismatch [%]



n=997, min= -0.88%, max= 0.7%

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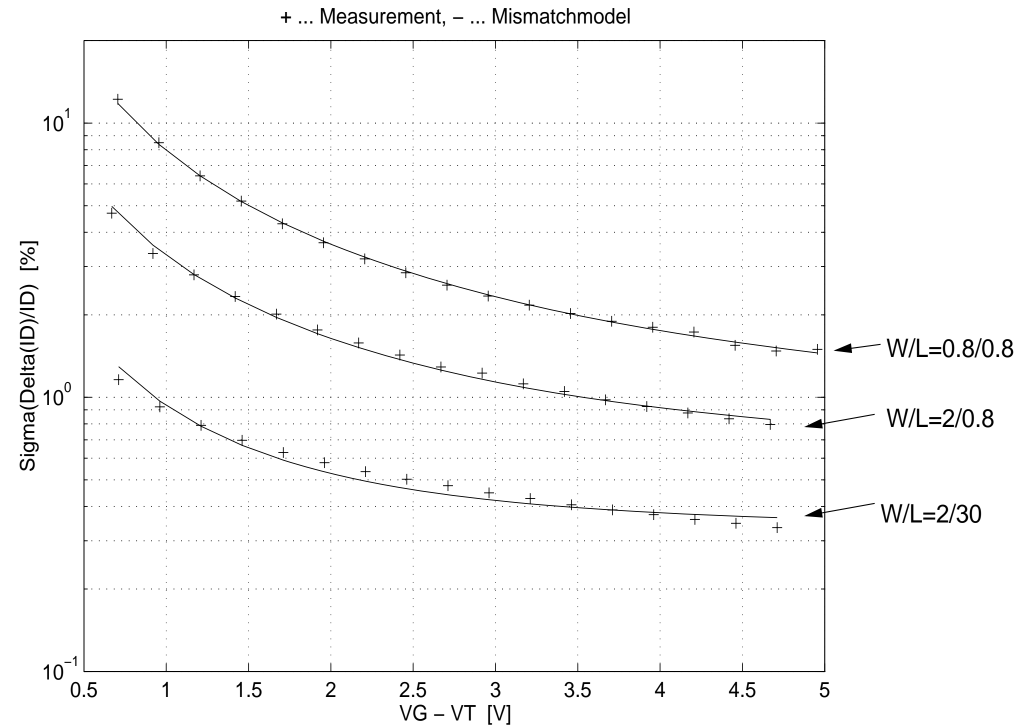
MEASUREMENT DATA

- Measure current ID1 and ID2 for several gate voltages (k=21 points per curve) .
- Several matched pairs of LDNMOS or LDPMOS transistors (m=60 pairs per wafer).
- Calculate relative mismatch

$$\sigma(\Delta ID / ID) = \sigma\left(\frac{2\cdot(ID_1 - ID_2)}{(ID_1 + ID_2)}\right)$$

for any gate voltage.



Measurement Data, Relative ID-Mismatch: +

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Variance Model

Drain current model:

$$I_D = f(P_1, P_2, \ldots, P_n)$$

Sensitivities S_{Pi}

Taylor Expansion:

$$\frac{\Delta I_D}{I_D} = \frac{1}{I_D}\left(\frac{\partial f}{\partial P_1}\right)\Delta P_1 + \frac{1}{I_D}\left(\frac{\partial f}{\partial P_2}\right)\Delta P_2 + \cdots + \frac{1}{I_D}\left(\frac{\partial f}{\partial P_n}\right)\Delta P_n + corr.$$

$$\sigma^2\left(\frac{\Delta I_D}{I_D}\right) = S_{P1}^{\ 2}\,\sigma^2(\Delta P1) + S_{P2}^{\ 2}\sigma^2(\Delta P2) + \cdots \quad + S_{Pn}^{\ 2}\sigma^2(\Delta Pn) \quad + corr$$

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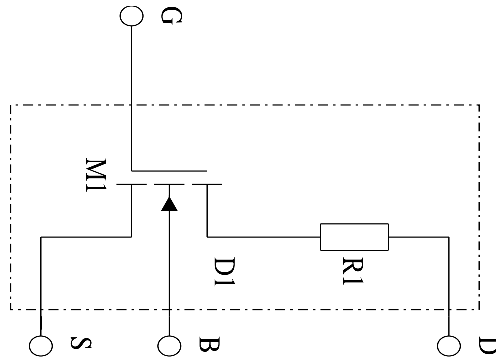
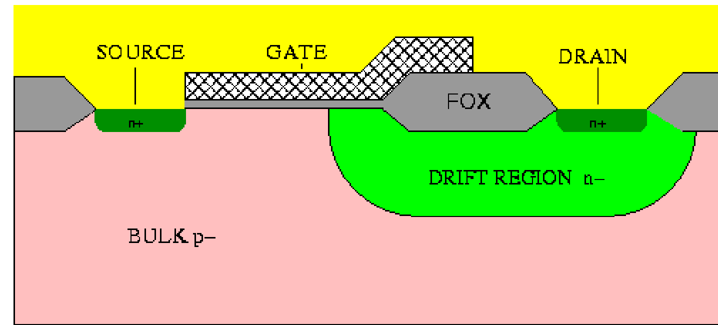
HV-LDMOS Structure & Model





MOS Model + Drain Resistor

Parameters: V_T κ θ R_D

threshold voltage

current gain factor

mobility reduction

drain resistance

$$I_D = \frac{W}{L}\frac{\kappa}{2}\frac{(V_G - V_T)^2}{1+\theta(V_G - V_T)}$$

......Saturation region

$$I_D = \frac{W}{L}\frac{\kappa(V_G - V_T)\cdot VDS}{1+(\theta+\alpha_r)\cdot(V_G - V_T)}, \qquad \alpha_r = \frac{W}{L}\cdot\kappa\cdot R_D$$

......Linear region

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Sensitivities Saturation:

$$\frac{\Delta I_D}{I_D} = f_{sat}(\Delta V_T, \Delta\kappa, \Delta\theta)$$

$$\sigma(\Delta V_T), \quad \sigma(\Delta\kappa), \quad \sigma(\Delta\theta)$$

Extract from measured σ(ΔID)/ID

$$I_D = \frac{W}{L}\frac{\kappa}{2}\frac{(V_G - V_T)^2}{1+\theta(V_G - V_T)} \Rightarrow$$

Taylor Expansion

$$\Delta I_D = \left(\frac{\partial I_D}{\partial V_T}\right)\Delta V_T + \left(\frac{\partial I_D}{\partial \kappa}\right)\Delta\kappa + \left(\frac{\partial I_D}{\partial \theta}\right)\Delta\theta \Rightarrow$$

$$\frac{\Delta I_D}{I_D} = -\left(\frac{2+\theta(V_G - V_T)}{(V_G - V_T)(1+\theta(V_G - V_T))}\right)\Delta V_T + \frac{1}{\kappa}\Delta\kappa - \left(\frac{V_G - V_T}{1+\theta(V_G - V_T)}\right)\Delta\theta$$

Sensitivities

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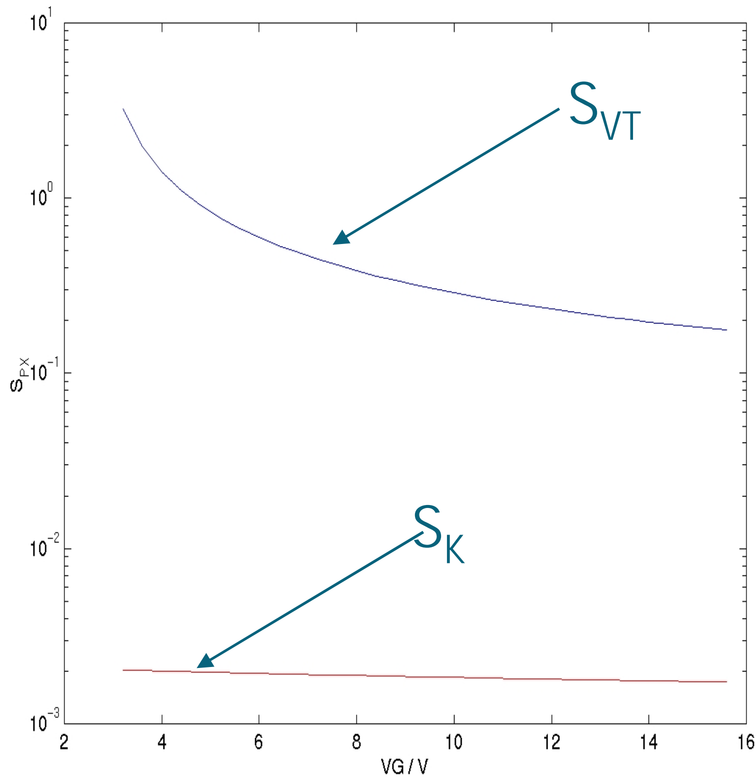
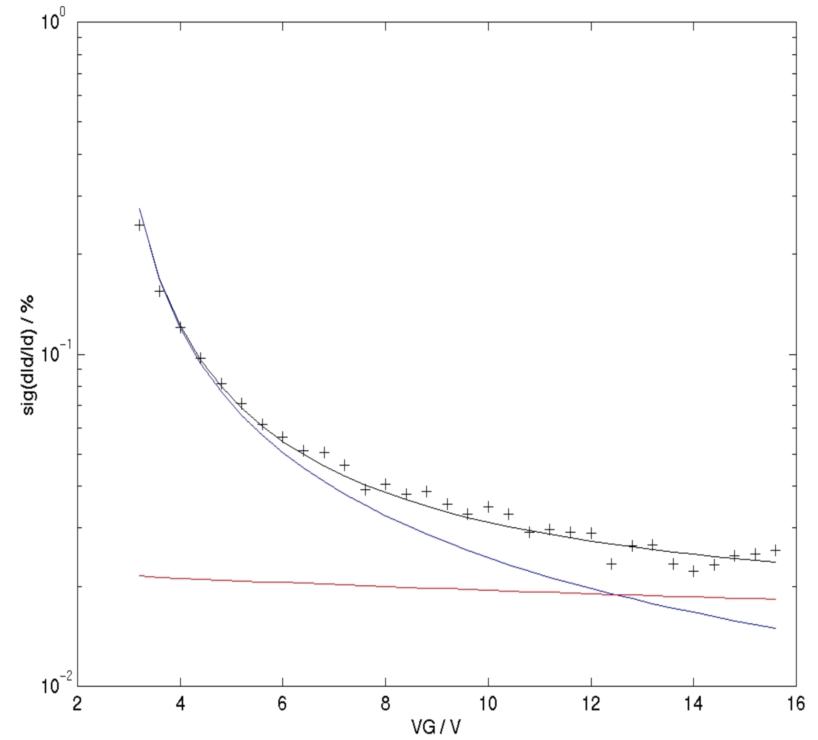
SATURATION





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Sensitivities linear Region:

$$\frac{\Delta I_D}{I_D} = f_{lin}(\Delta V_T, \Delta\kappa, \Delta\theta, \Delta R_D)$$

→ Extract $\sigma(\Delta V_T)$, $\sigma(\Delta R)$ from measured σ(ΔID)/ID

$$I_D = \frac{W}{L}\frac{\kappa(V_G - V_T)\cdot VDS}{1+(\theta+\alpha_r)\cdot(V_G - V_T)}, \qquad \alpha_r = \frac{W}{L}\cdot\kappa\cdot R_D$$

Taylor Expansion 1st oder

$$\Delta I_D = \left(\frac{\partial I_D}{\partial V_T}\right)\Delta V_T + \left(\frac{\partial I_D}{\partial \kappa}\right)\Delta\kappa + \left(\frac{\partial I_D}{\partial \theta}\right)\Delta\theta + \left(\frac{\partial I_D}{\partial R_D}\right)\Delta R_D \Rightarrow$$

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Sensitivities linear Region:

$$\frac{\Delta I_D}{I_D} = -\left(\frac{1}{(V_G - V_T)(1 + (\theta + \alpha_r)(V_G - V_T))}\right)\Delta V_T - \left(\frac{V_G - V_T}{1 + (\theta + \alpha_r)(V_G - V_T)}\right)\Delta\theta$$

Sensitivities

$$+\left(\frac{1 + \theta(V_G - V_T)}{\kappa(1 + (\theta + \alpha_r)(V_G - V_T))}\right)\Delta\kappa - \left(\frac{W}{L}\frac{\kappa(V_G - V_T)}{1 + (\theta + \alpha_r)(V_G - V_T)}\right)\cdot\Delta R_D$$

$$-\frac{I_D}{VDS}$$

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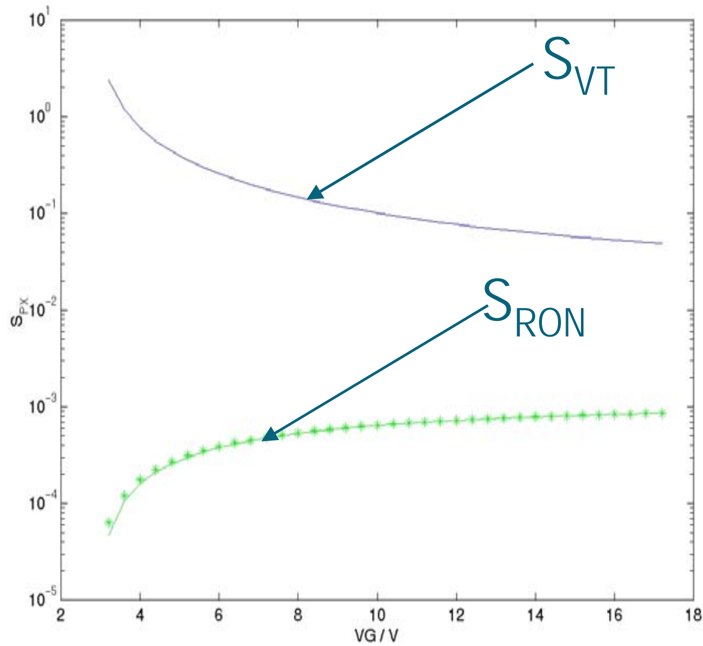
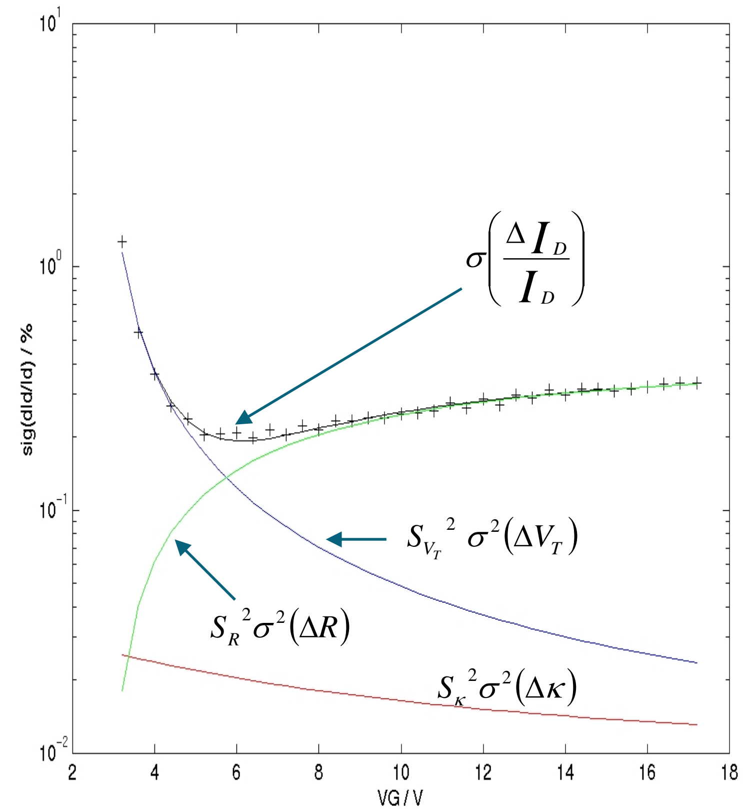
LINEAR REGION





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Extraction of mismatch parameters

$$\sigma^2\left(\frac{\Delta I_D}{I_D}\right) = S_{V_T}{}^2\,\sigma^2(\Delta V_T) + S_\kappa{}^2\sigma^2(\Delta\kappa) + S_\theta{}^2\sigma^2(\Delta\theta) + S_R{}^2\sigma^2(\Delta R)$$

1. Step: Saturation:

Extract $\sigma(\Delta V_T)$, $\sigma(\Delta\kappa)$, $\sigma(\Delta\theta)$ from measured σ(ΔID)/ID

2. Step: Linear region:

Extract $\sigma(\Delta V_T)$, $\sigma(\Delta R)$ from measured σ(ΔID)/ID

$\boldsymbol{\sigma^2(\Delta V_T)}$: *threshold mismatch parameter*

$\dfrac{\boldsymbol{\sigma^2(\Delta\kappa)}}{\boldsymbol{\kappa^2}}$: *gain mismatch parameter*

$\boldsymbol{\sigma^2(\Delta\theta)}$: *mobility reduction mismatch parameter*

$\boldsymbol{\sigma^2(\Delta R_D)}$: *drain resistor mismatch parameter*

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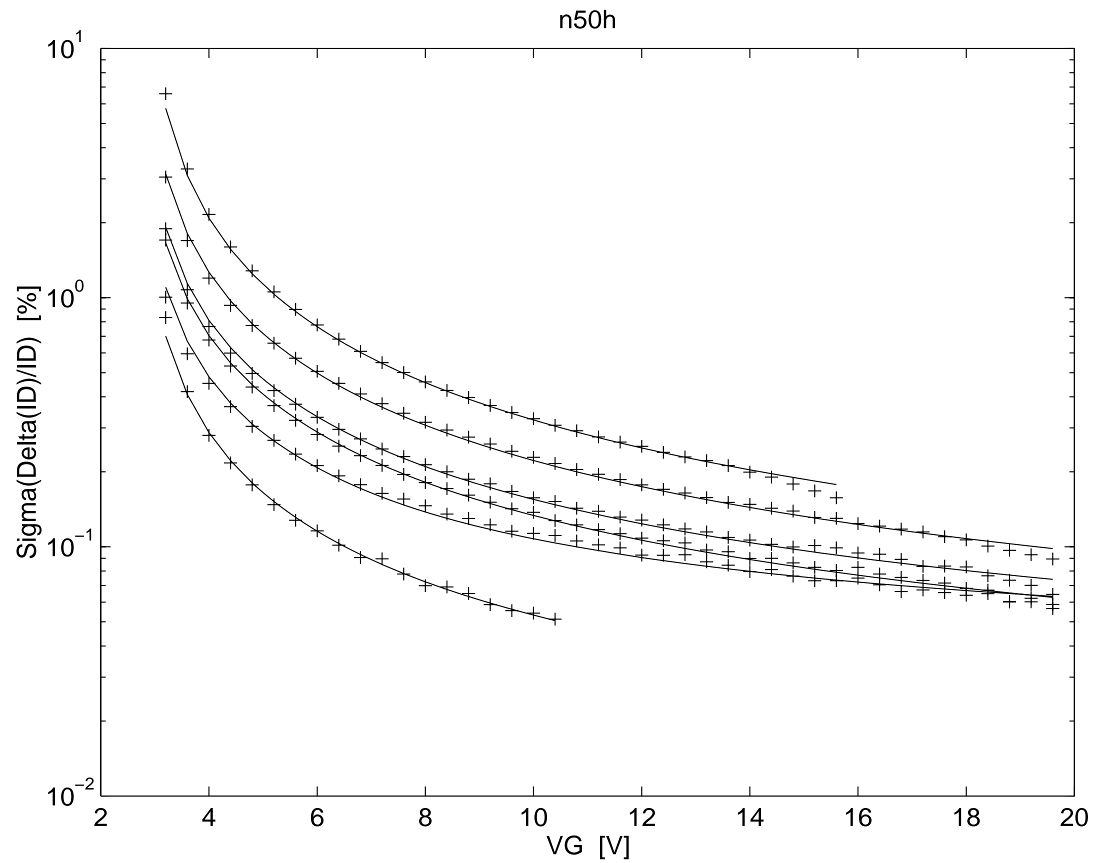
RESULT: Saturation Region



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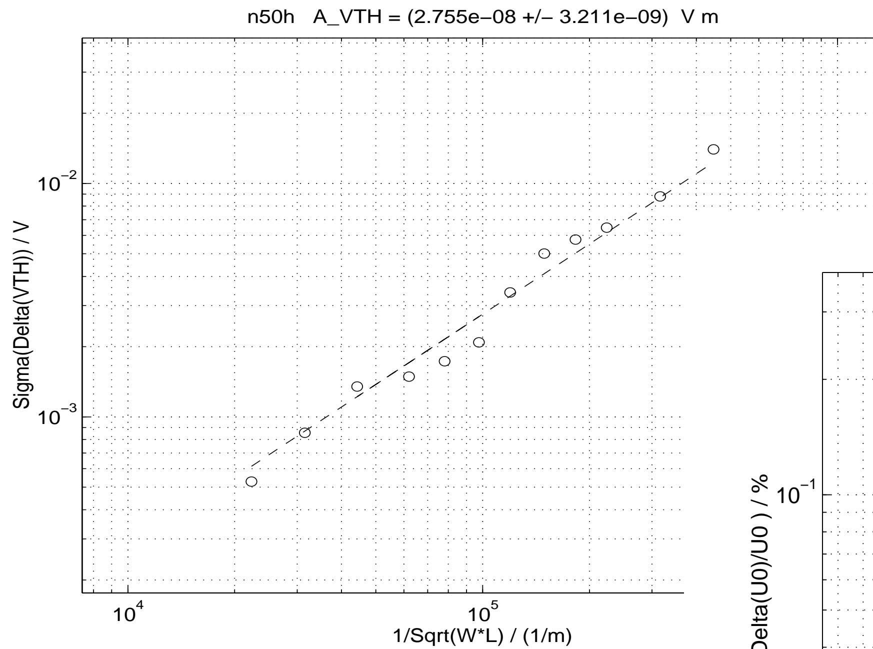
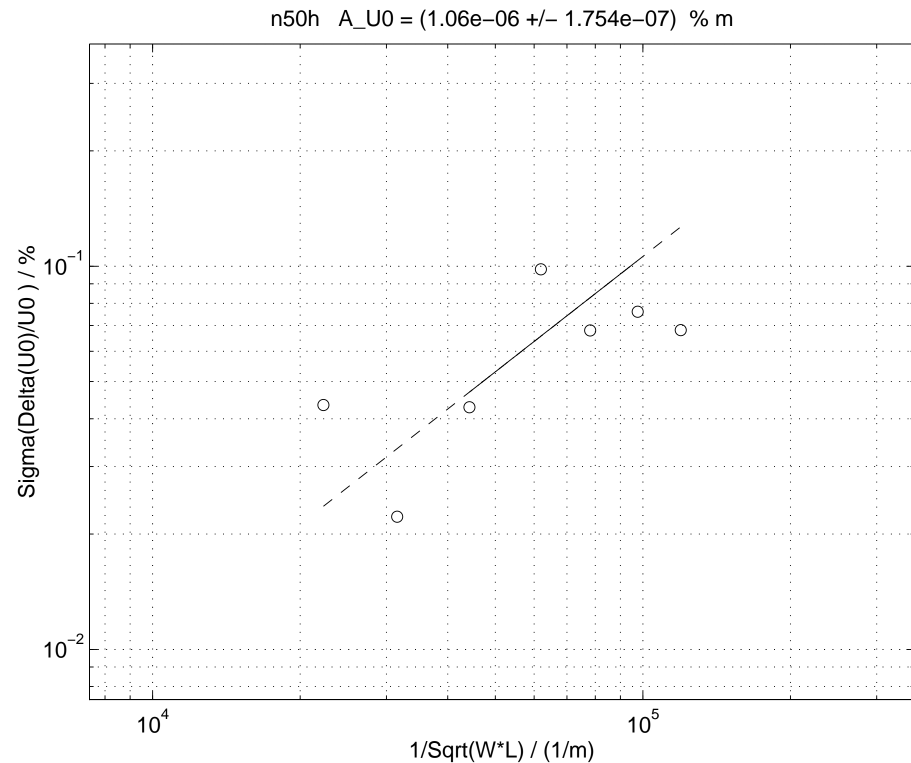
RESULT: Saturation Region





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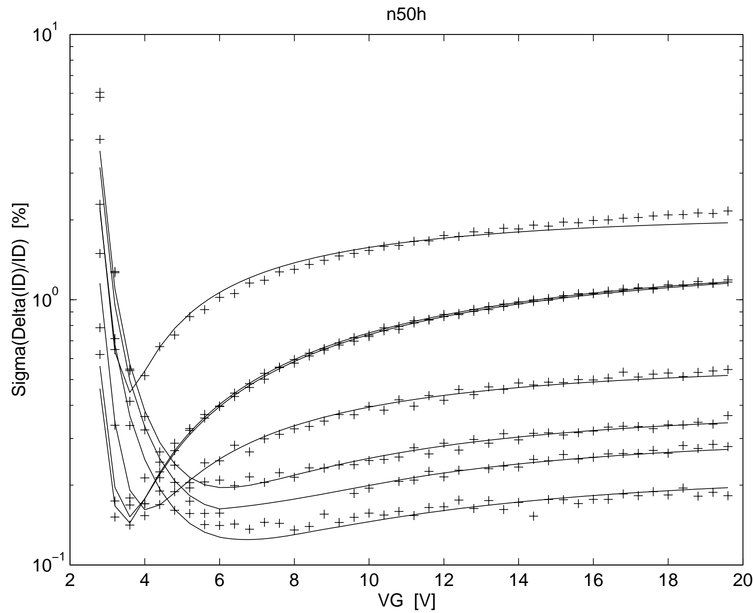
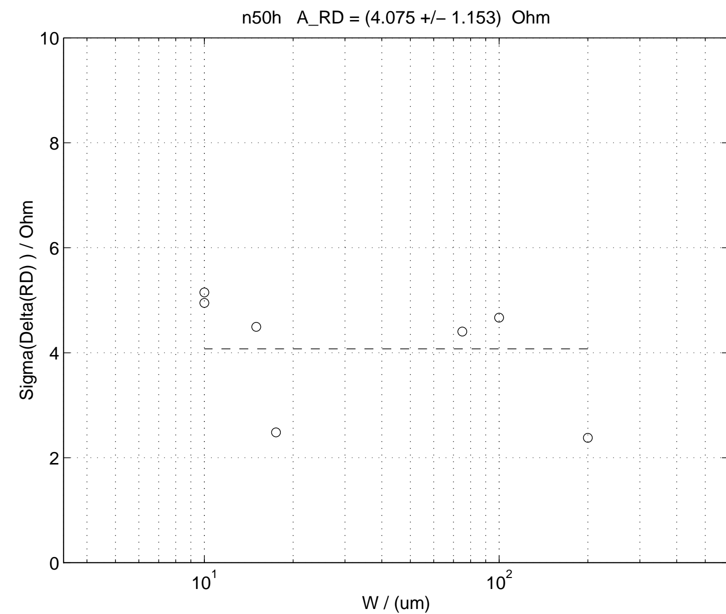
RESULT: Linear Region





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Summary

Presentation of a HV LDMOS transistors sub-circuit model

- DC/AC modeling for W & L scalable devices
- Scalable modeling of the parasitic diodes and bipolar transistors
- Mismatch parameter discussion for LDMOS transistors

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