High-Voltage LDMOS compact modelling

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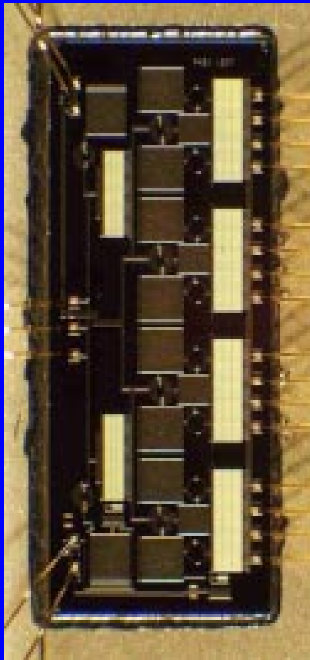
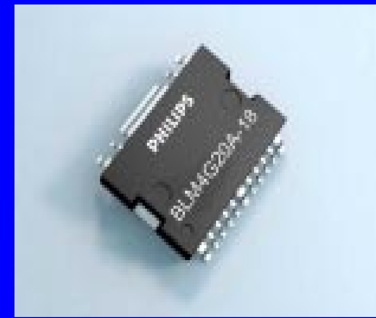
RF-LDMOS applications

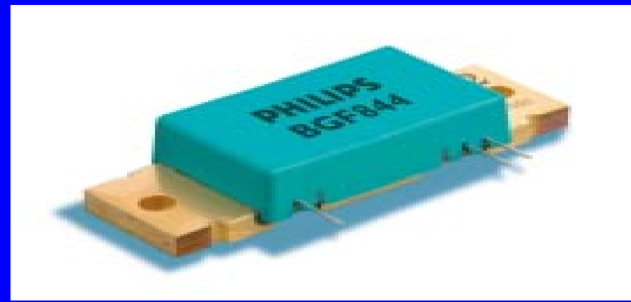




base stations

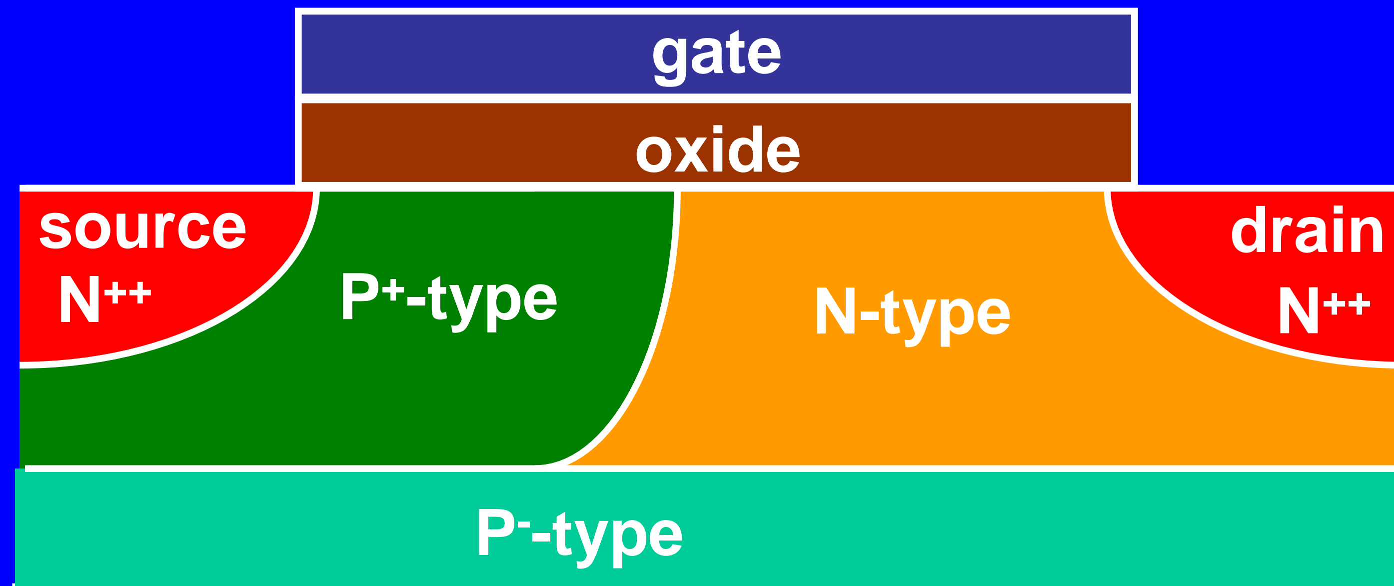
MMIC design

……



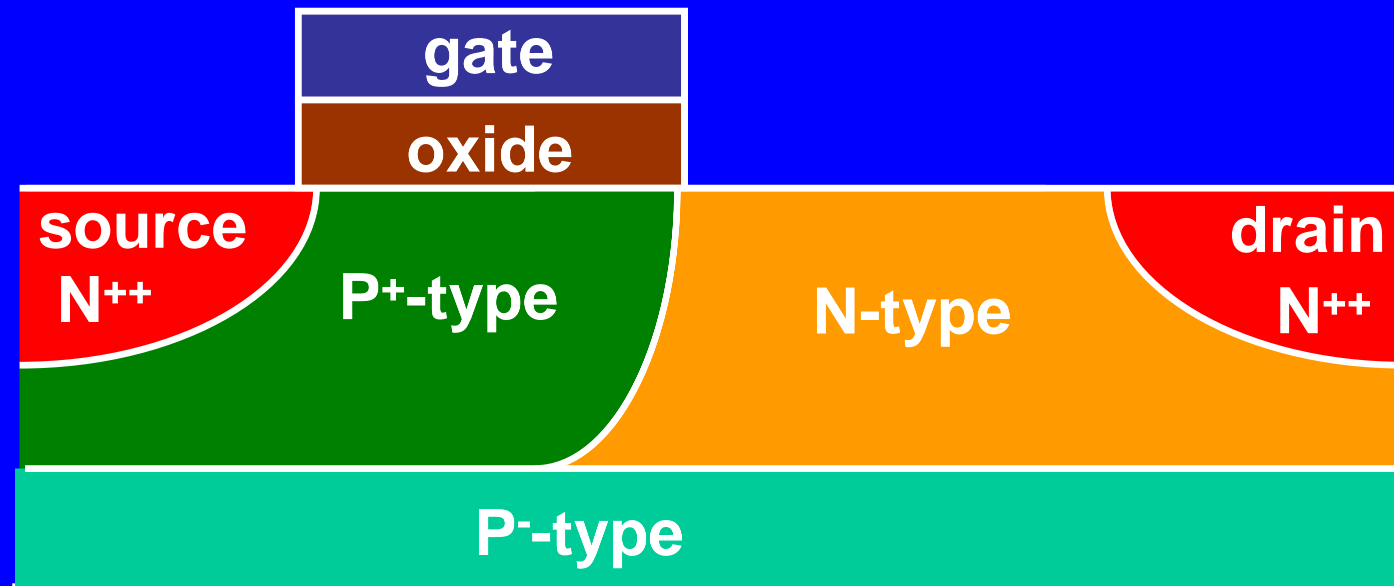
high-voltage LDMOS structures

- low on-resistance
- high capacitances

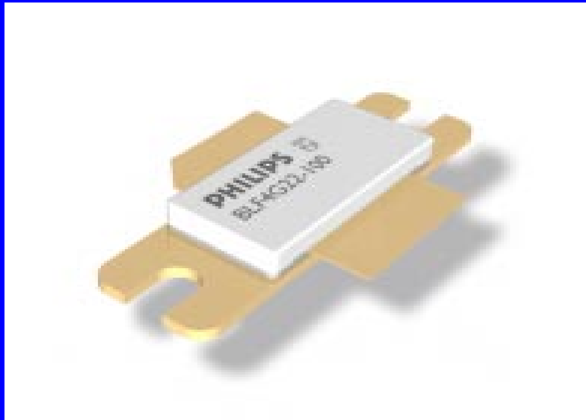


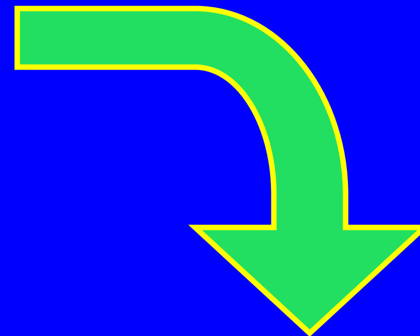
high-voltage LDMOS structures

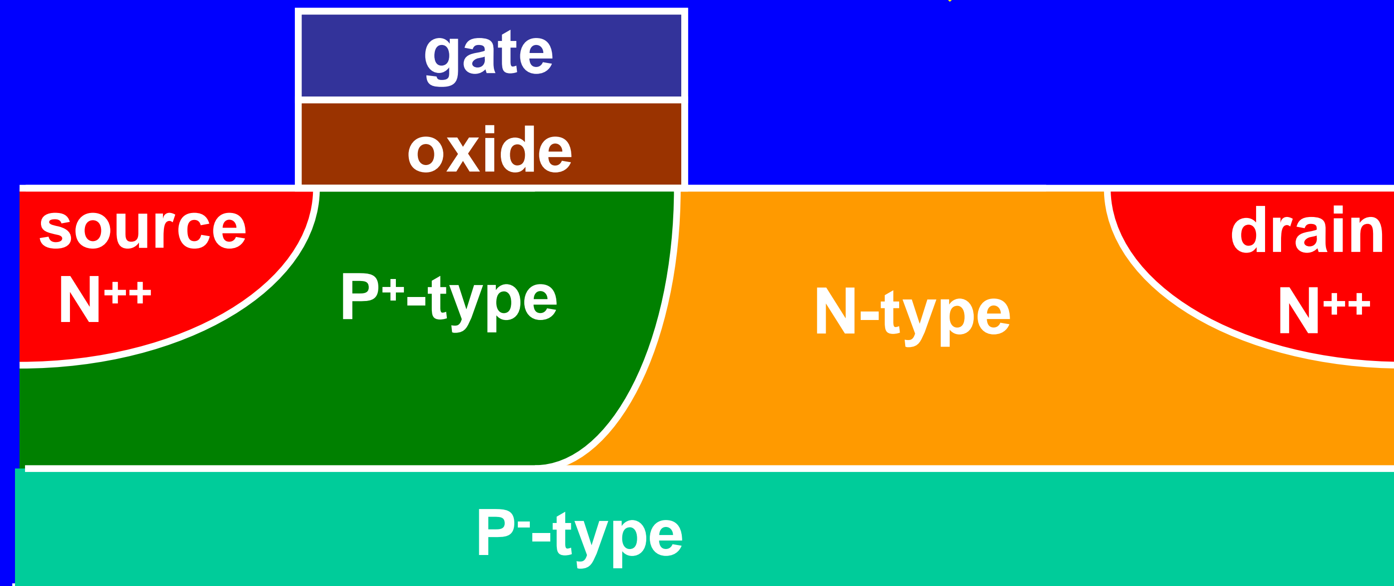
- higher on-resistance
- low capacitances



high-voltage RF LDMOS structure







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- missing phenomena in drift region models
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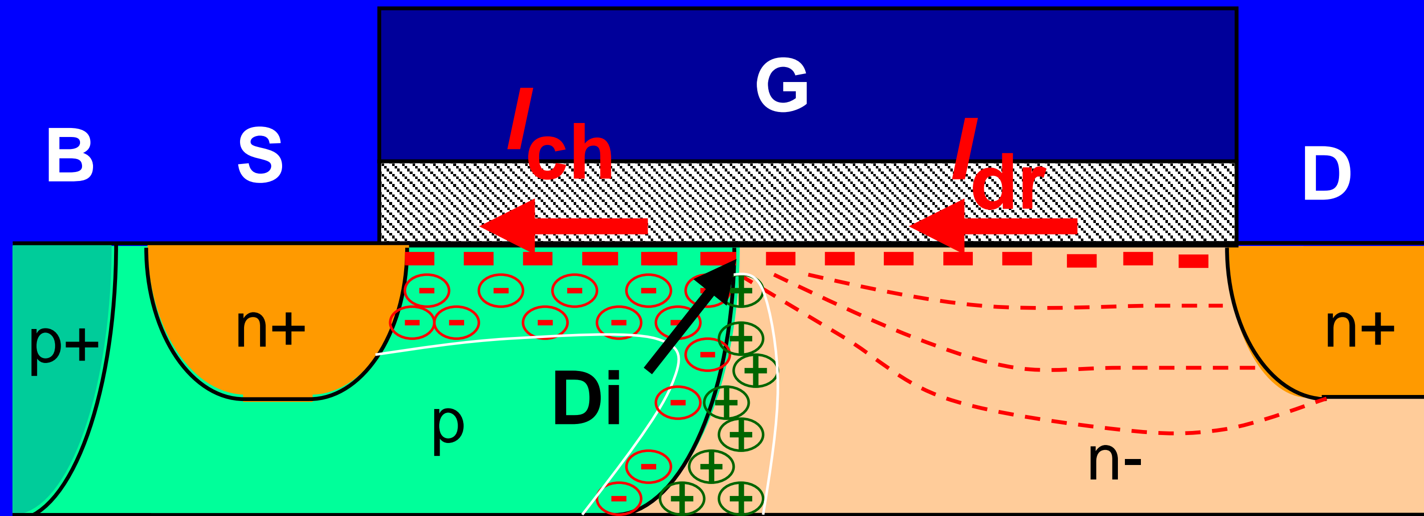
existing compact models

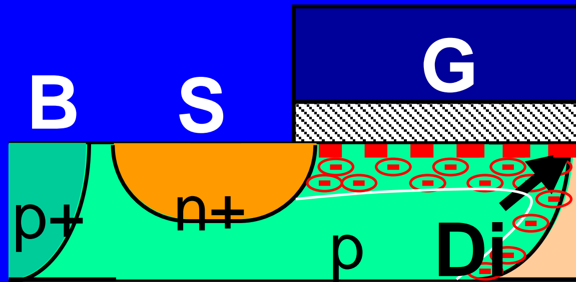


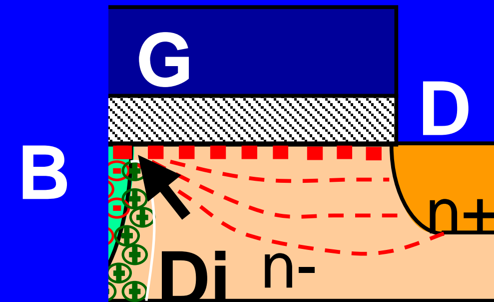
MOS Model 20

website

http://www.semiconductors.philips.com/Philips_Models

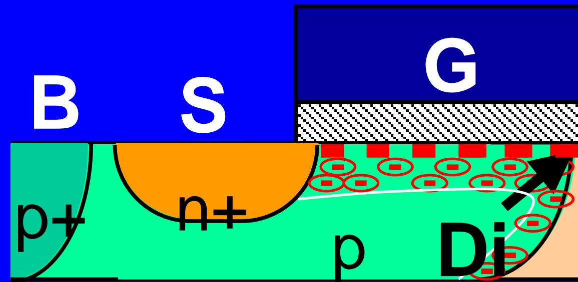
existing compact models: MM20



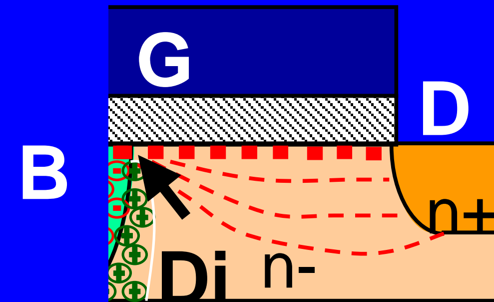


- surface-potential-based (MM11)
- mobility reduction due
  to vertical field (MM9)
- velocity saturation (MM9)
- channel length
  modulation (MM11)
- DIBL (MM11)
- static feedback (MM11)

existing compact models: MM20



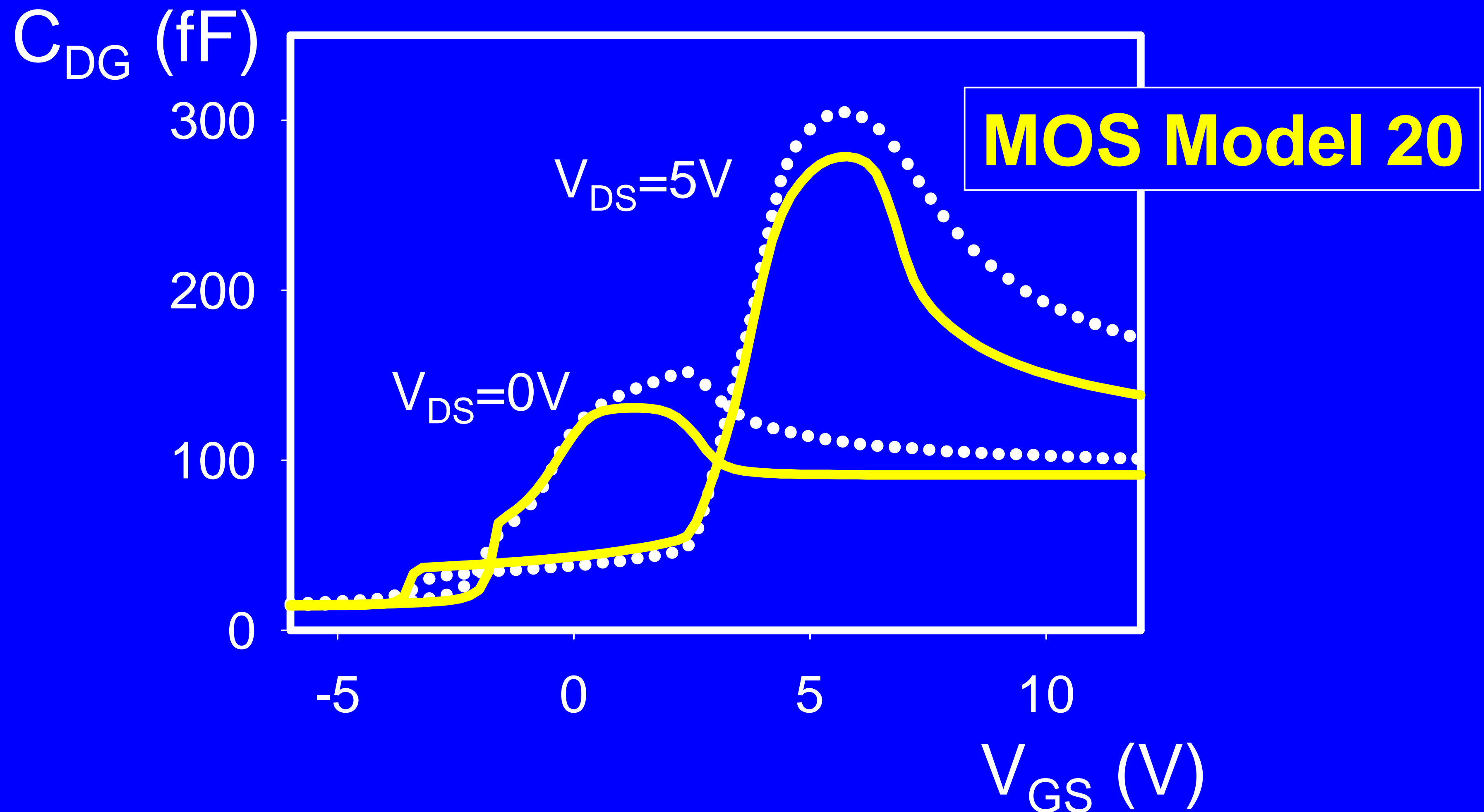
- surface-potential-based (MM11)
- mobility reduction due to vertical field (MM9)
- velocity saturation (MM9)
- channel length modulation (MM11)
- DIBL (MM11)
- static feedback (MM11)



- accumulation
- depletion
- bulk current
- mobility reduction due to vertical field
- velocity saturation

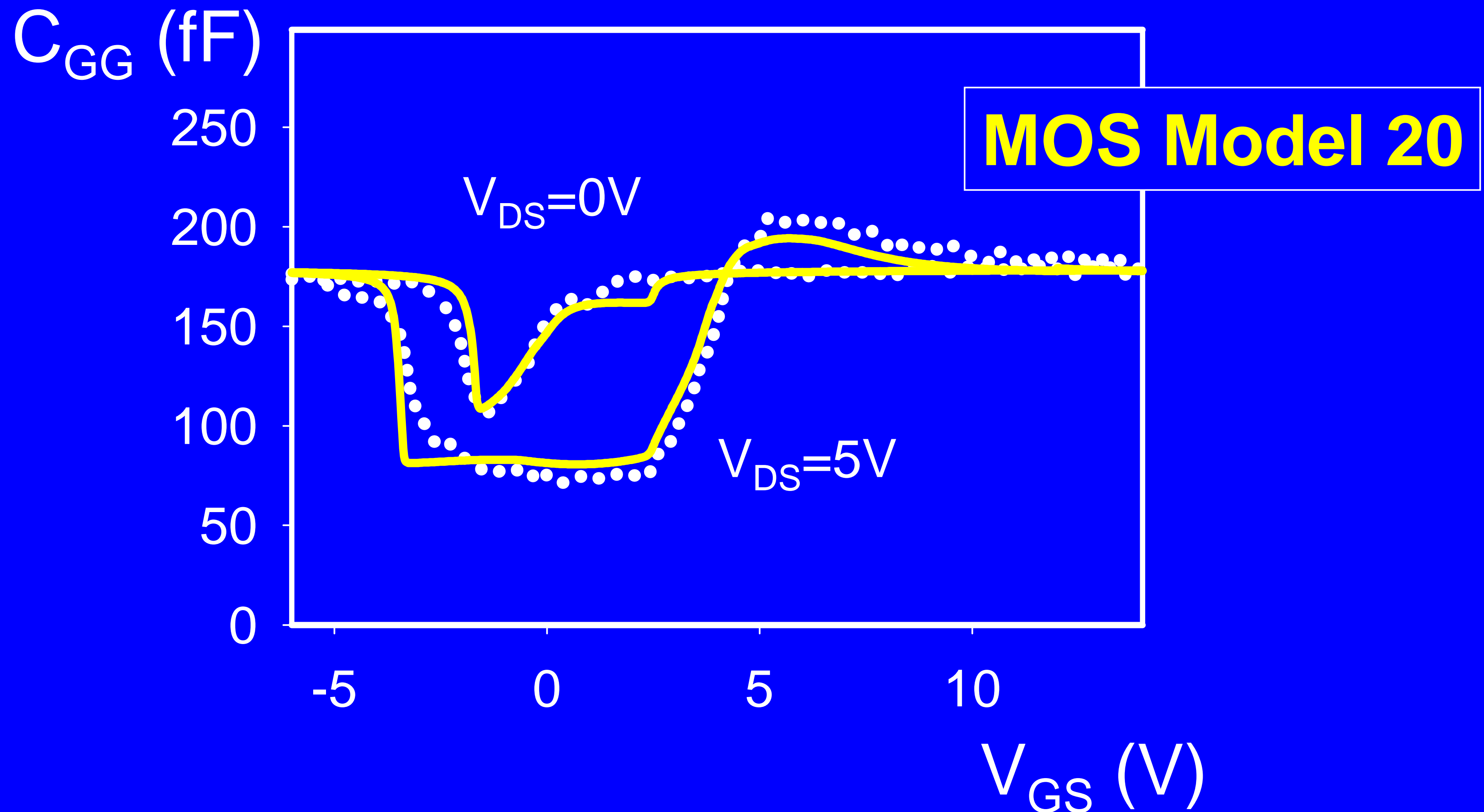
existing compact models

12V SOI-LDMOS: T_{ox}= 38nm, W = 17µm, L = 1.6µm, T = 25°C



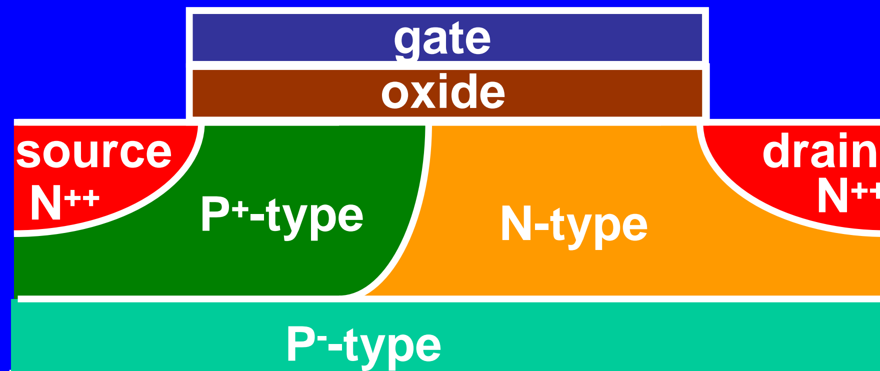
existing compact models

12V SOI-LDMOS: T_{ox}= 38nm, W = 17μm, L = 1.6μm, T = 25°C

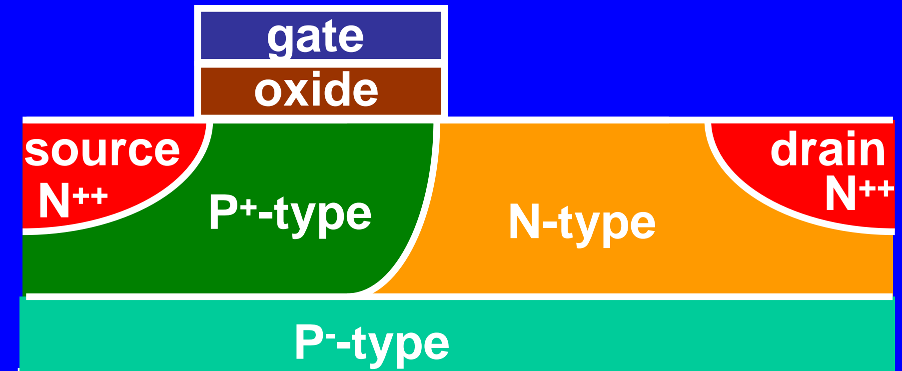


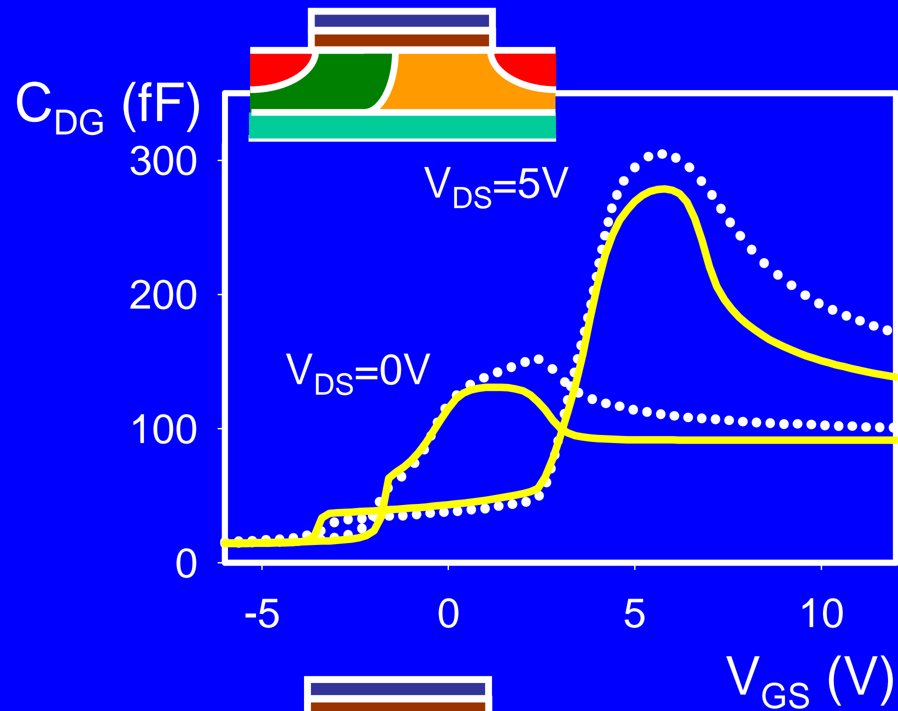
existing compact models

MOS Model 20

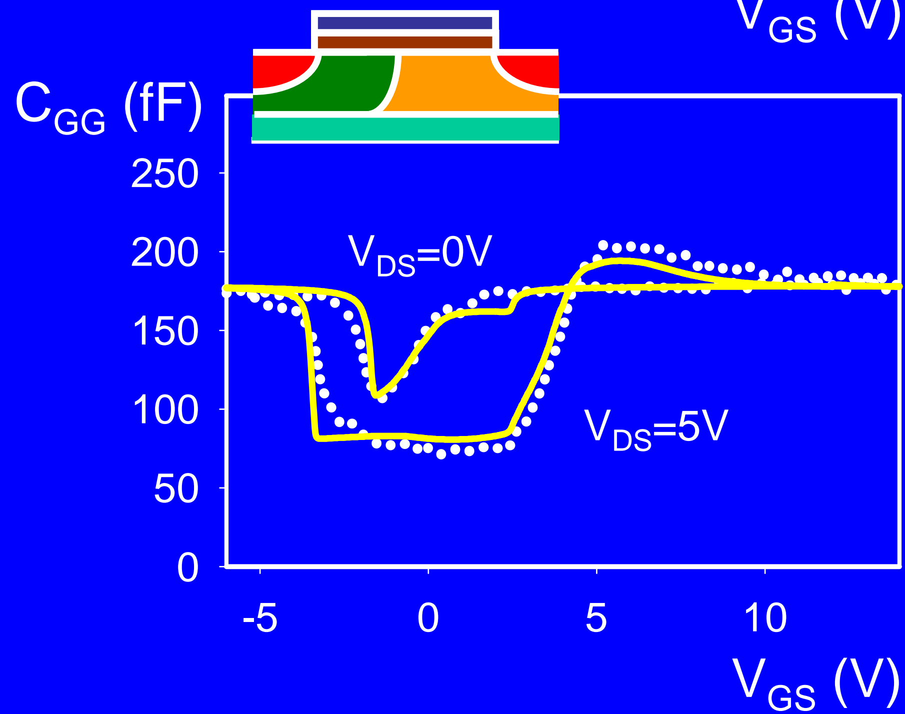


RF-LDMOS

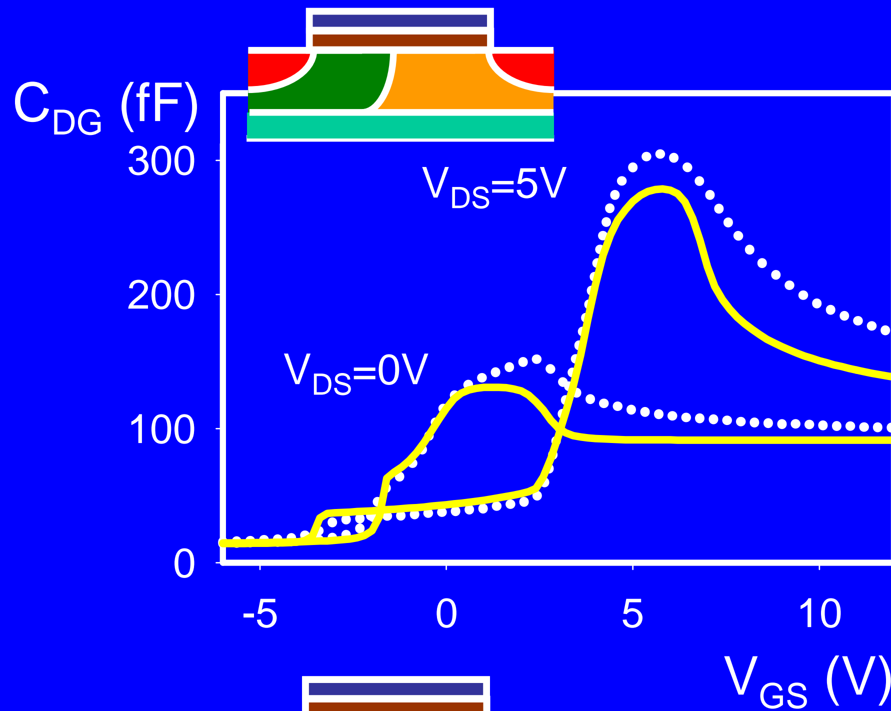




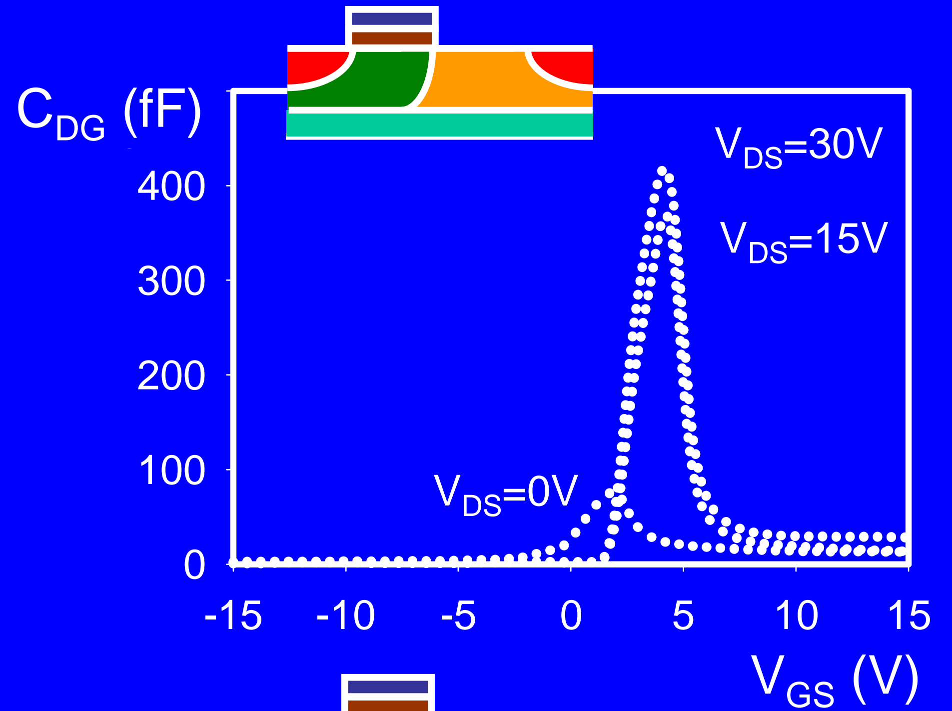
C_{DG} (fF)
300
200
100
0
V_{DS}=5V
V_{DS}=0V
-5
0
5
10
V_{GS} (V)



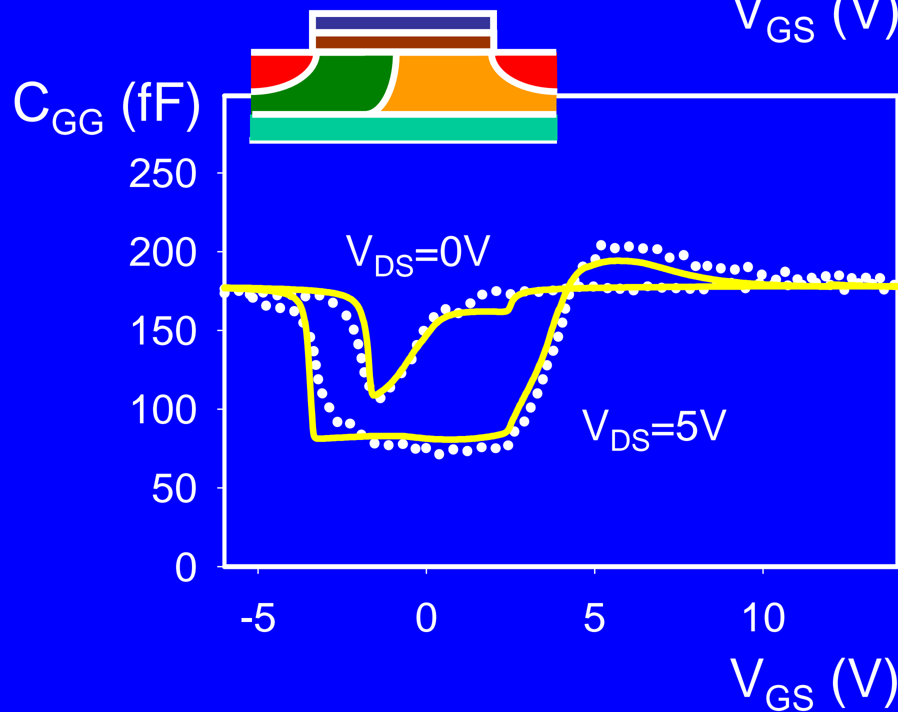
C_{GG} (fF)
250
200
150
100
50
0
V_{DS}=0V
V_{DS}=5V
-5
0
5
10
V_{GS} (V)



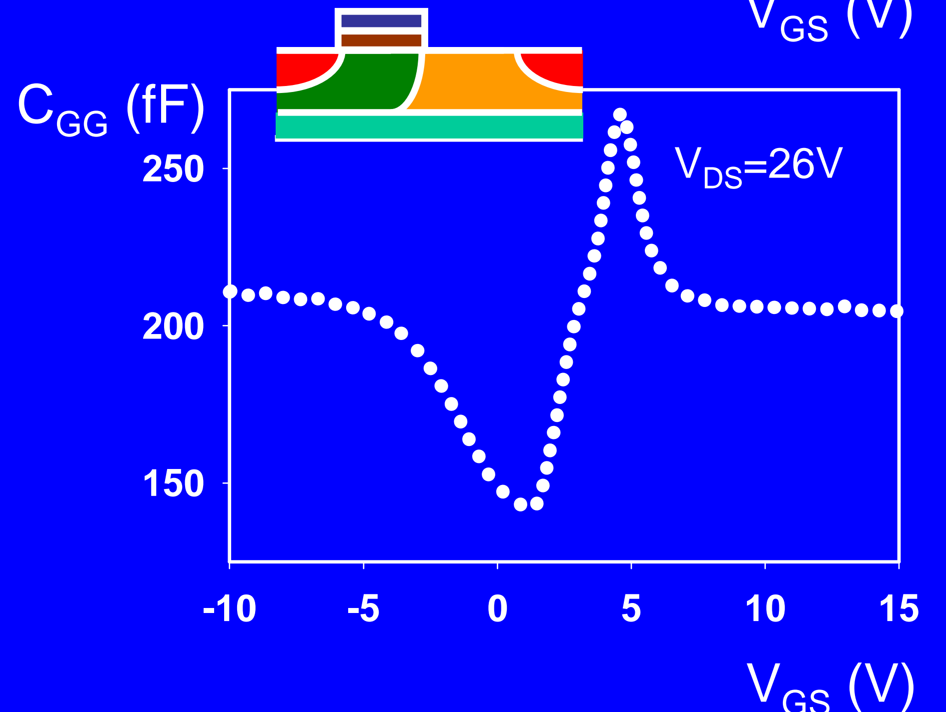
C_{DG} (fF)
300
200
100
0
V_{DS}=5V
V_{DS}=0V
-5
0
5
10
V_{GS} (V)



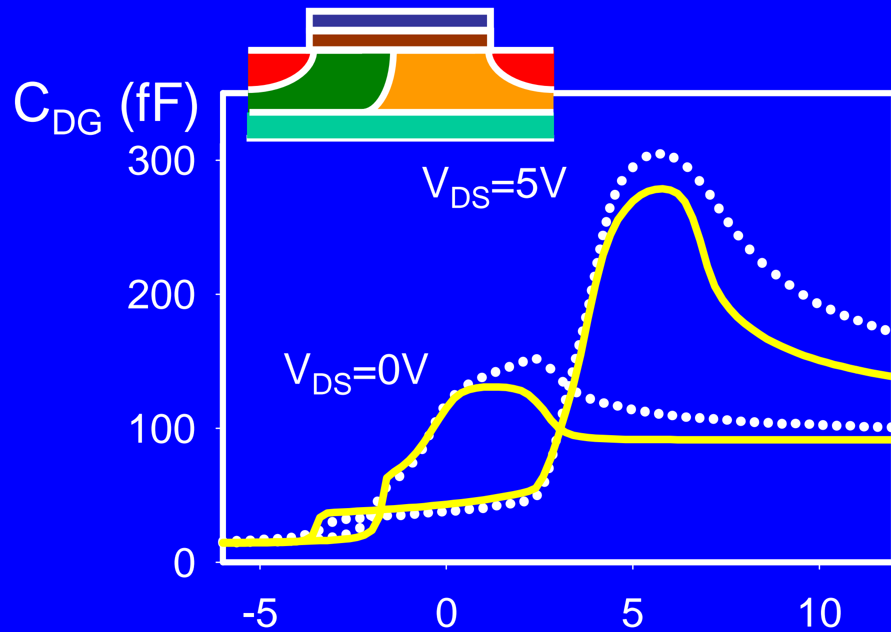
C_{DG} (fF)
400
300
200
100
0
V_{DS}=30V
V_{DS}=15V
V_{DS}=0V
-15
-10
-5
0
5
10
15
V_{GS} (V)

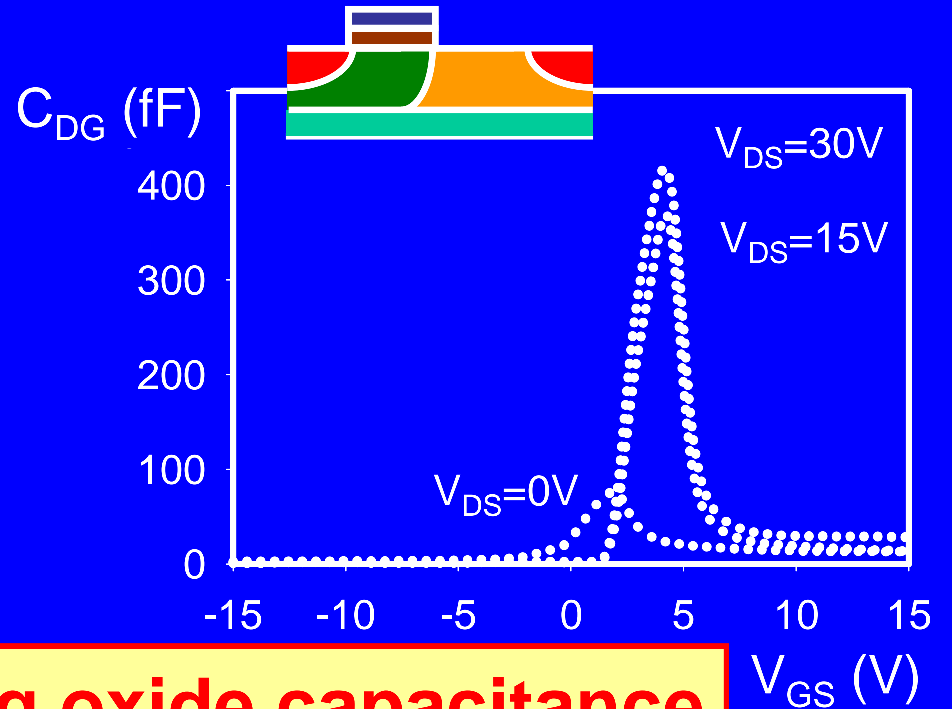


C_{GG} (fF)
250
200
150
100
50
0
V_{DS}=0V
V_{DS}=5V
-5
0
5
10
V_{GS} (V)

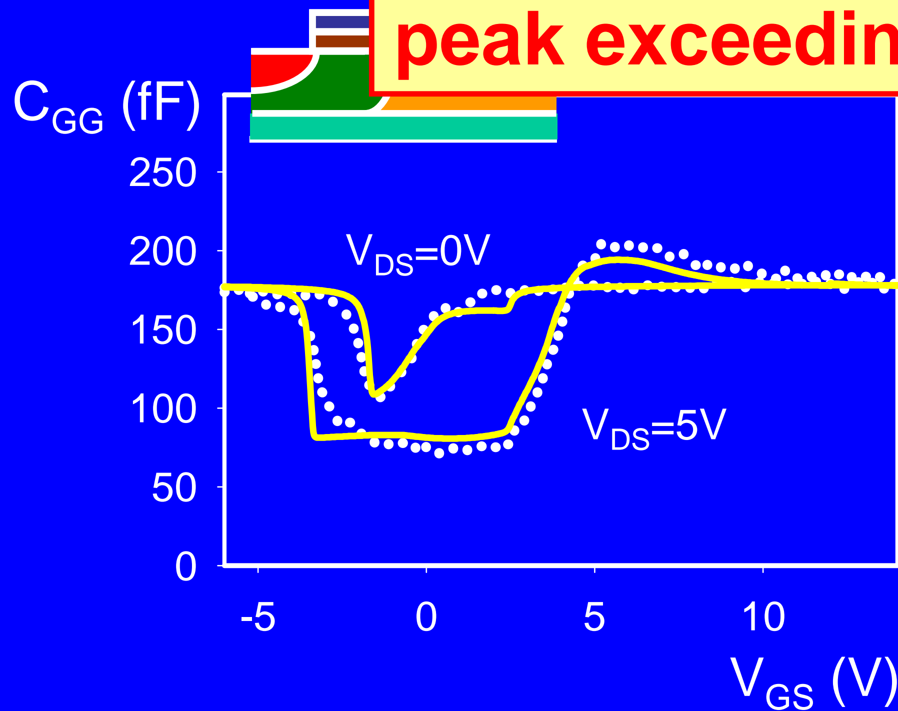


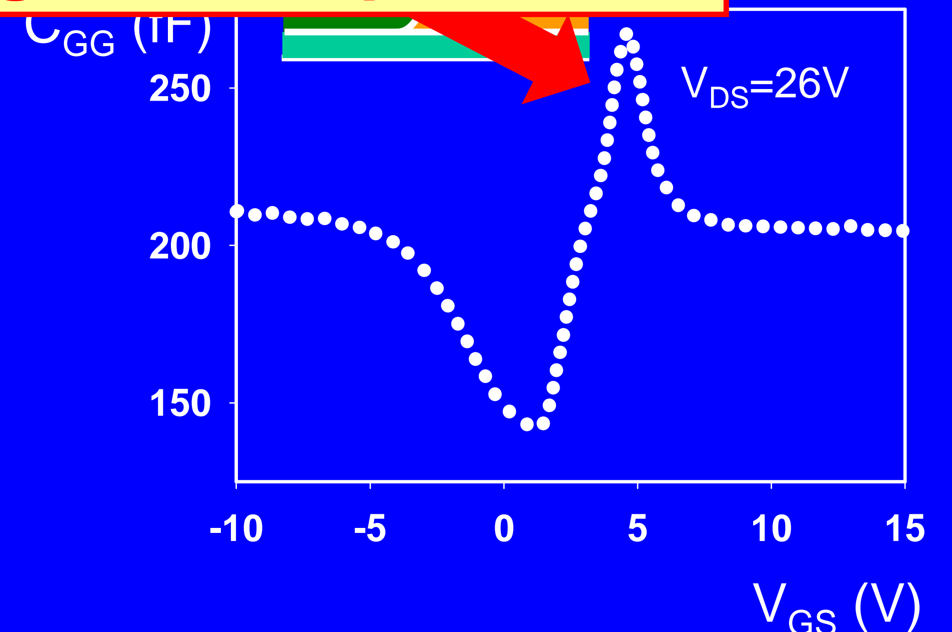
C_{GG} (fF)
250
200
150
V_{DS}=26V
-10
-5
0
5
10
15
V_{GS} (V)

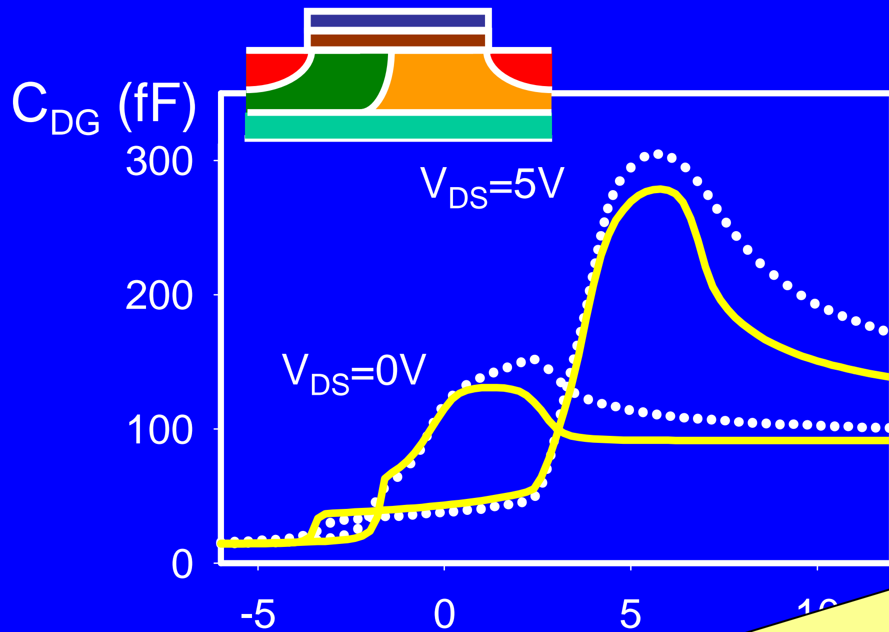


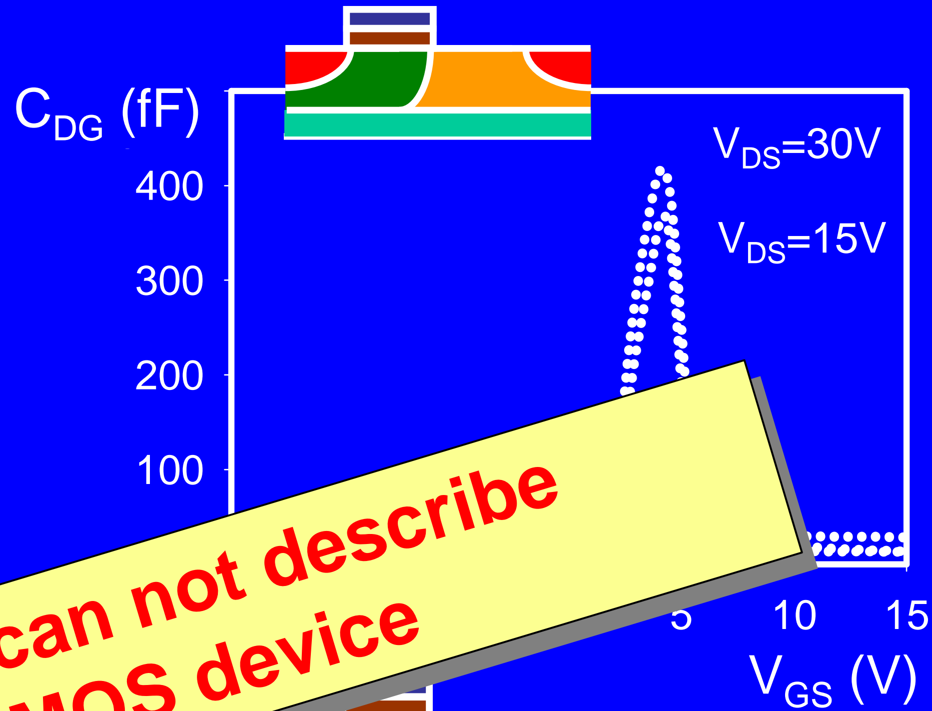


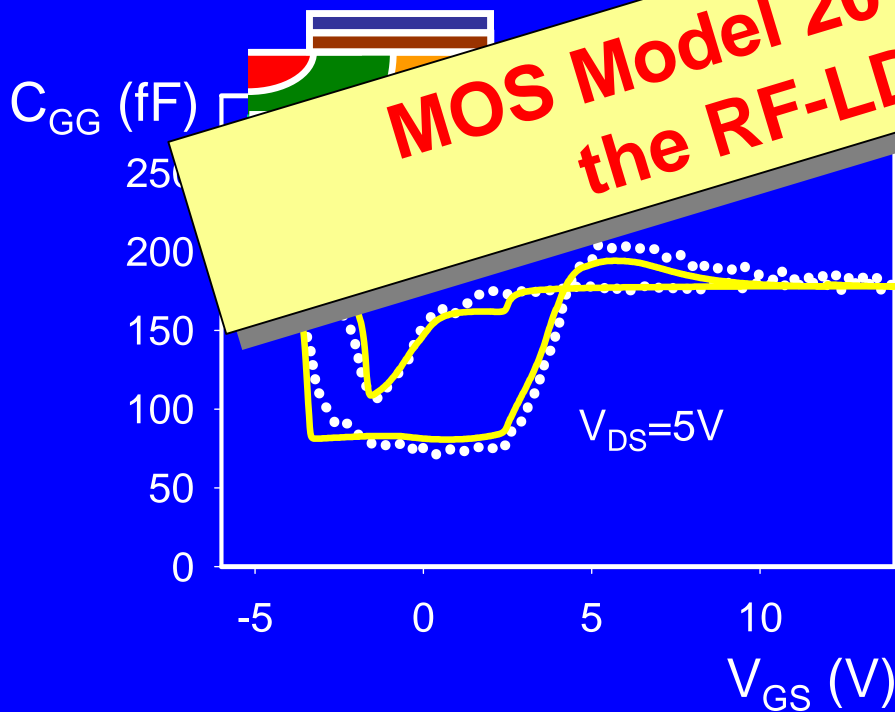
peak exceeding oxide capacitance

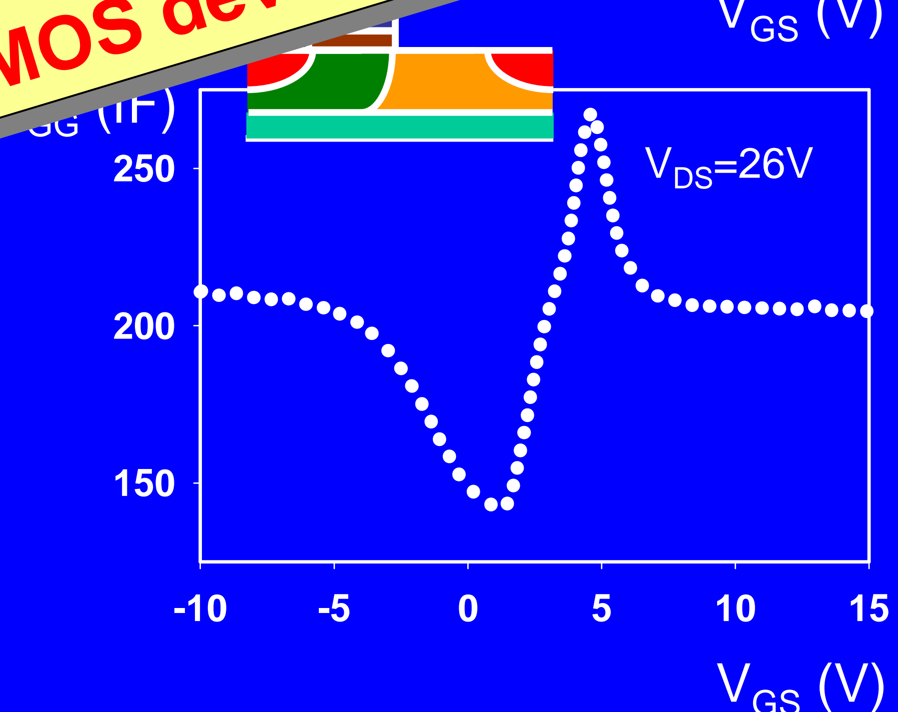






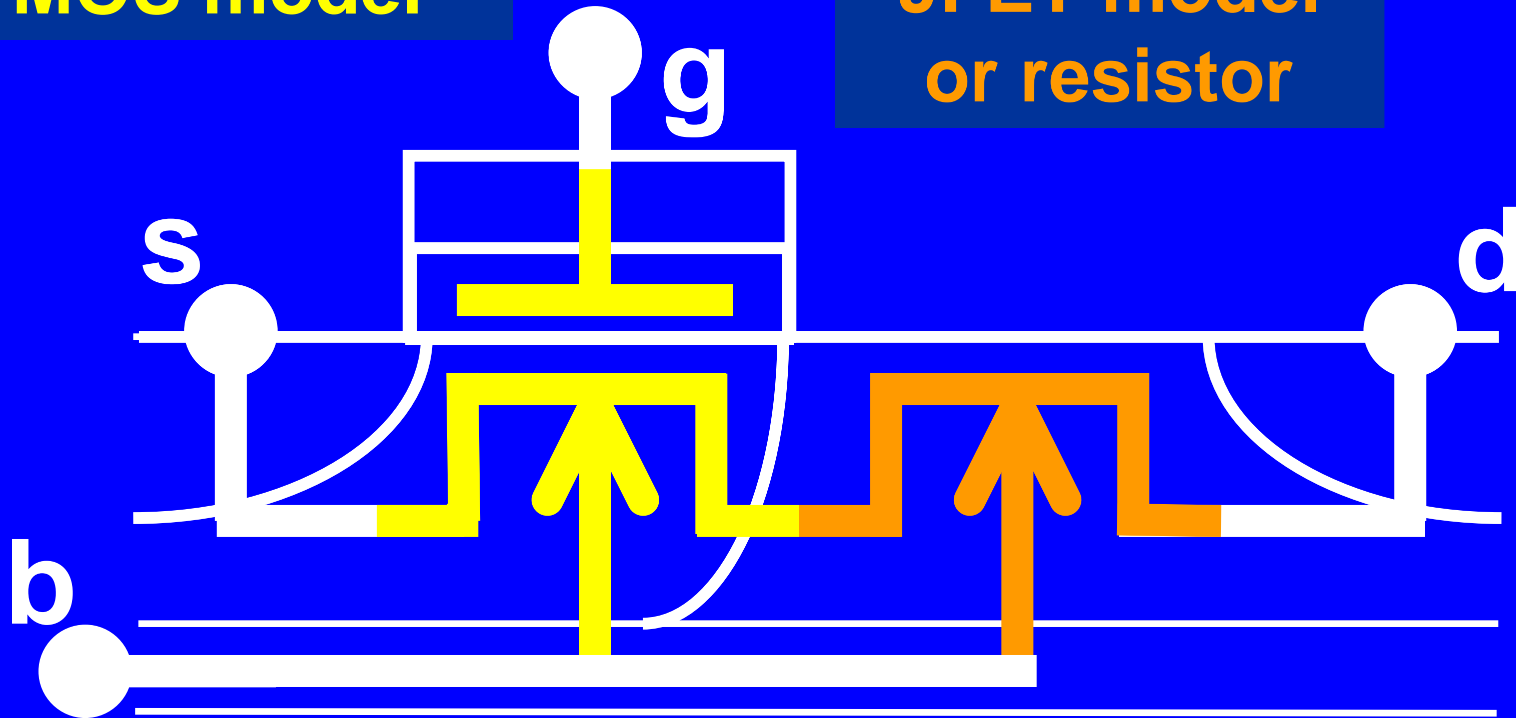




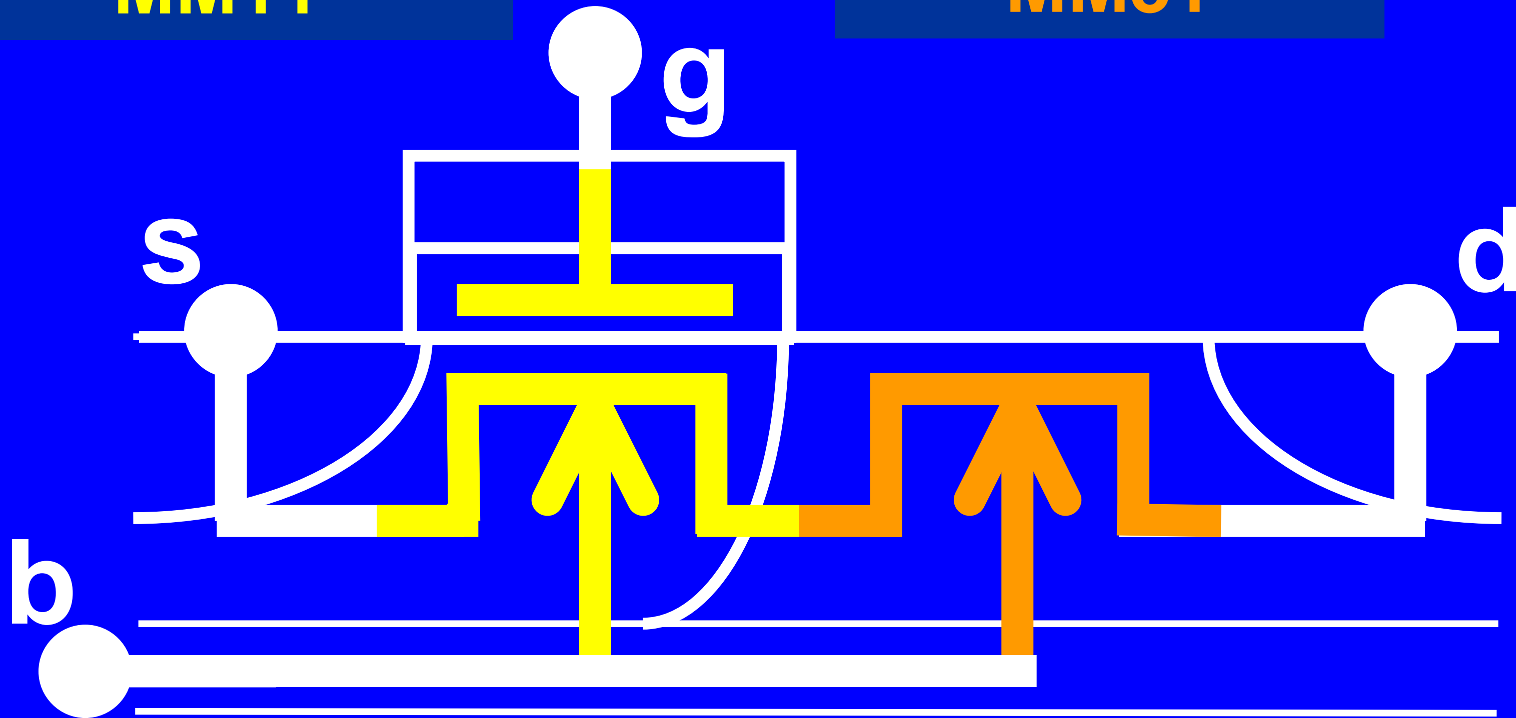


MOS Model 20 can not describe the RF-LDMOS device

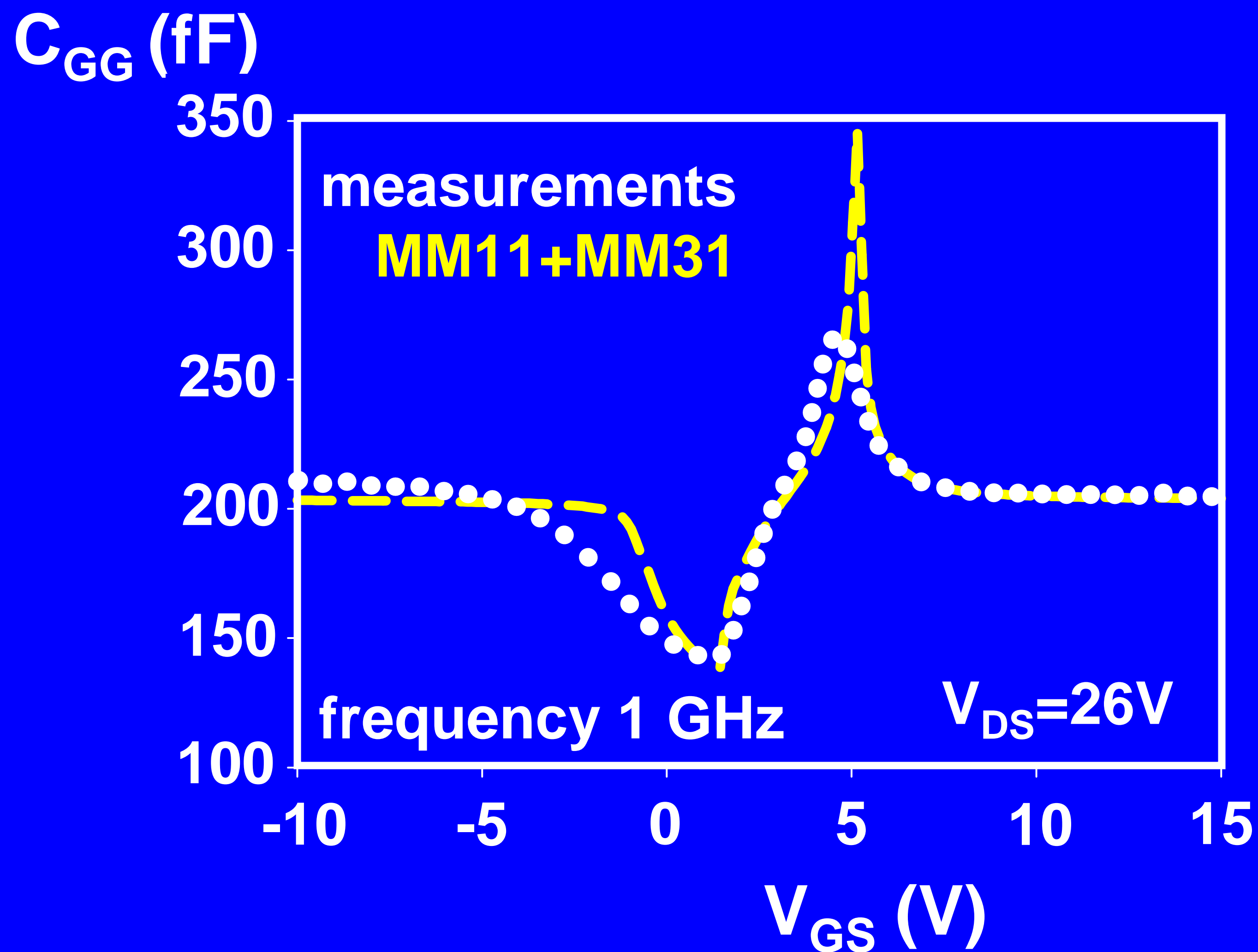
conventional sub-circuit approach



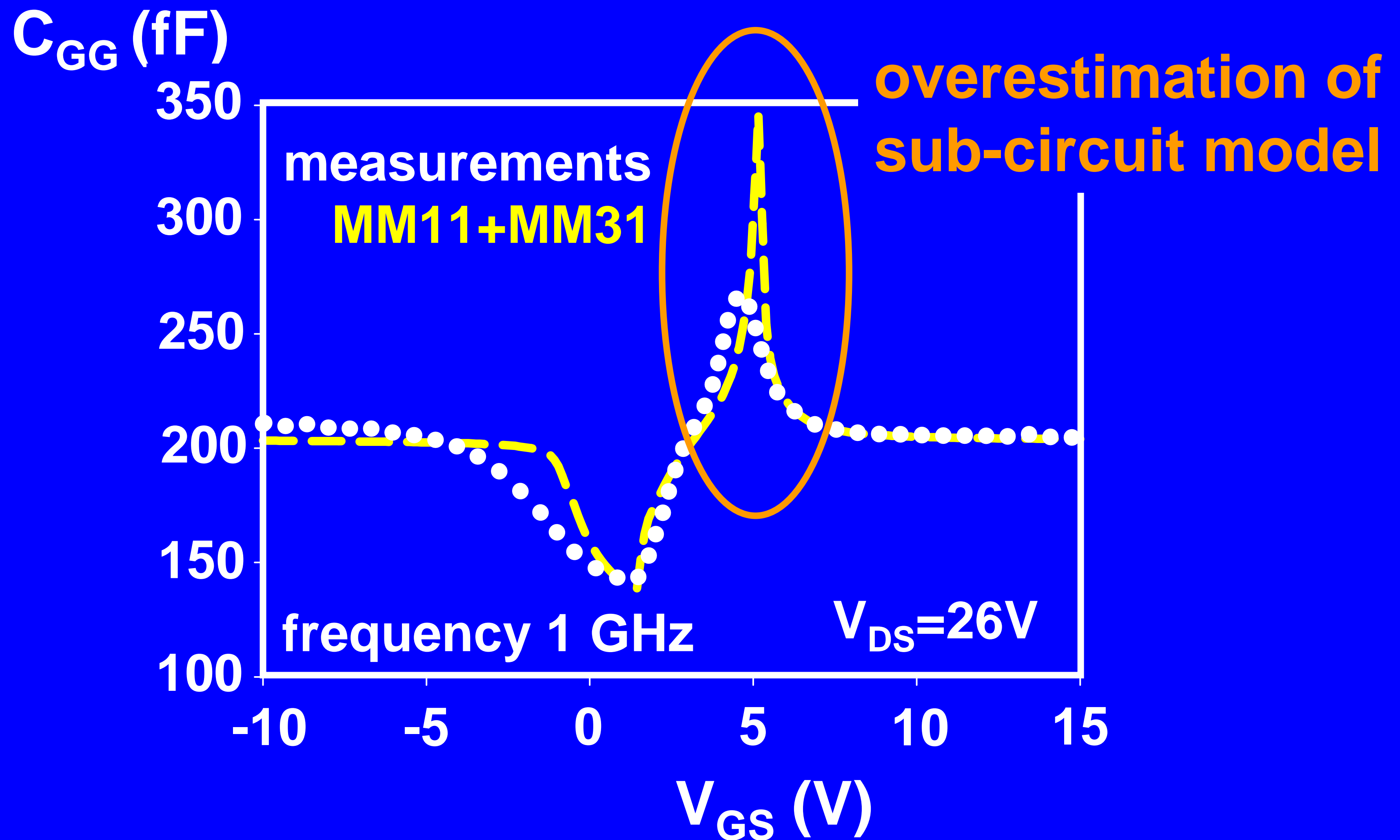
conventional sub-circuit approach



conventional sub-circuit approach

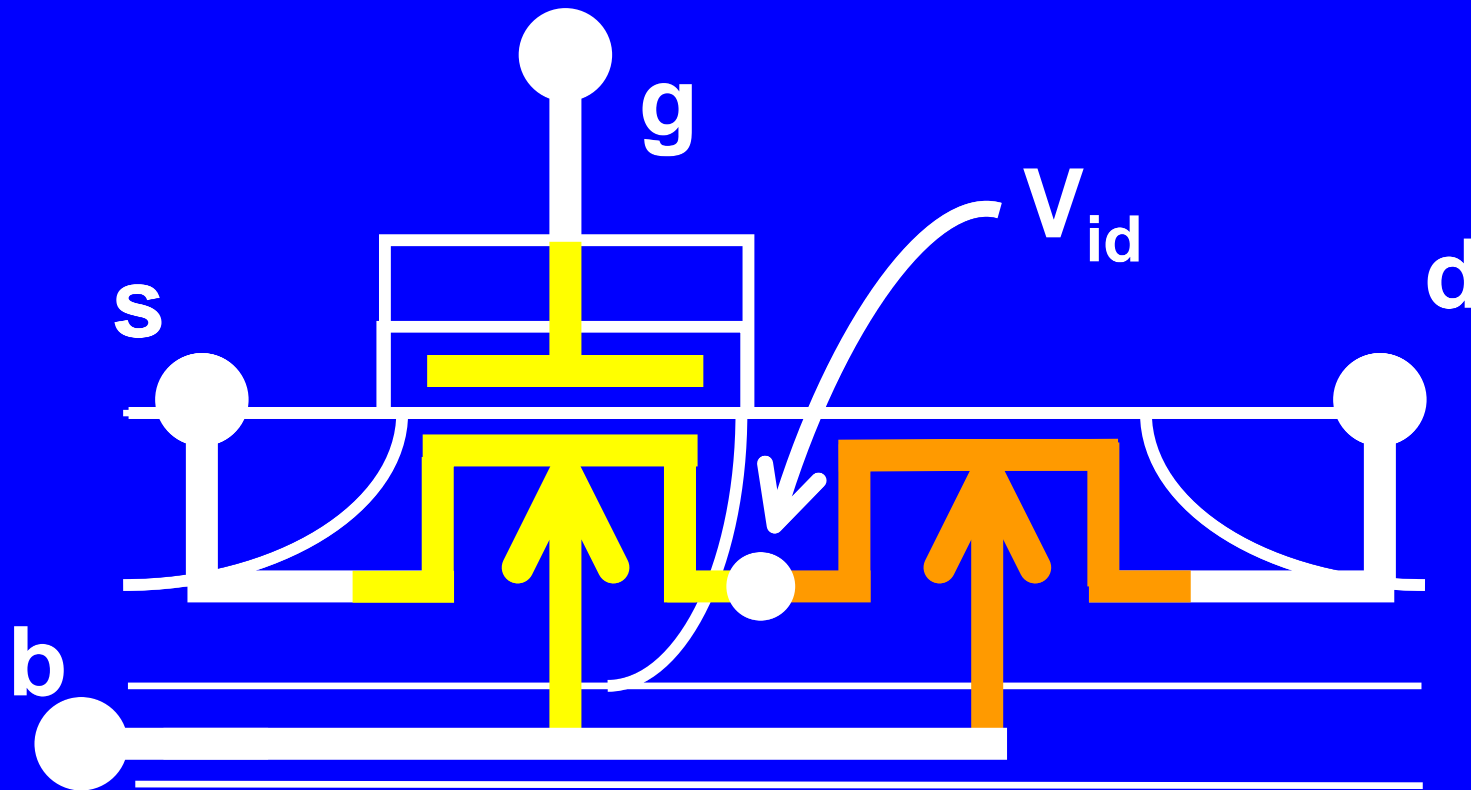


conventional sub-circuit approach



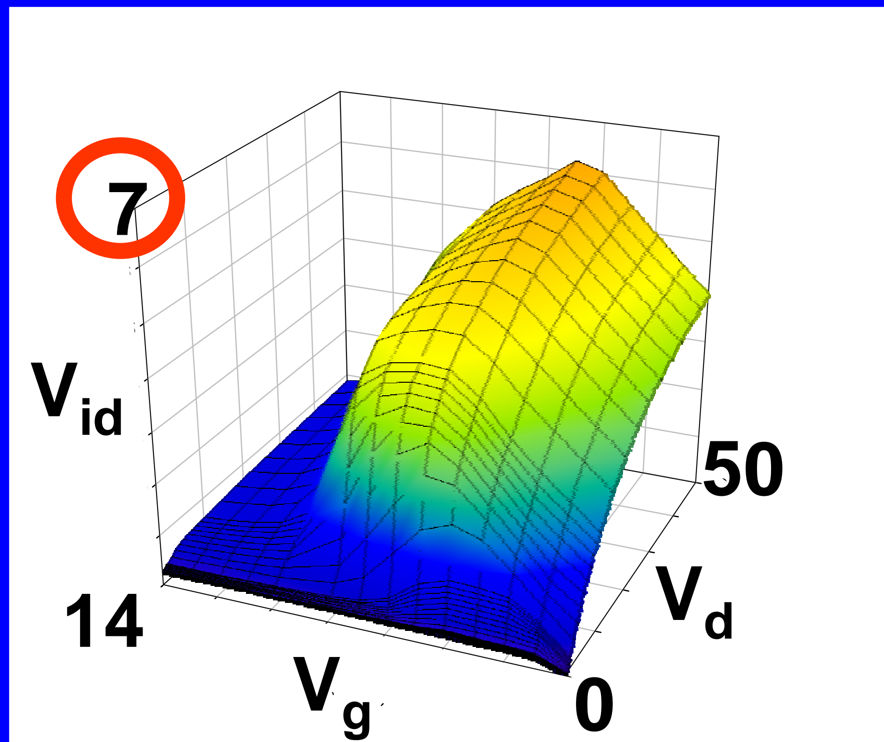
conventional sub-circuit approach

→ testing internal drain voltage (V_{id})



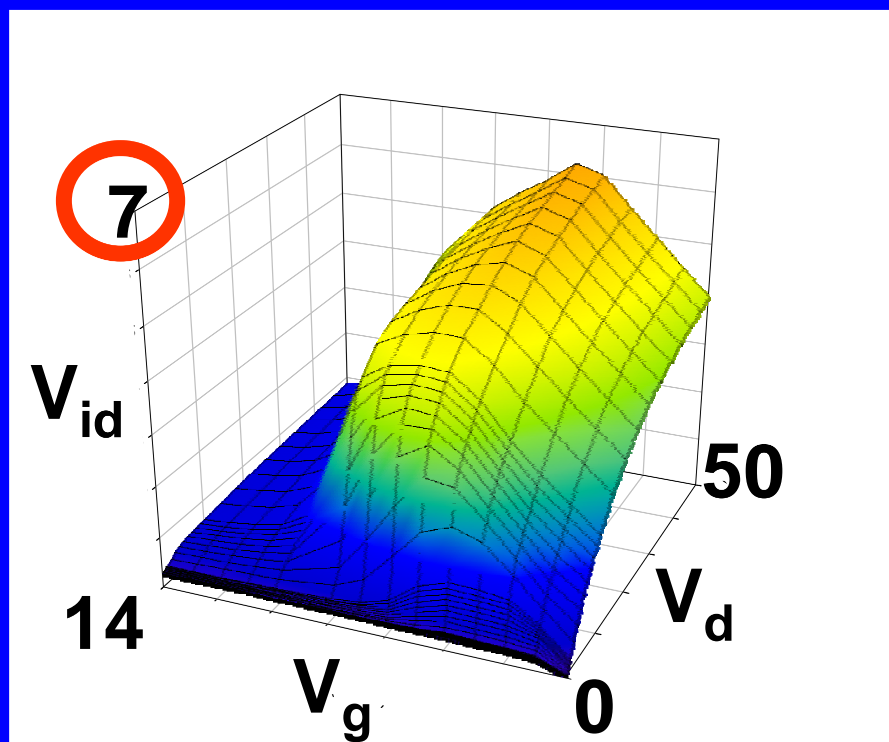
conventional sub-circuit approach

device simulations
TCAD

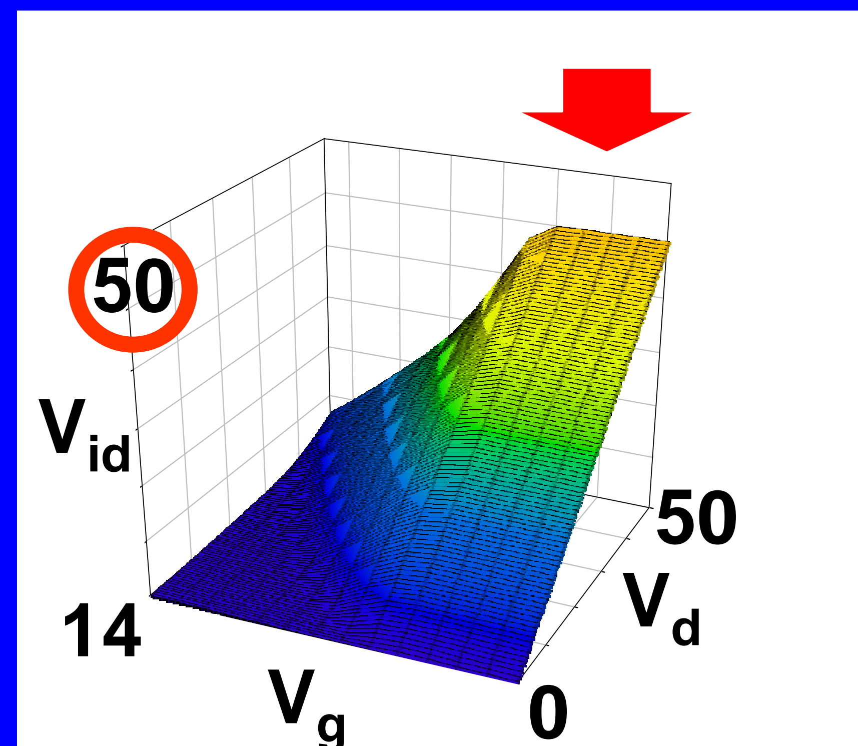


conventional sub-circuit approach

device simulations TCAD

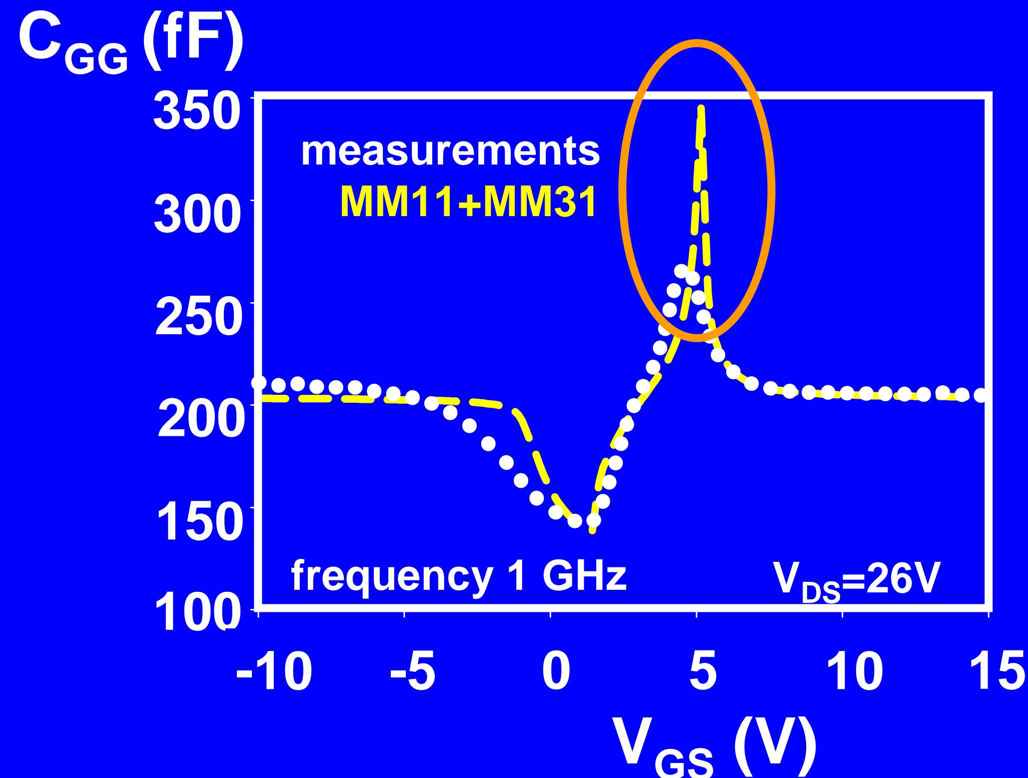


sub-circuit simulations



internal drain voltage too large !

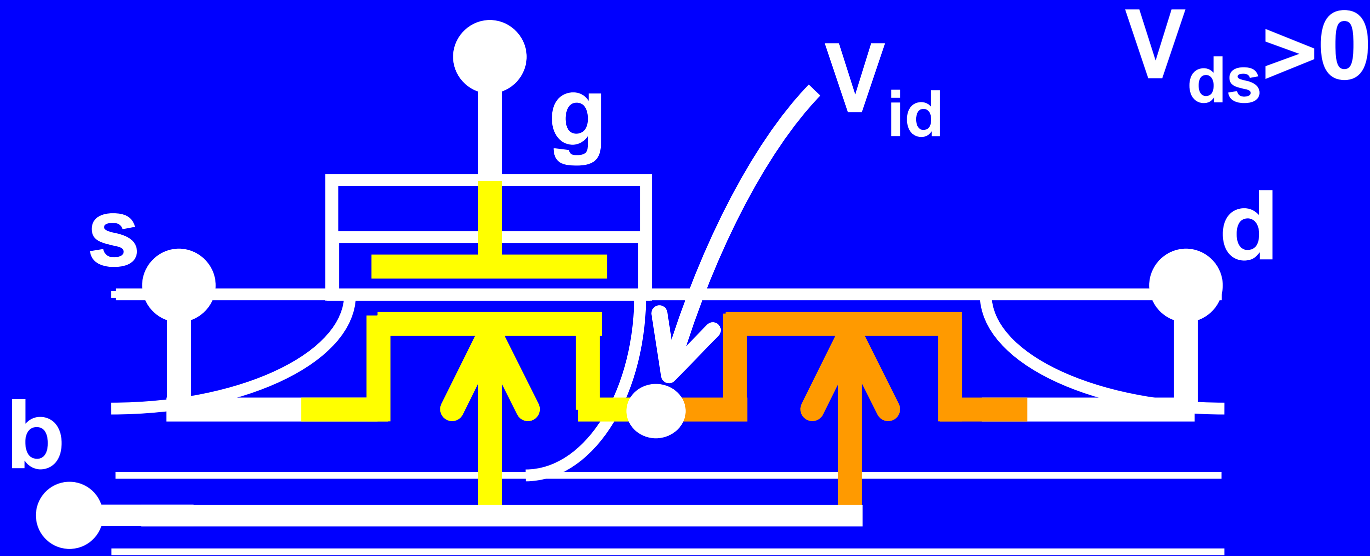
conventional sub-circuit approach



$$C_{GG}^{LDMOS} = C_{GG}^{channel} - C_{GiD}^{channel} \cdot \frac{\partial V_{ID}}{\partial V_G}$$

conventional sub-circuit approach

➡ limitation of conventional models

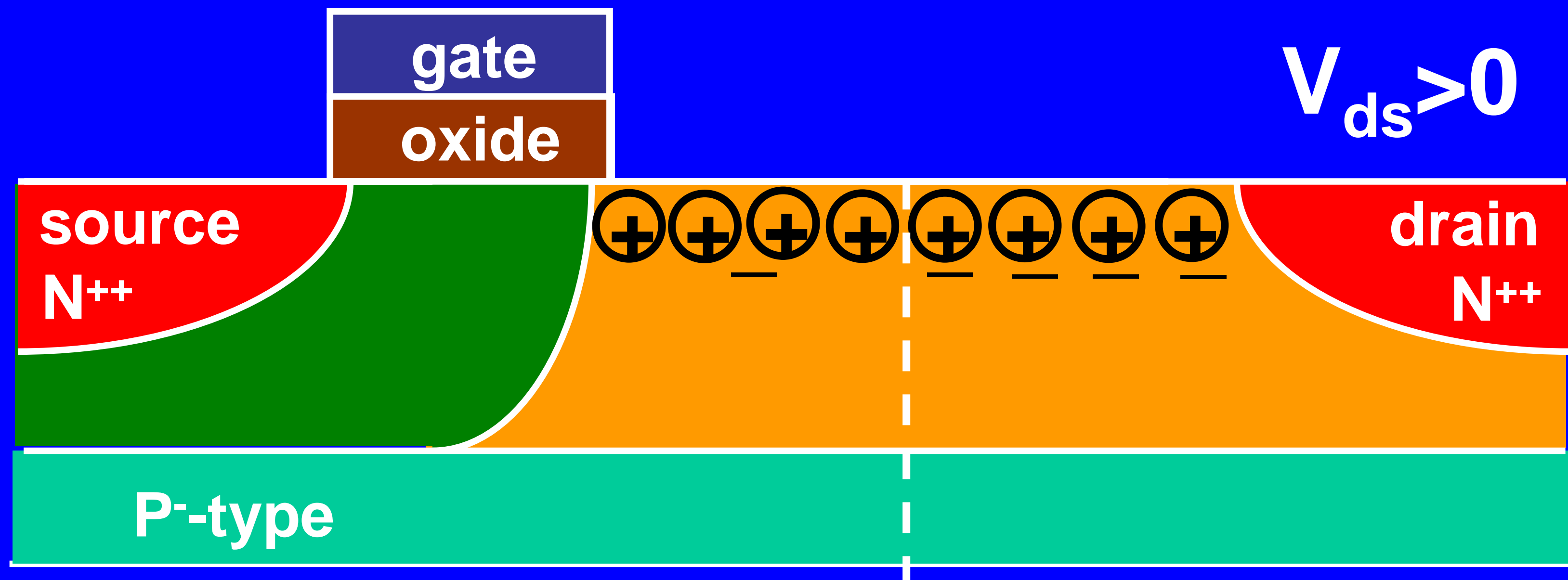


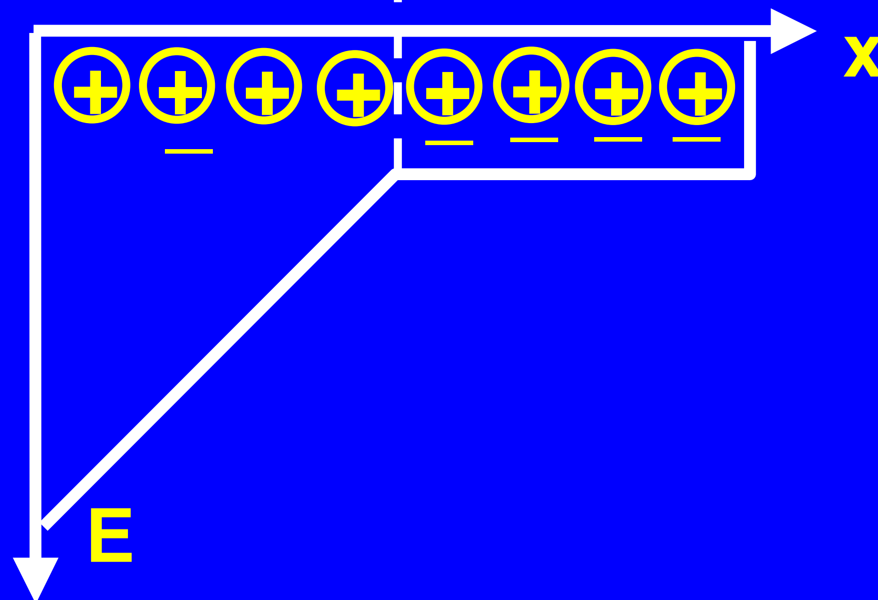
JFET models or **resistors** are not capable of sustaining large voltages at low currents

outline

- introduction
- evaluation of existing compact models
- missing phenomena in drift region models
- improved drift region model
- comparison
  - device simulations
  - measurements
- implementation in circuit simulators
- summary

missing phenomena in drift region models





partial lateral depletion sustains high voltages at low currents

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physics of a gate-less drift region

1D Poisson equation

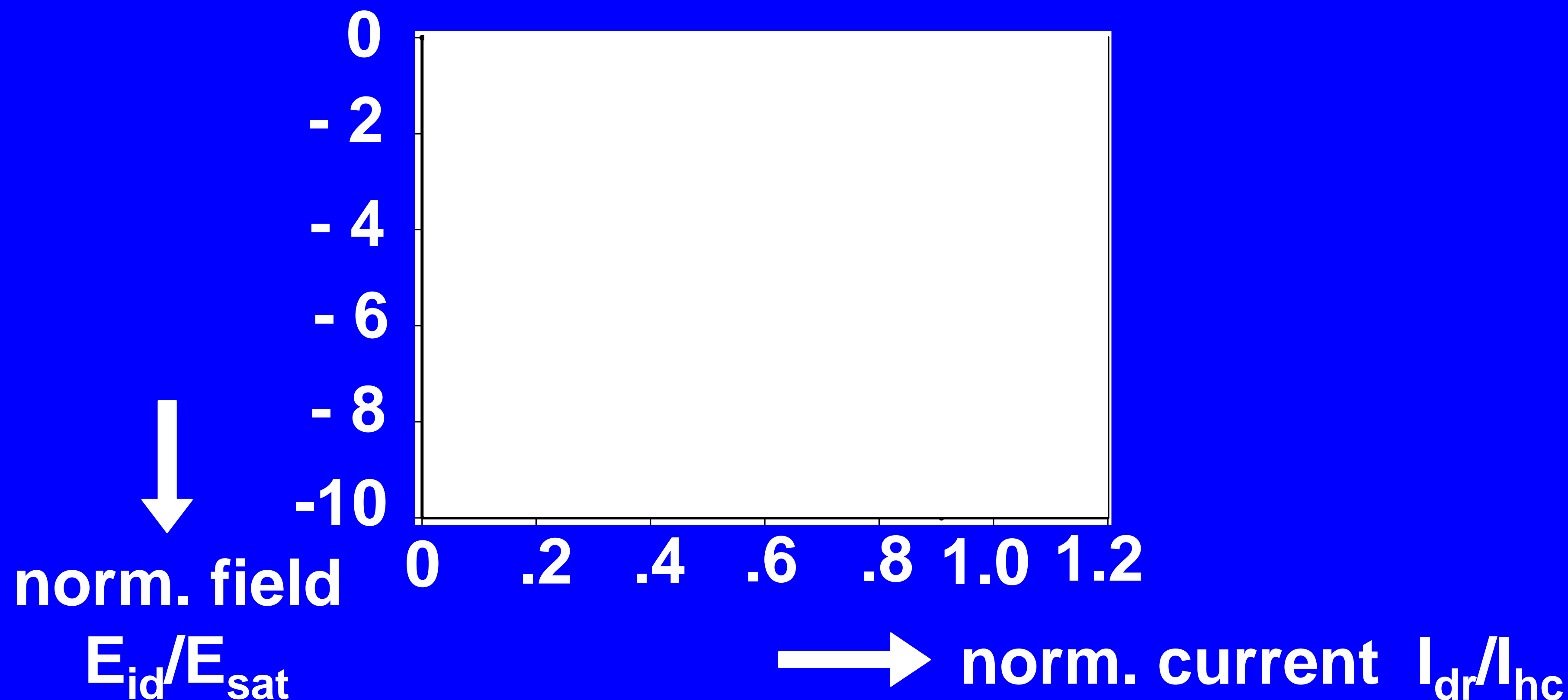
$$\frac{dE}{dx} = qN_D \left(1 - \frac{I_{dr}}{qN_D A v_{dr}} \right)$$

- E : electric field
- I_{dr} : current
- N_D : dope concentration
- A : cross section area
- $v_{dr} = \frac{\mu E}{1 + |E| / E_C}$: drift velocity

- charge distribution
- electric field distribution

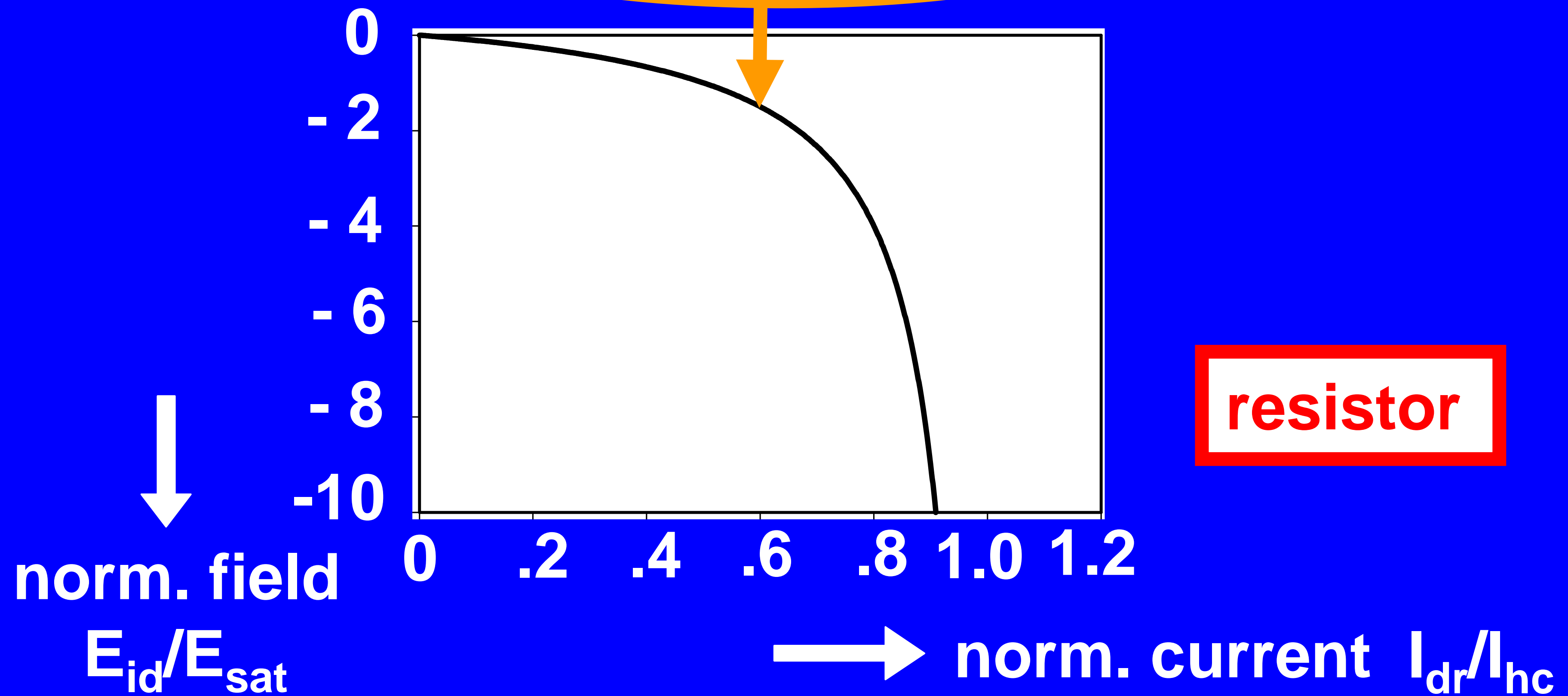
operation modes drift region

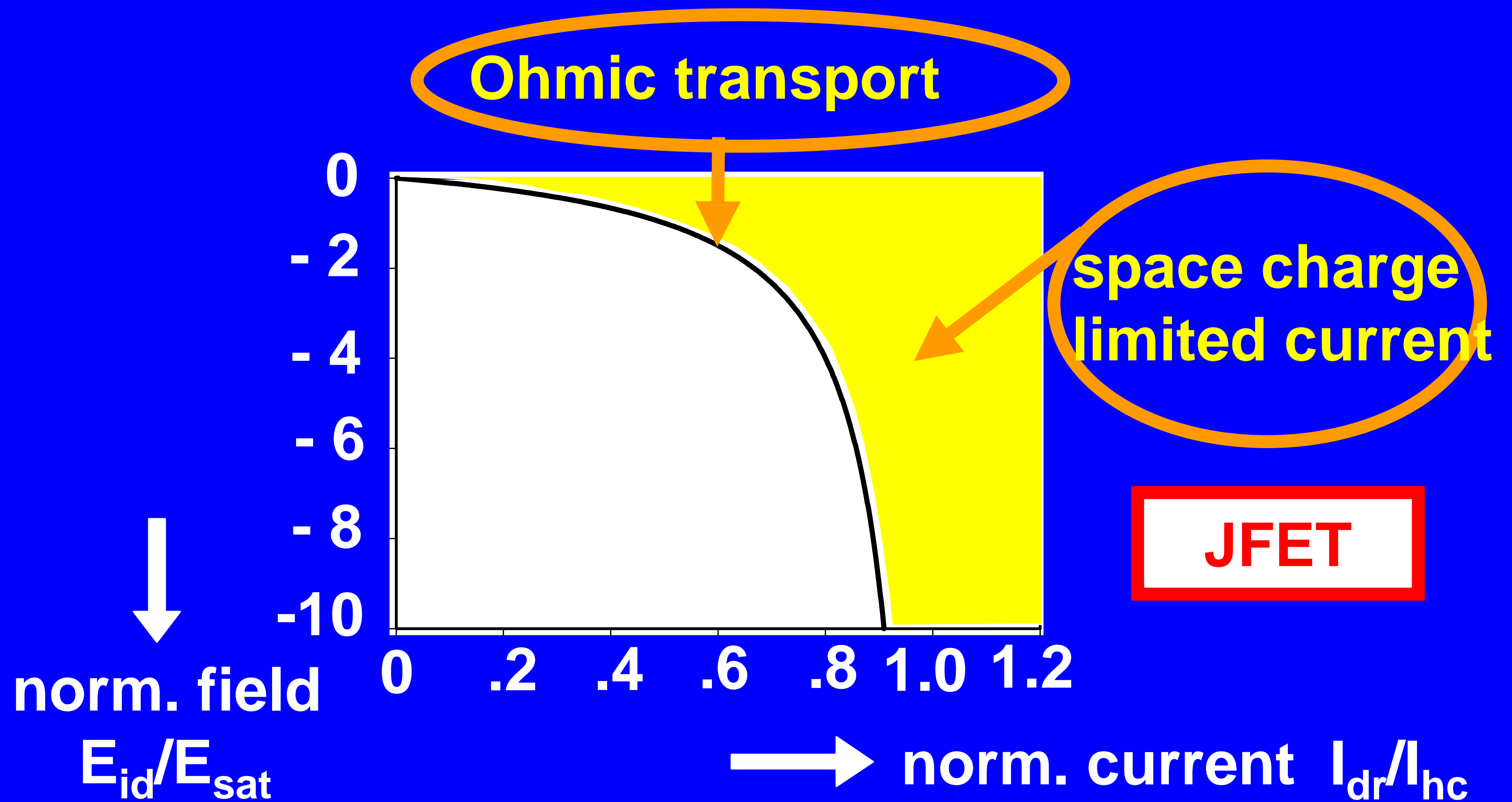
“phase” diagram



operation modes drift region

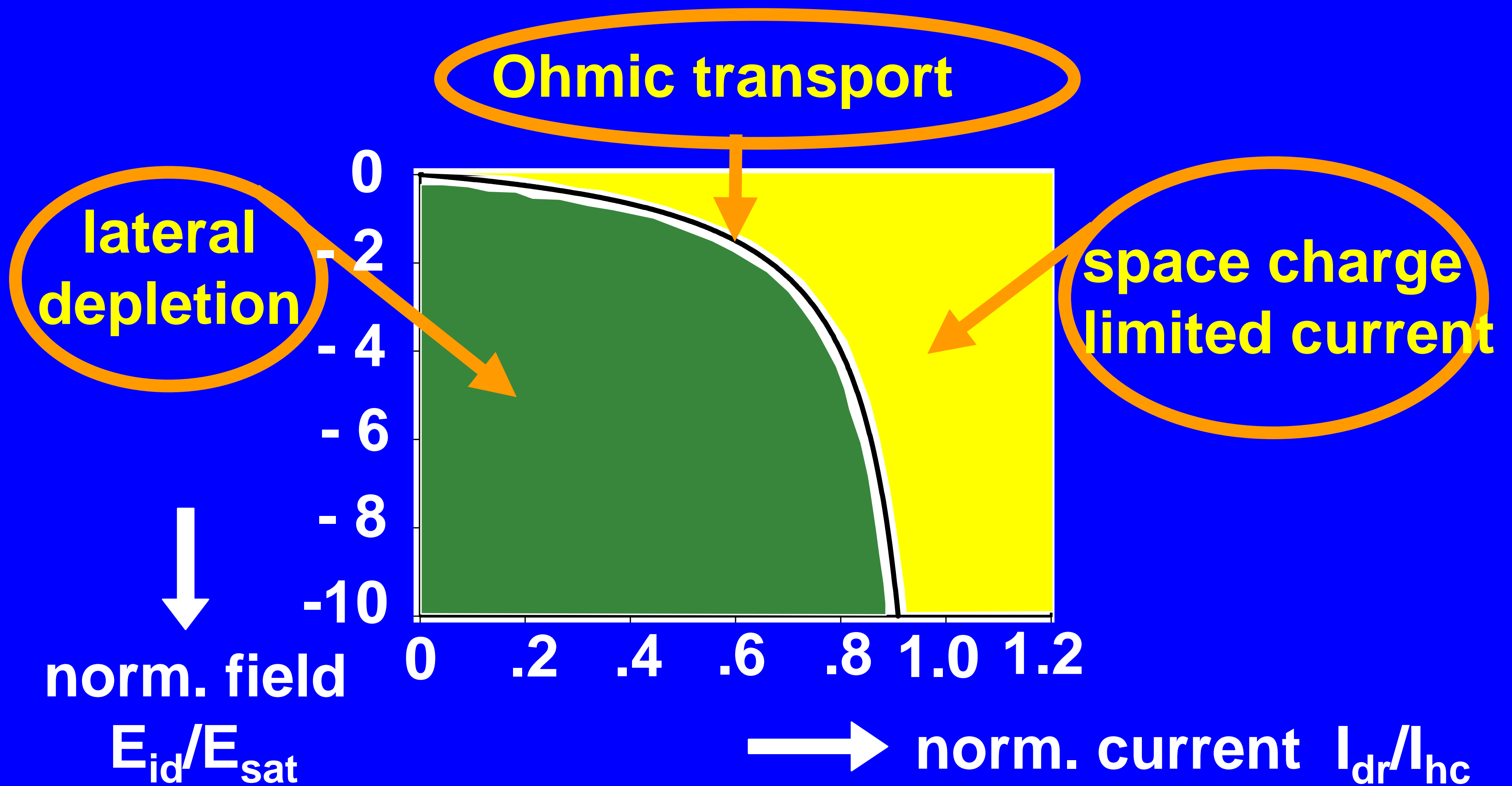
“phase” diagram



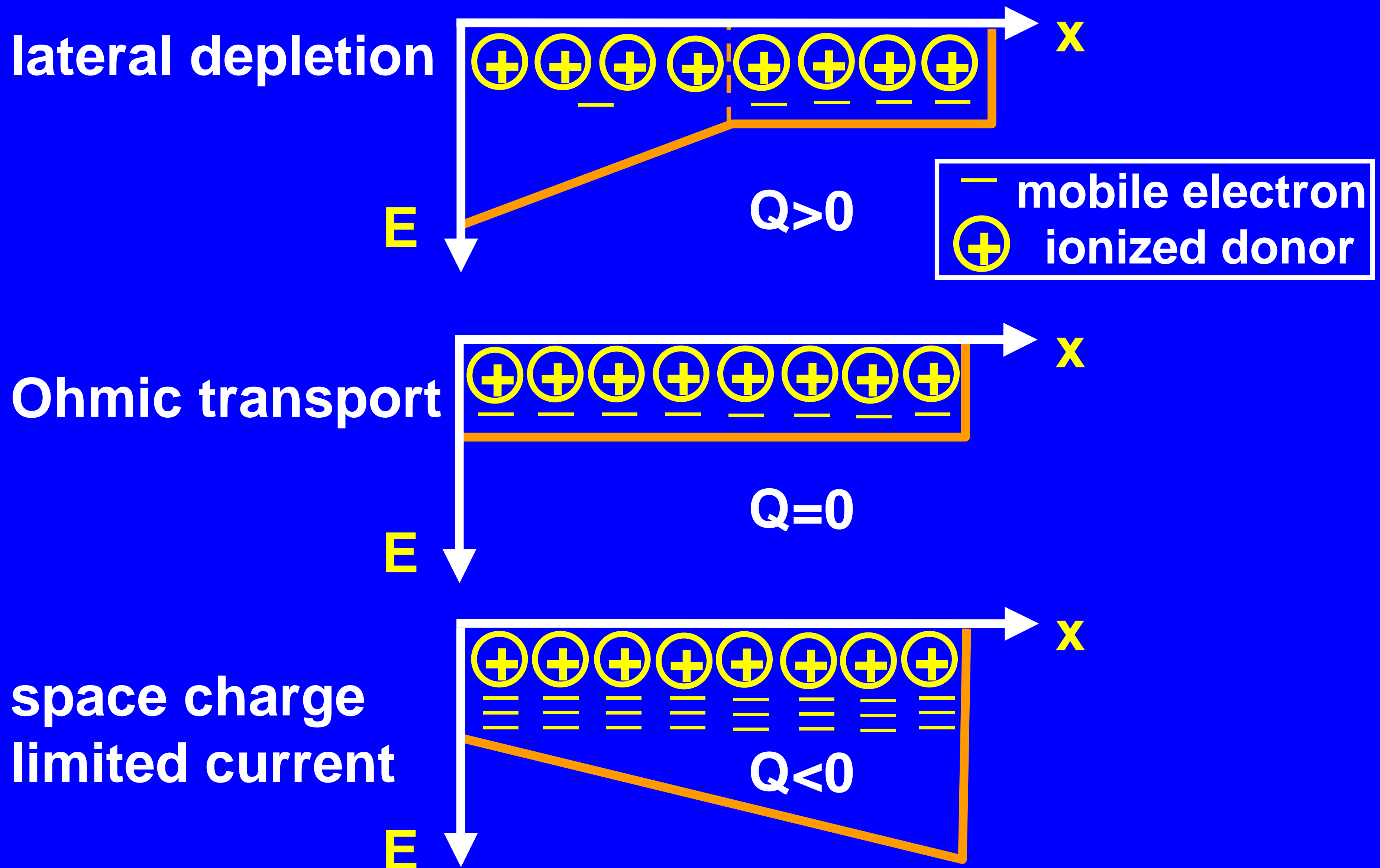

operation modes drift region
“phase” diagram
Ohmic transport
space charge
limited current
JFET
0
- 2
- 4
- 6
- 8
-10
0
.2
.4
.6
.8
1.0
1.2
norm. field
E_{id}/E_{sat}
norm. current I_{dr}/I_{hc}

operation modes drift region

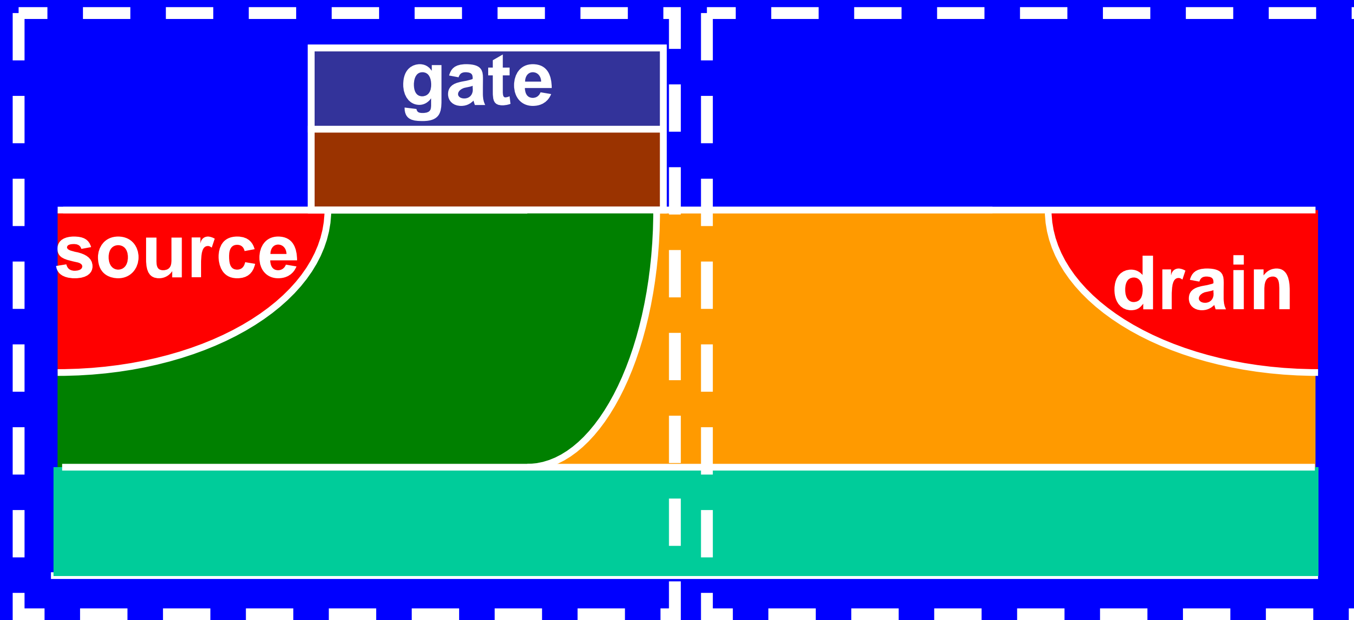
“phase” diagram



operation modes drift region



integration MOS and drift region



- <u>Kirchoff's laws</u>: voltages and currents are equal at the internal drain
- <u>extra boundary condition</u>: continuous lateral electric field at internal drain

lateral electric field in channel

linear region

$$E_{id} = -\frac{I_{ids}}{\mu W Q_I^{'}}$$

saturation

$$E_{id} = -E_{sat}\cosh\left(\Delta L / l_c\right)$$

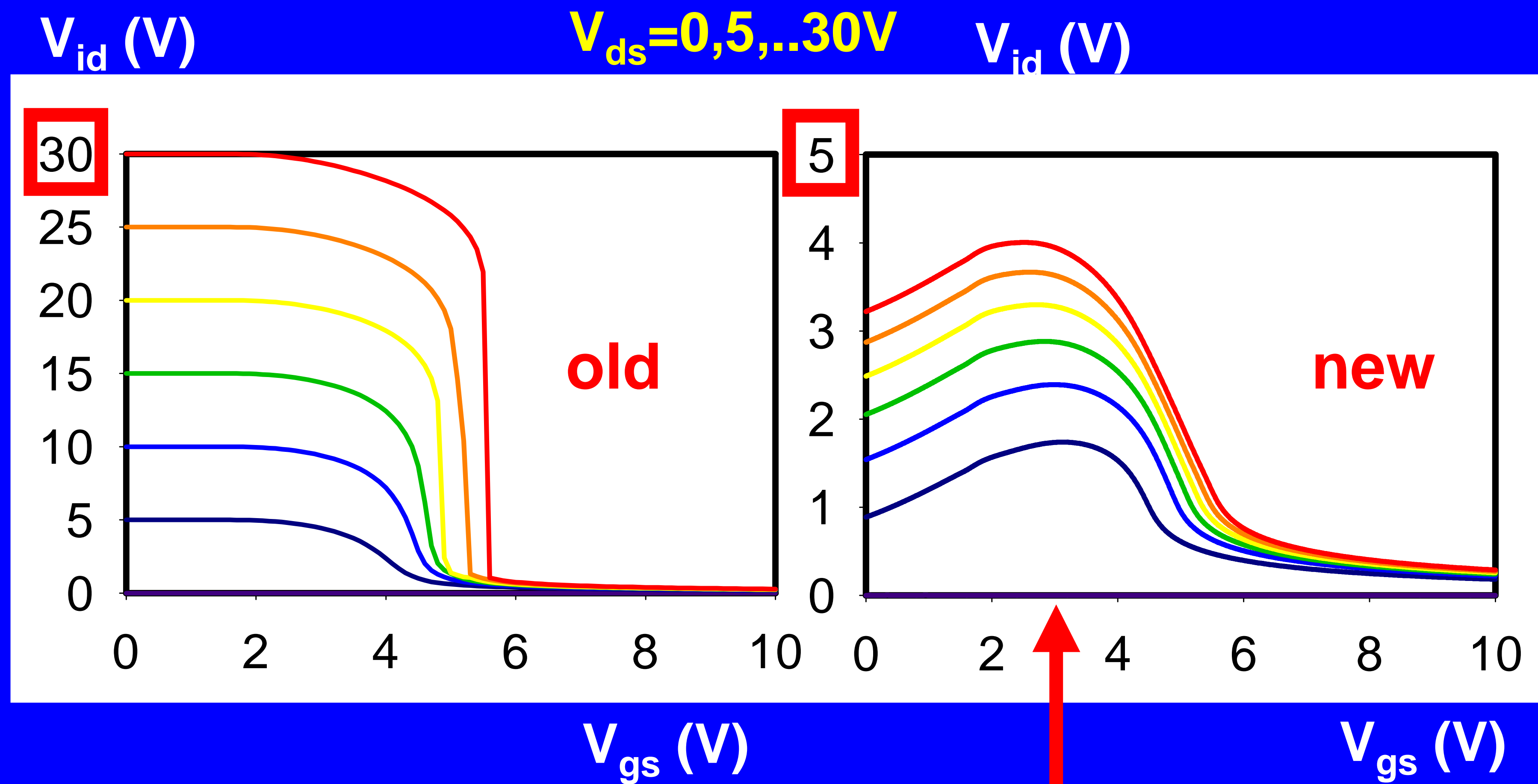
I_{ids} current, mobility

W width, $Q_I^{'}$ inversion charge

E_{sat} velocity saturation field

$\Delta L, l_c$ channel length modulation

simulations with new model



physical solution for internal drain voltage

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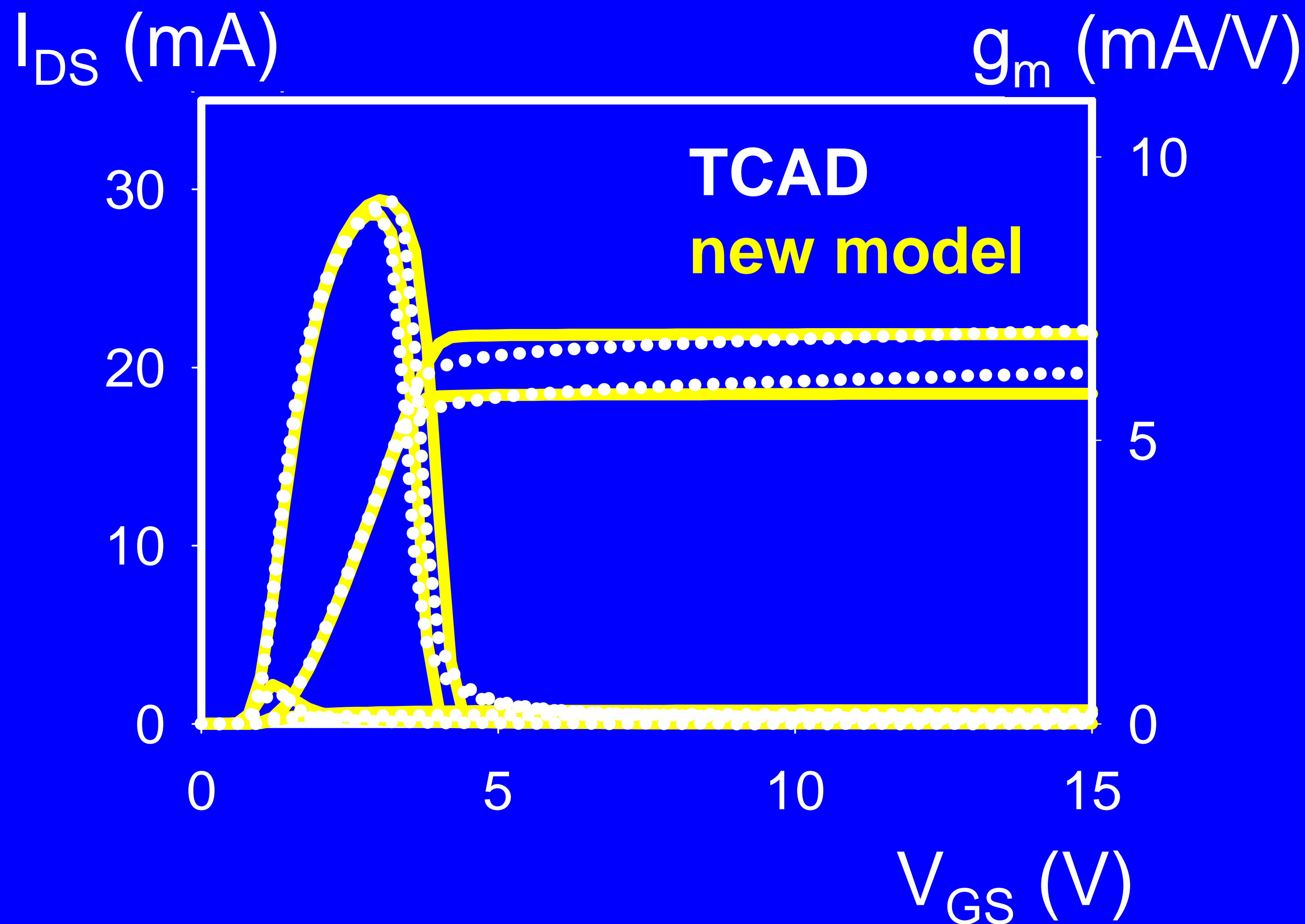
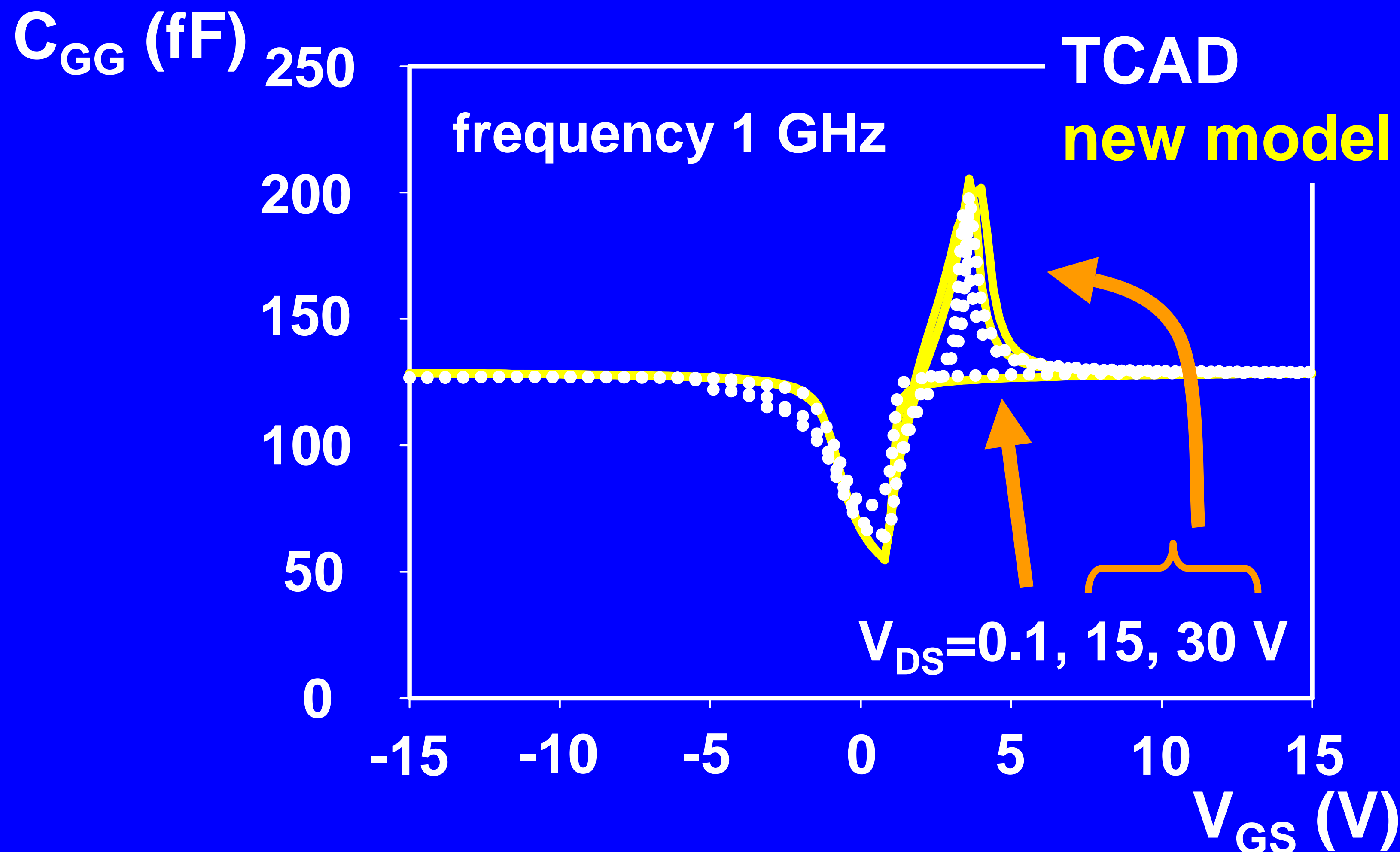
comparison device simulations



comparison device simulations

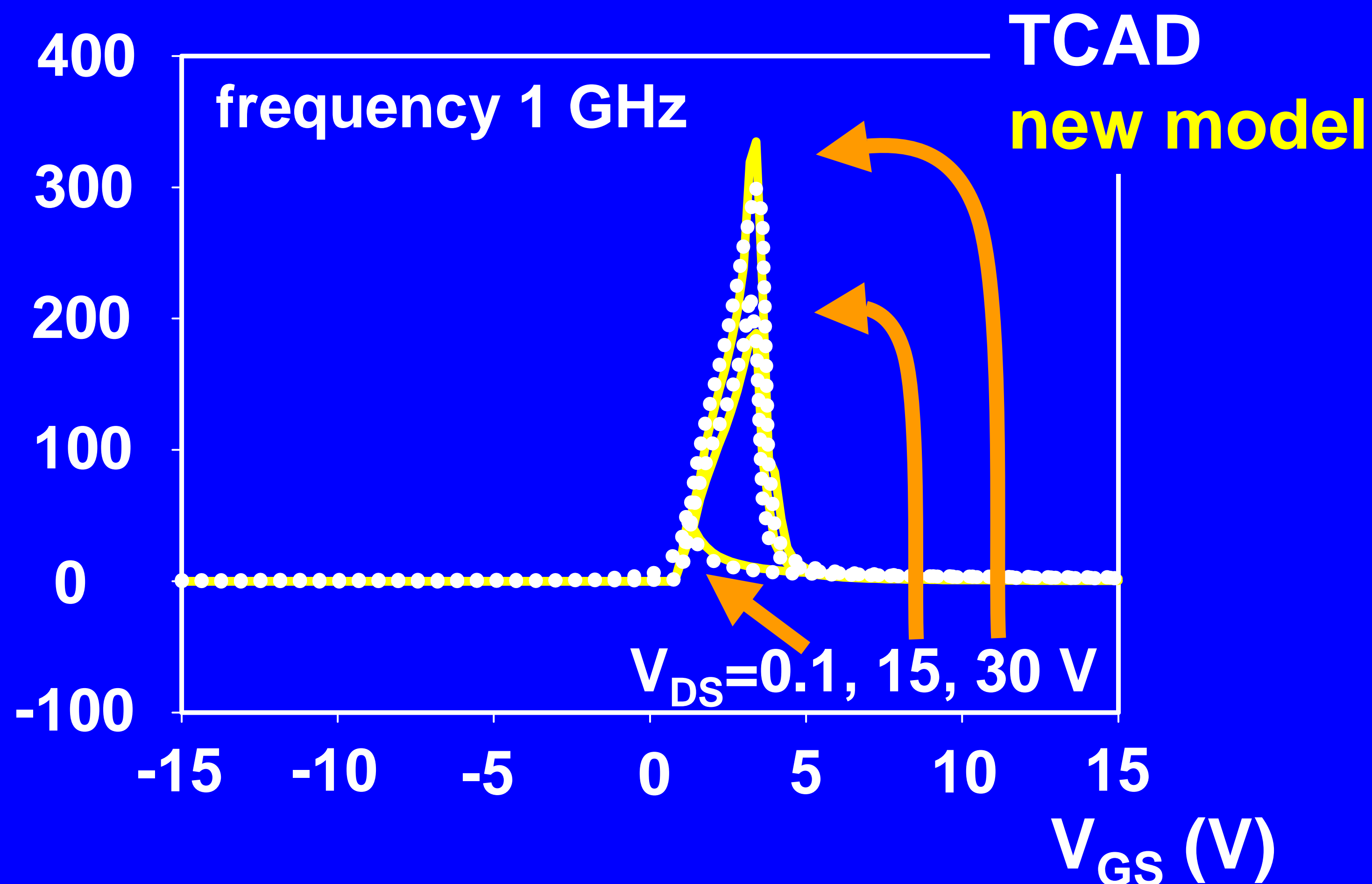
input capacitance



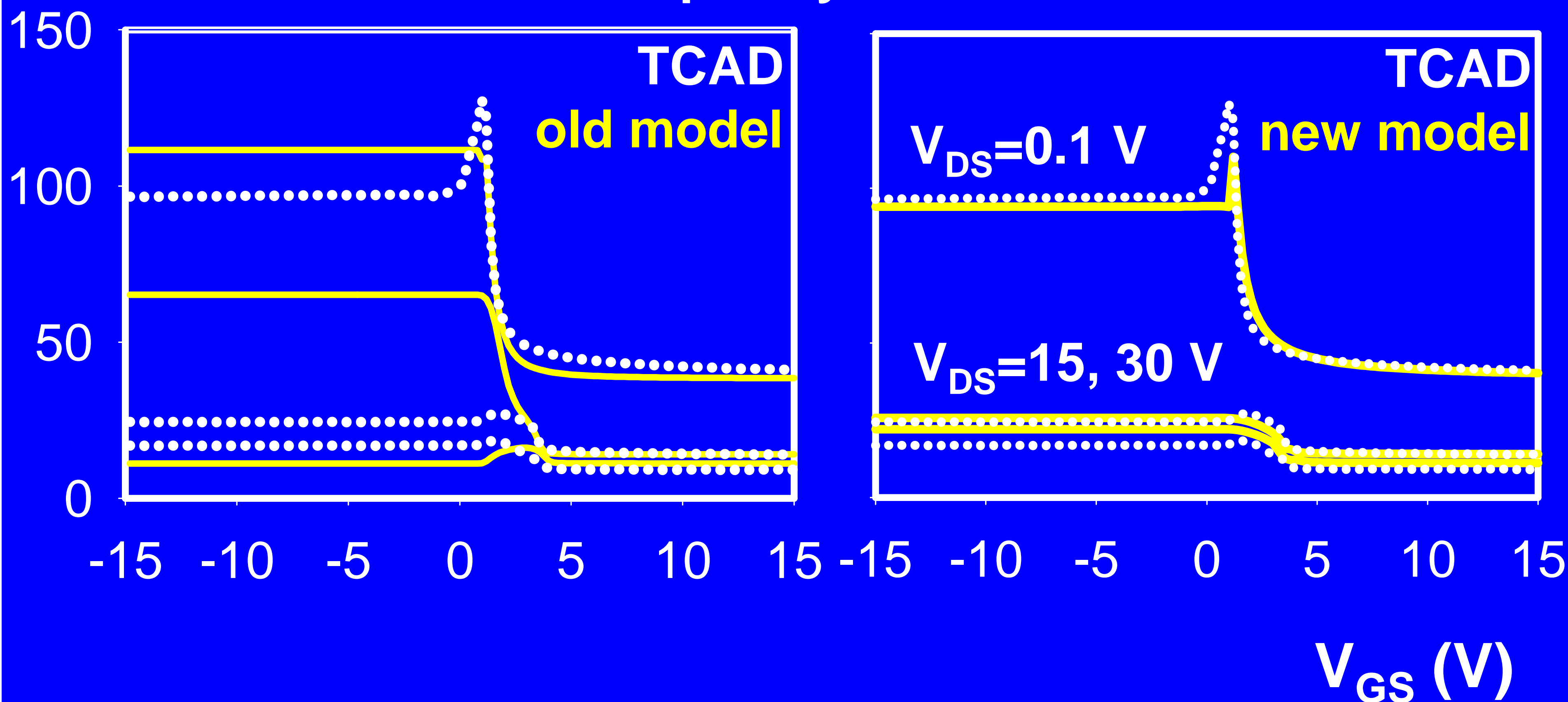
comparison device simulations

C_{DG} (fF)

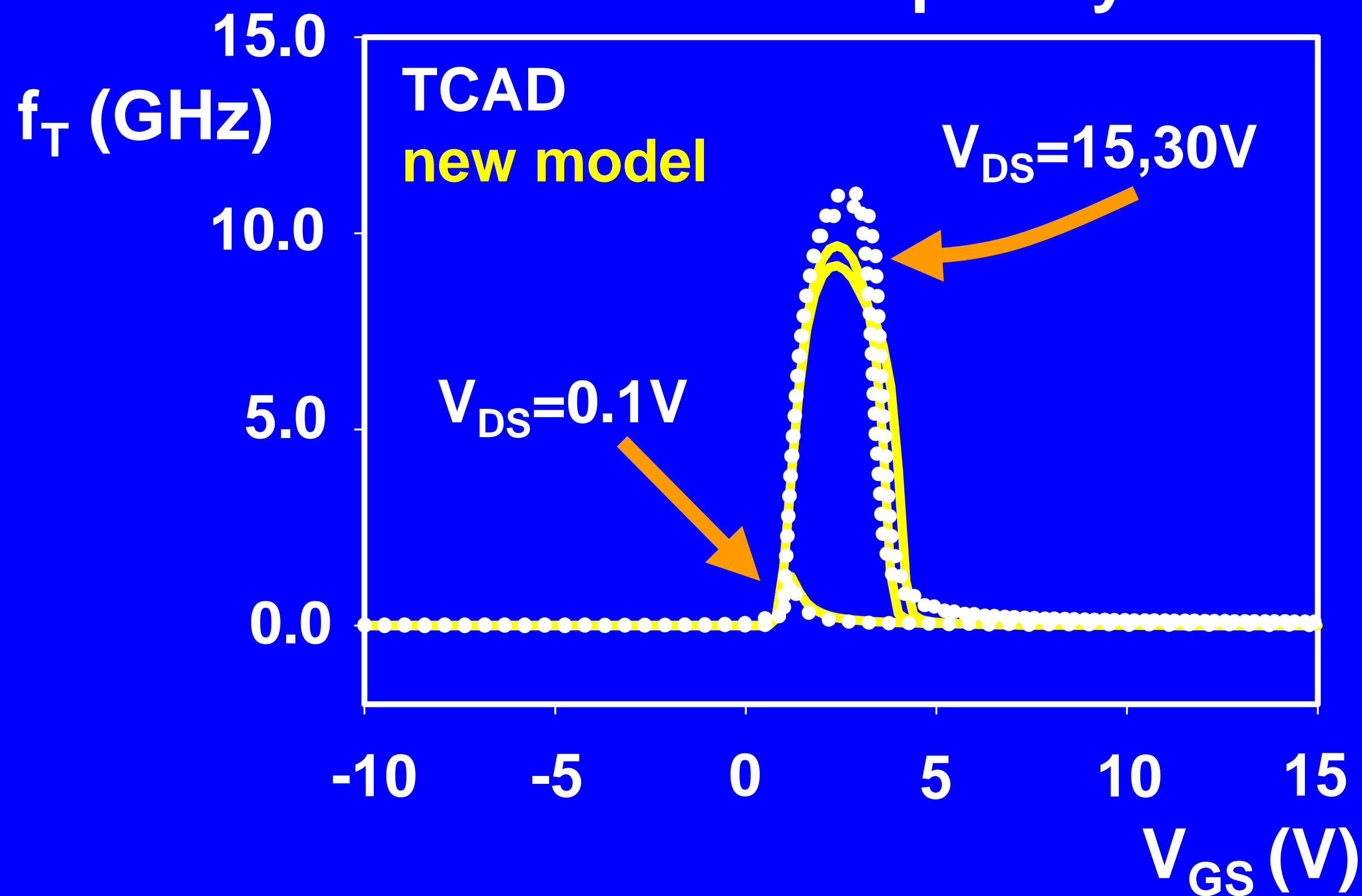
feedforward capacitance



comparison device simulations



comparison device simulations



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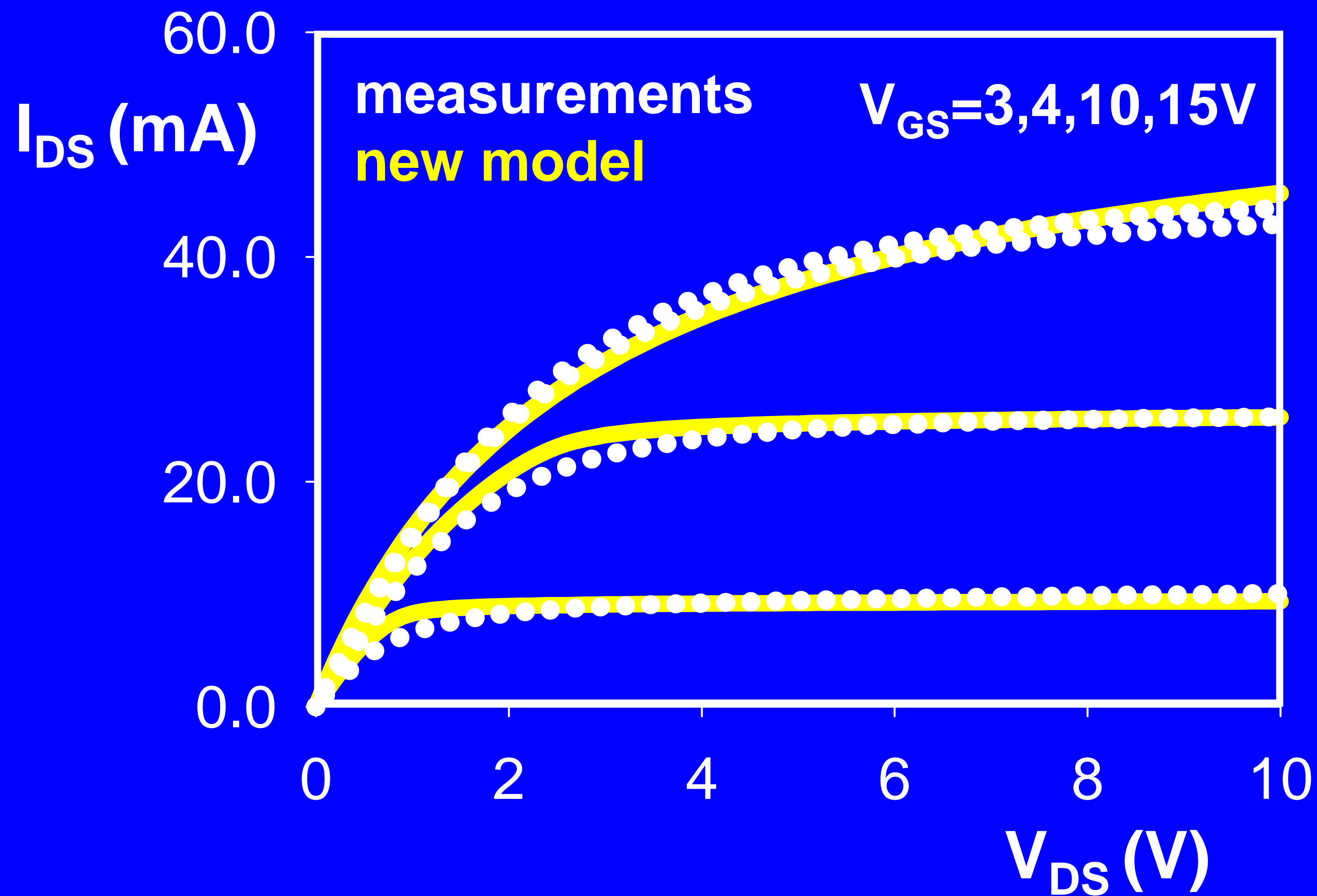
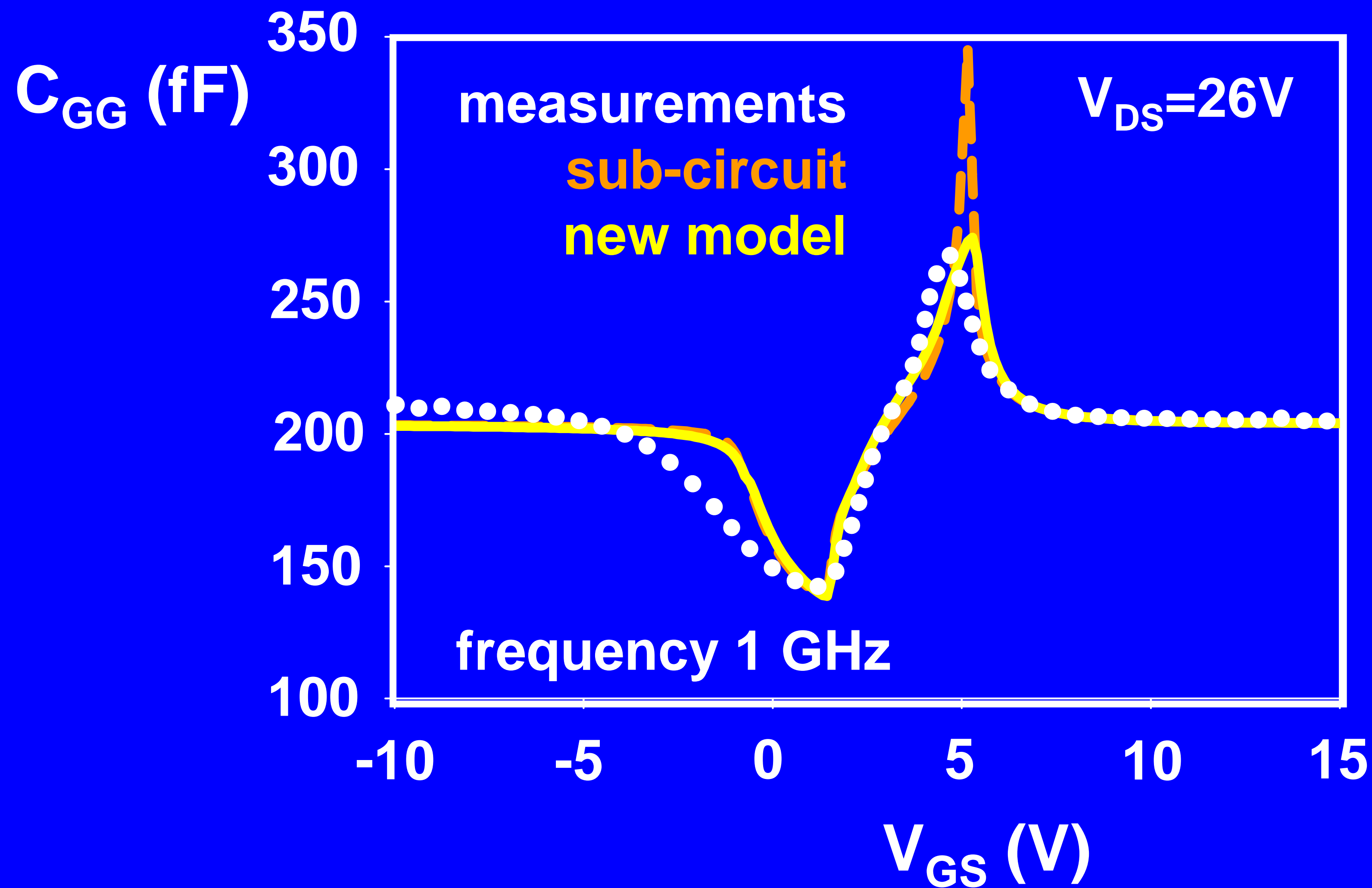
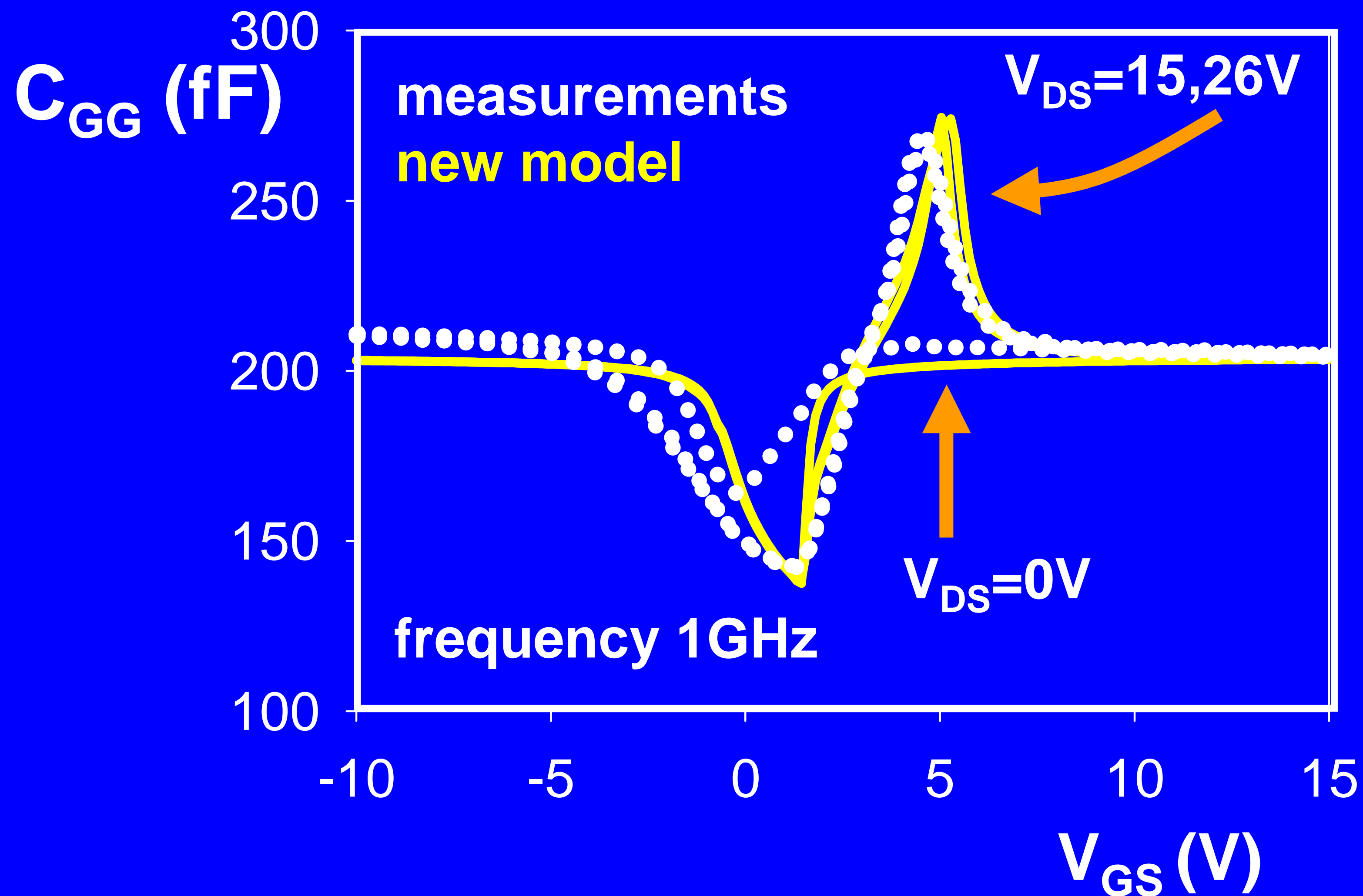
comparison measurements



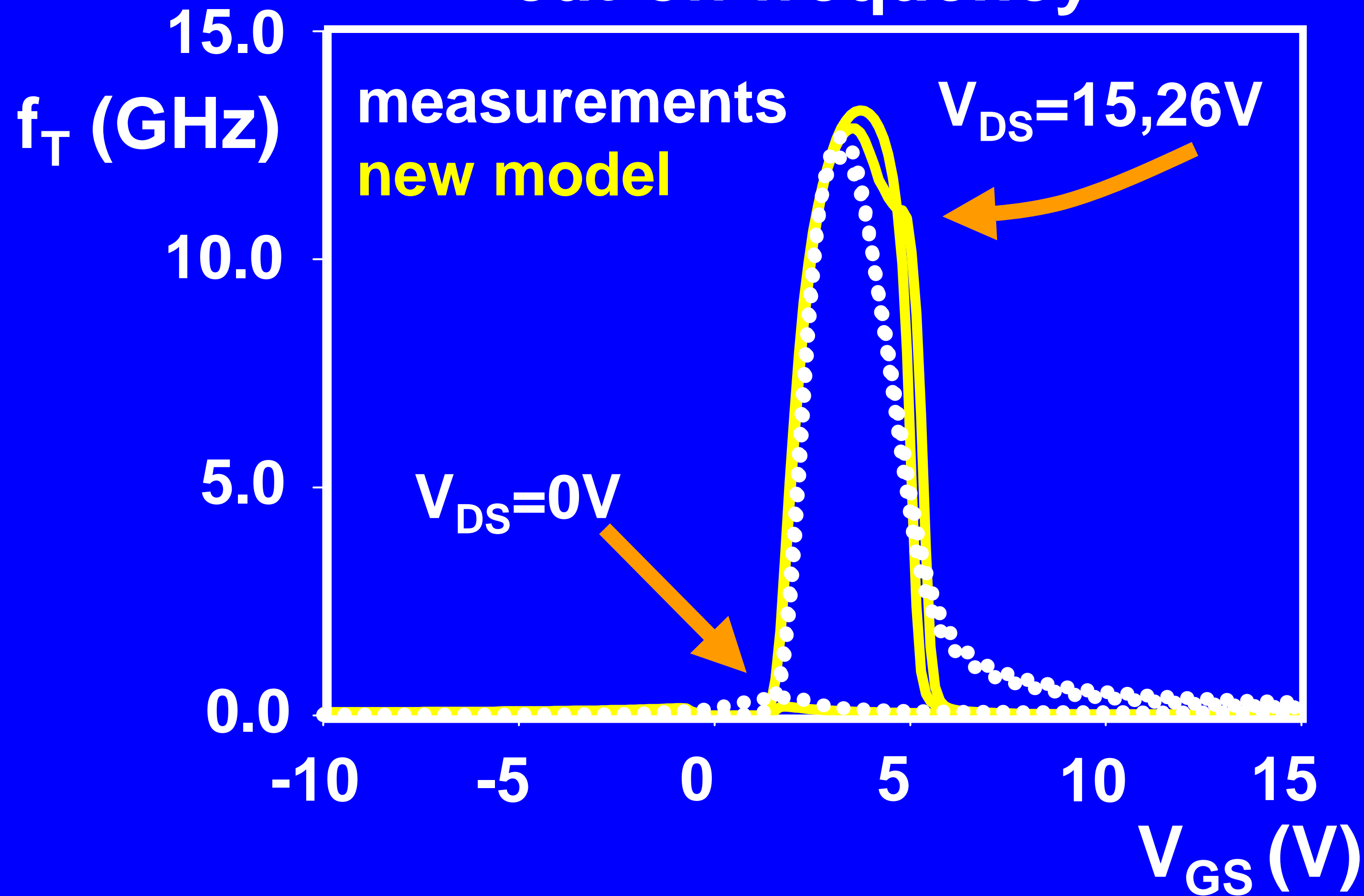
comparison measurements



comparison measurements



comparison measurements



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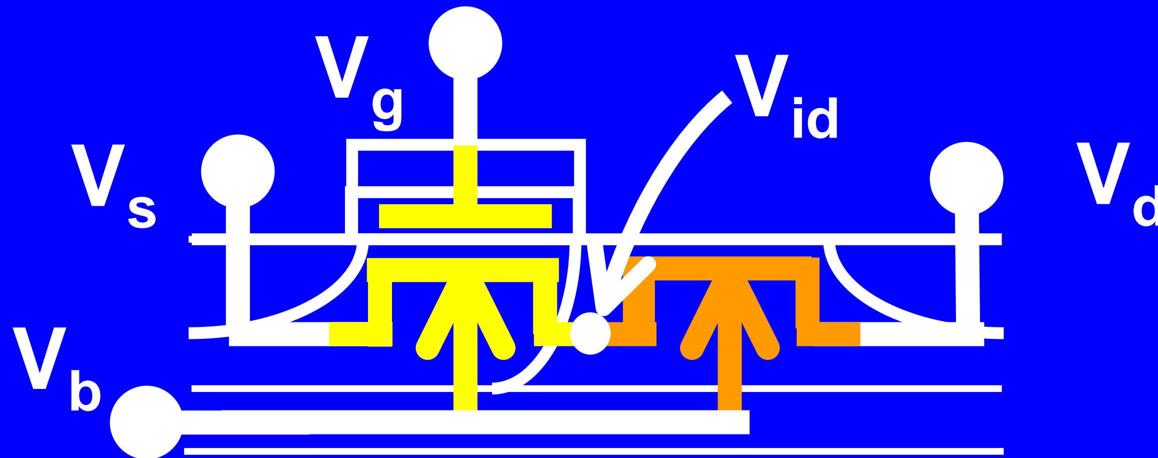
- improved drift region model
- comparison
  - device simulations
  - measurements
- implementation in circuit simulators
- summary

implementation in circuit simulators

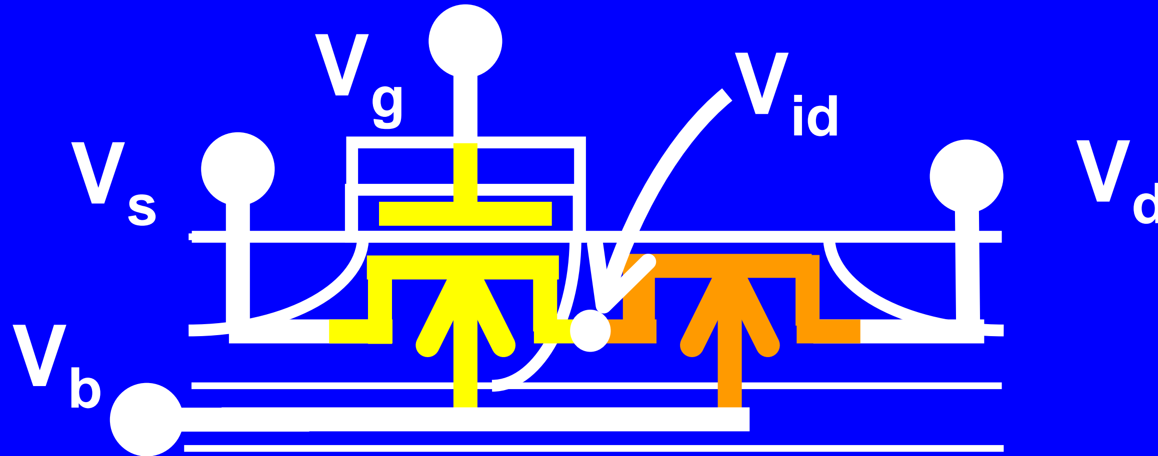


lateral electric field in channel

terminal voltages
V_{id}, V_g, V_s, V_b

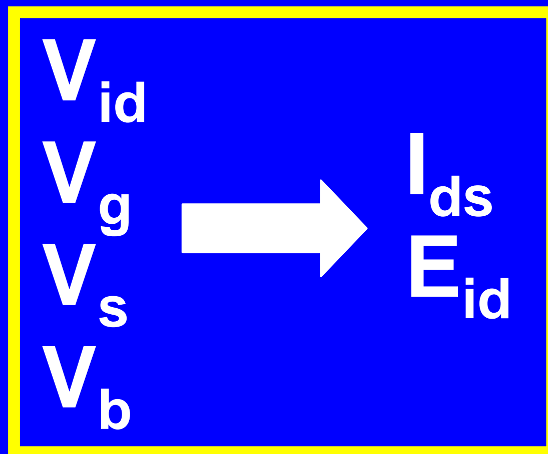
current I_{ids}
elec. field E_{id}

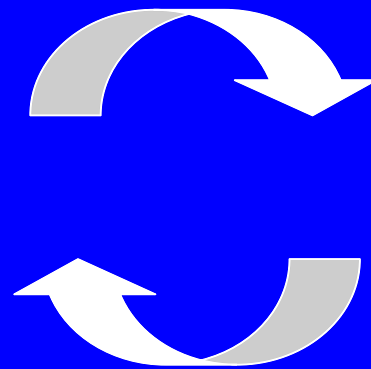
implementation in circuit simulators

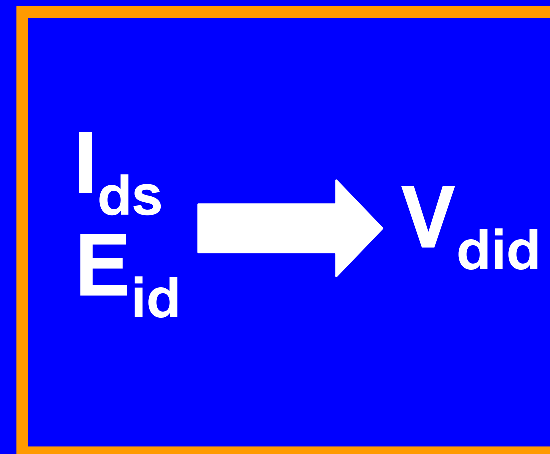


MOS model

drift region model







outline

- introduction
- evaluation of existing compact models
- missing phenomena in drift region models
- improved drift region model
- comparison
  - device simulations
  - measurements
- implementation in circuit simulators
- summary

summary

- new physics-based high-voltage LDMOS model for RF applications
  - based on lateral electric field continuity
  - inclusion of partial lateral depletion
  - sound physical solution for internal drain voltage
- model validation with device simulations and measurements
  - DC-characteristics
  - Y-parameter bias sweeps (including f_T)

summary

- new physics-based high-voltage LDMOS model for RF applications
- model validation with device simulations and measurements
- implementation in circuit simulator
  - additional terminal for lateral electrical field

PHILIPS