

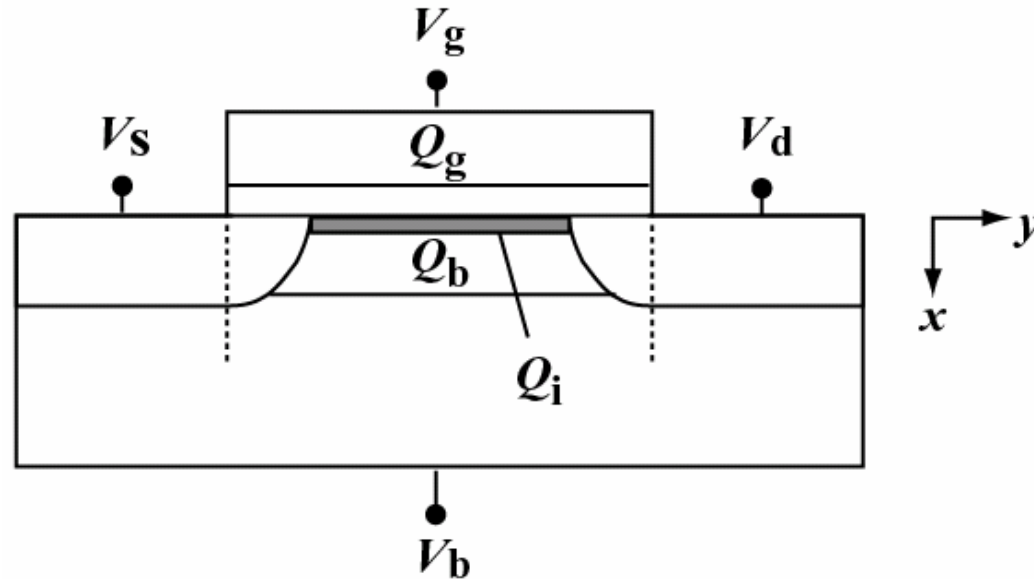
Surface-Potential-Based Modeling: Indispensable for Compact Models

Mitiko Miura-Mattausch, Hiroshima University

- **Origin of MOSFET Behavior**
 - **Charges Induced on Nodes**

- **Origin of Induced Charges**
 - **Potential Distribution in the MOSFET**

Surface Potential is the Basis for the Self-Consistent Modeling



$$I_{ds} = q \frac{W}{L} \int v Q_i dy$$

current



$$Q$$

charge



$$C_{jk} = \frac{dQ_j}{dV_k}$$

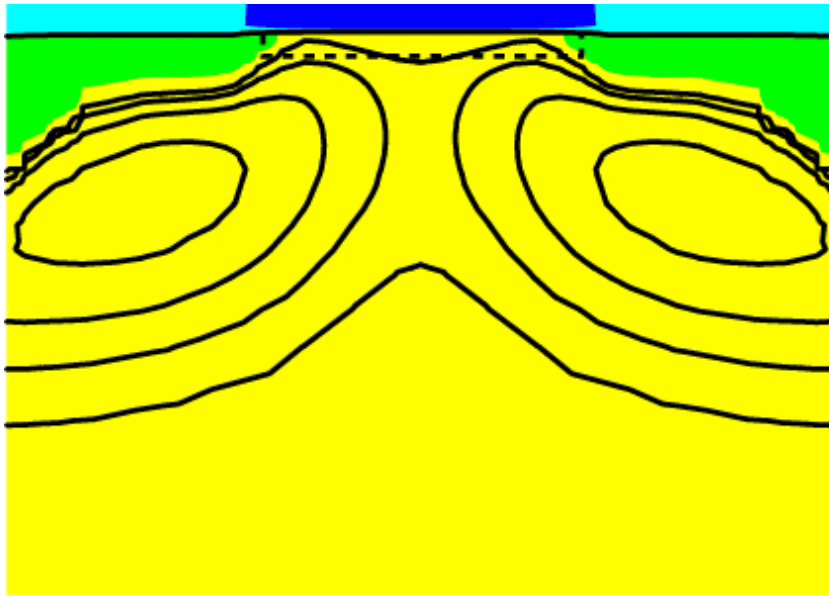
capacitance

$$Q_b(y) = -qN_{\text{sub}} \times W_d = -\sqrt{\frac{2\epsilon_s qN_{\text{sub}}}{\beta}} \left\{ \beta \left(\phi_s(y) - V_{bs} \right) - 1 \right\}^{-\frac{1}{2}}$$

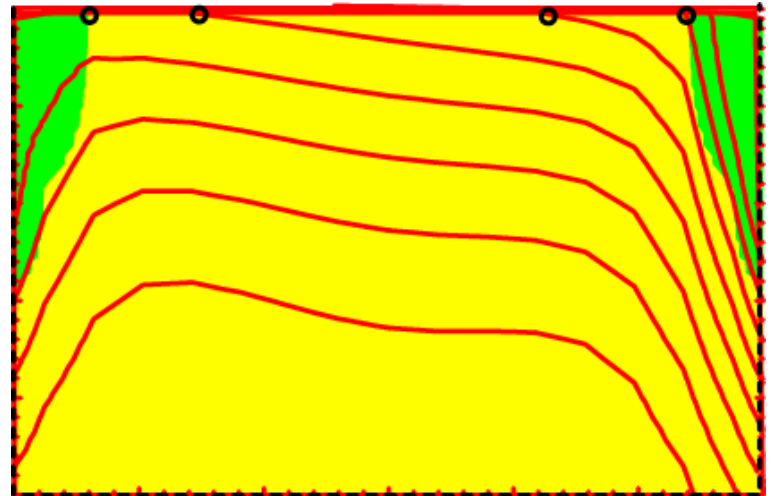
ϕ_s : surface potential

Surface-Potential Distribution Reflects Technology Dependence

Impurity Profile with Pocket Implant



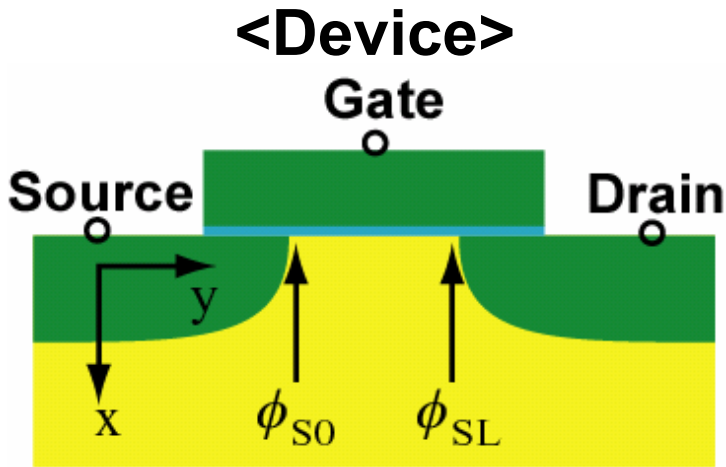
Calculated Potential Distribution



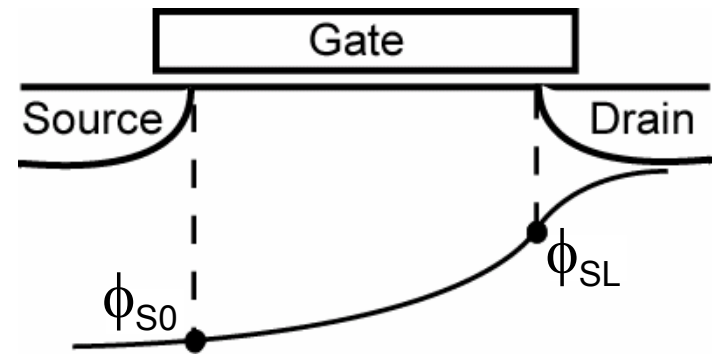
Surface-Potential Distribution



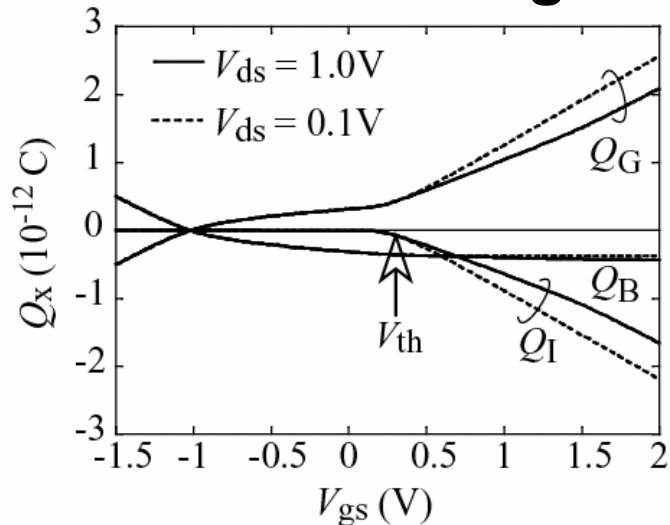
Schematic Relationship



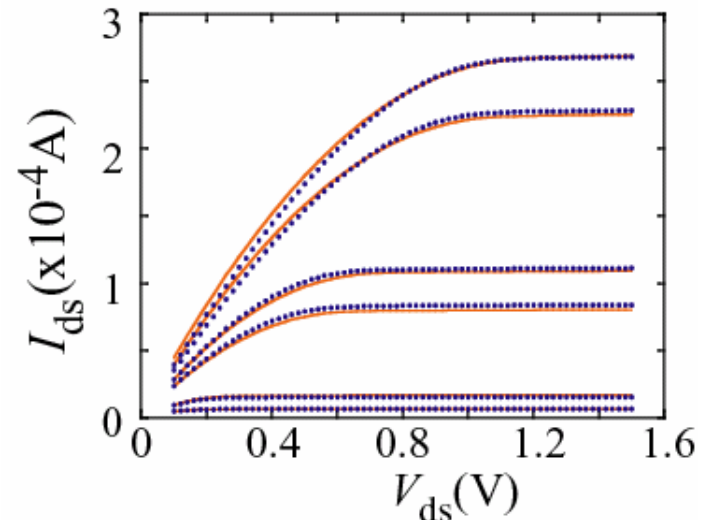
<Potential Distribution>



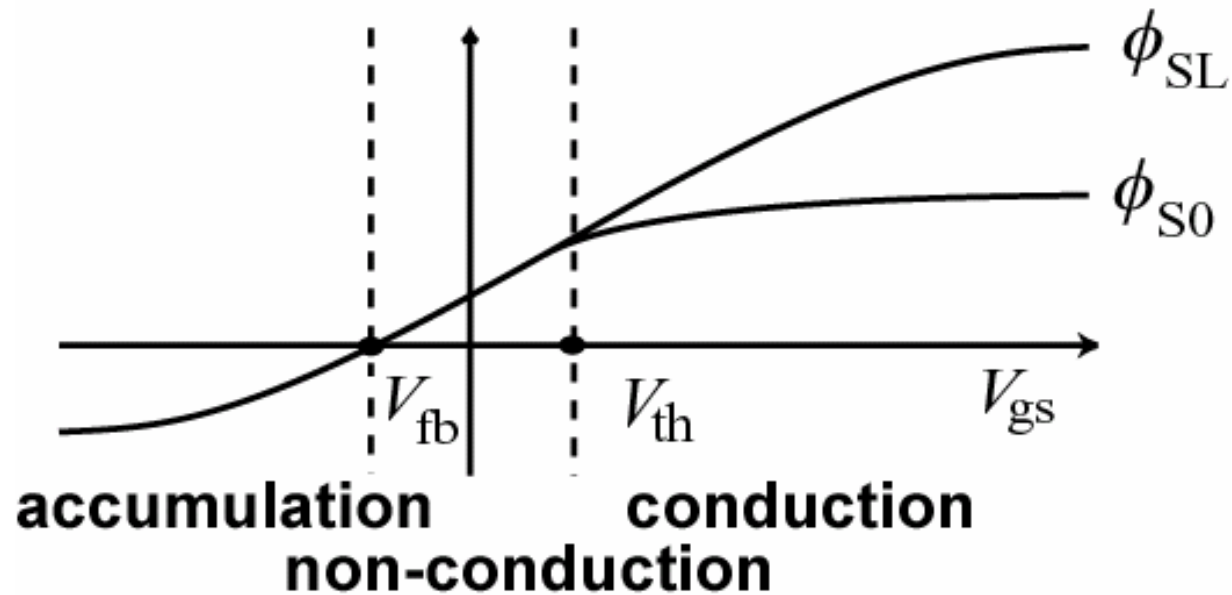
<Induced Charges>



<Device Characteristics>



Surface Potential is a Complicated Function of Applied Voltages



Surface-Potential Calculation

Solution of Poisson Equation:

$$C_{\text{ox}}(V_G' - \phi_S(y)) = \sqrt{\frac{2\epsilon_s q N_{\text{sub}}}{\beta}} \left[\exp\{-\beta(\phi_S(y) - V_{\text{bs}})\} + \beta(\phi_S(y) - V_{\text{bs}}) - 1 + \frac{n_{\text{p}0}}{p_{\text{p}0}} \left\{ \exp(\beta(\phi_S(y) - \phi_f(y))) - \exp(\beta(V_{\text{bs}} - \phi_f(y))) \right\} \right]^{\frac{1}{2}}$$

- ✧ **Exact Iterative Solution: HiSIM**
- ✧ **Approximate Analytical Solution: PSP**

Iteration does not Increase but Rather Decrease Simulation Time

- published already in Jan. 1996 (IEEE Trans. CAD/ICAS)
- A/D Converter: #Element=59723; #MOST=59432

	memory[kb]	# iteration	CPU time
HiSIM	124234	30624	20:58:46
BSIM3v3	197634	51678	21:01:29

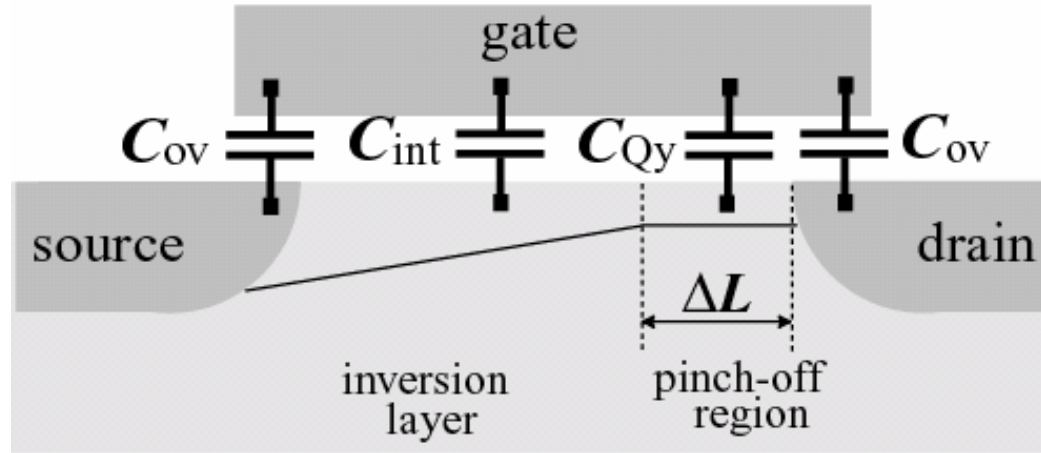
Why Surface-Potential-Based Modeling?

(1) Capacitances

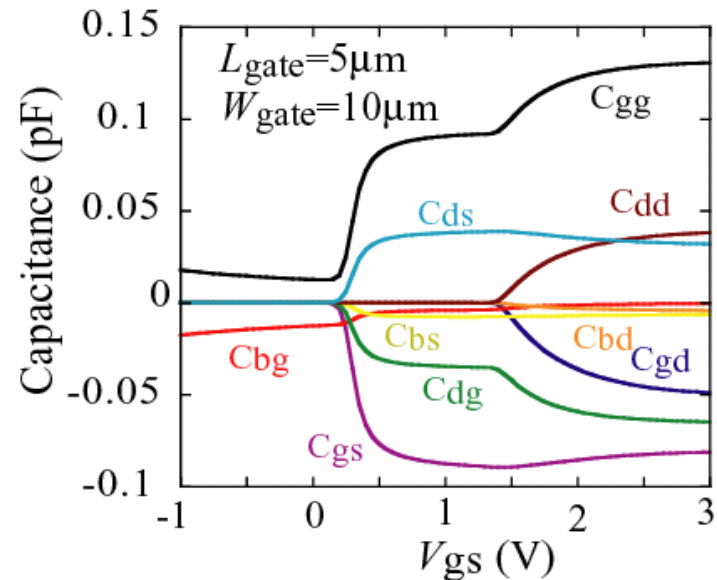
(2) Technology Variations

(3) Higher-Order Phenomena

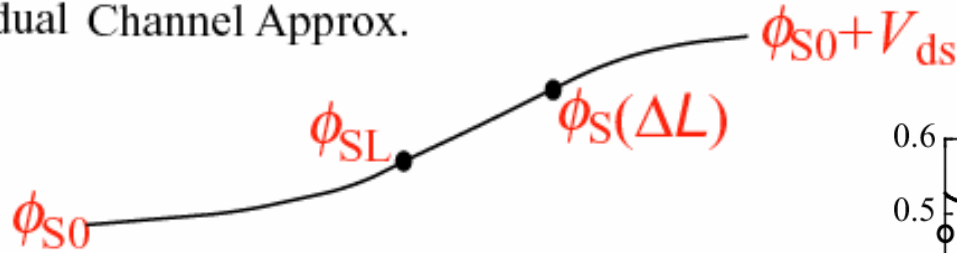
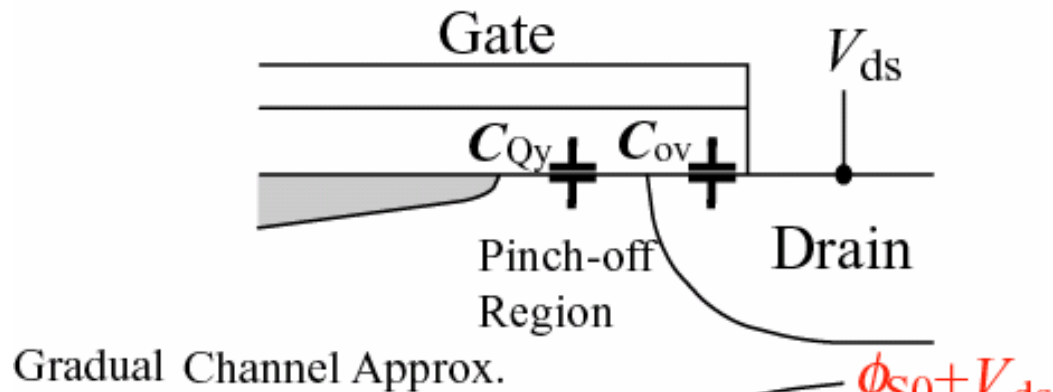
(1) Capacitances



**Intrinsic capacitances
are self-consistent
(no parameters)**

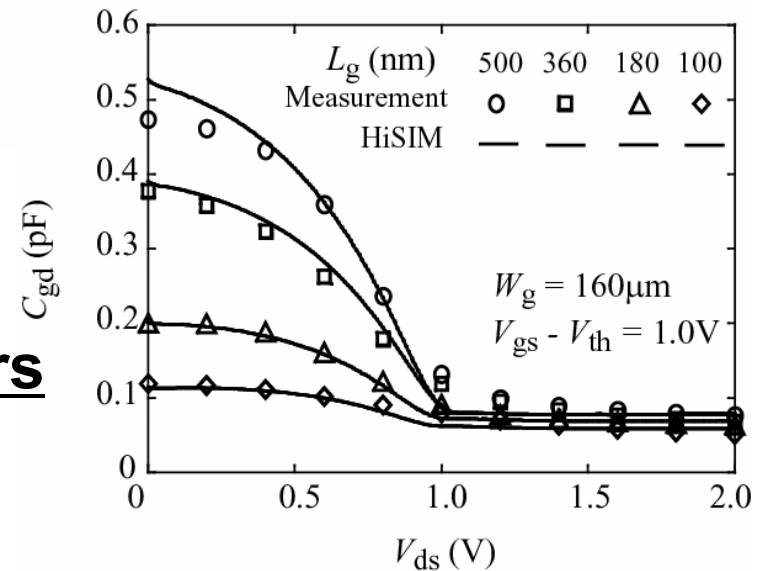


Capacitance Description Beyond the Pinch-off Point



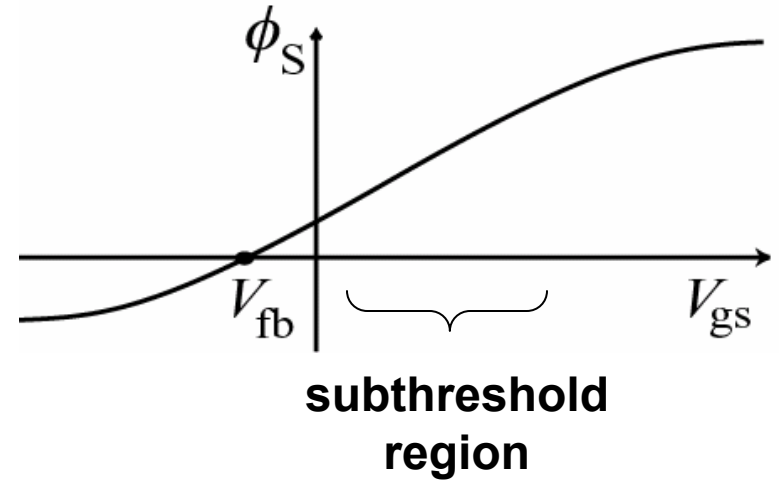
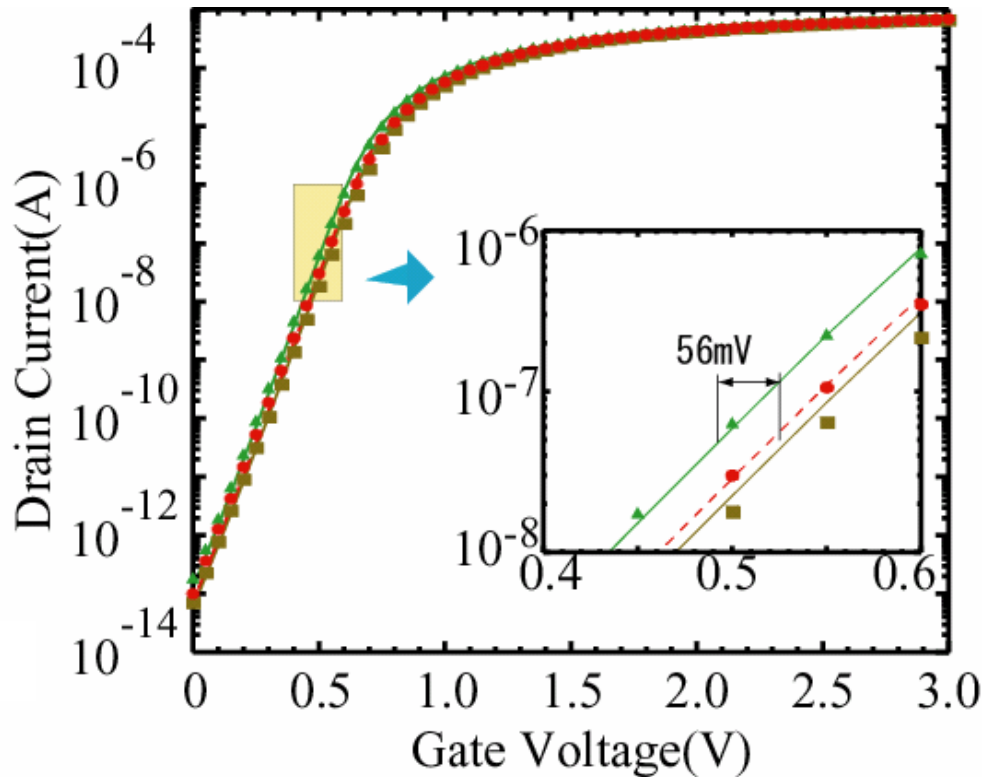
for short-channel transistors

$$C_{gd}(\text{total}) \approx C_{Qy} + C_{ov}$$



Potential distribution beyond the pinch-off point is a key for determining advanced MOSFET capacitances.

(2) Technology Variations



Subthreshold characteristics are sensitive to technology variations.

	ΔN_{sub}	$\Delta L_{gate}/0.6\mu m$
Inter	7%	6.7%
Intra	1%	3.8%

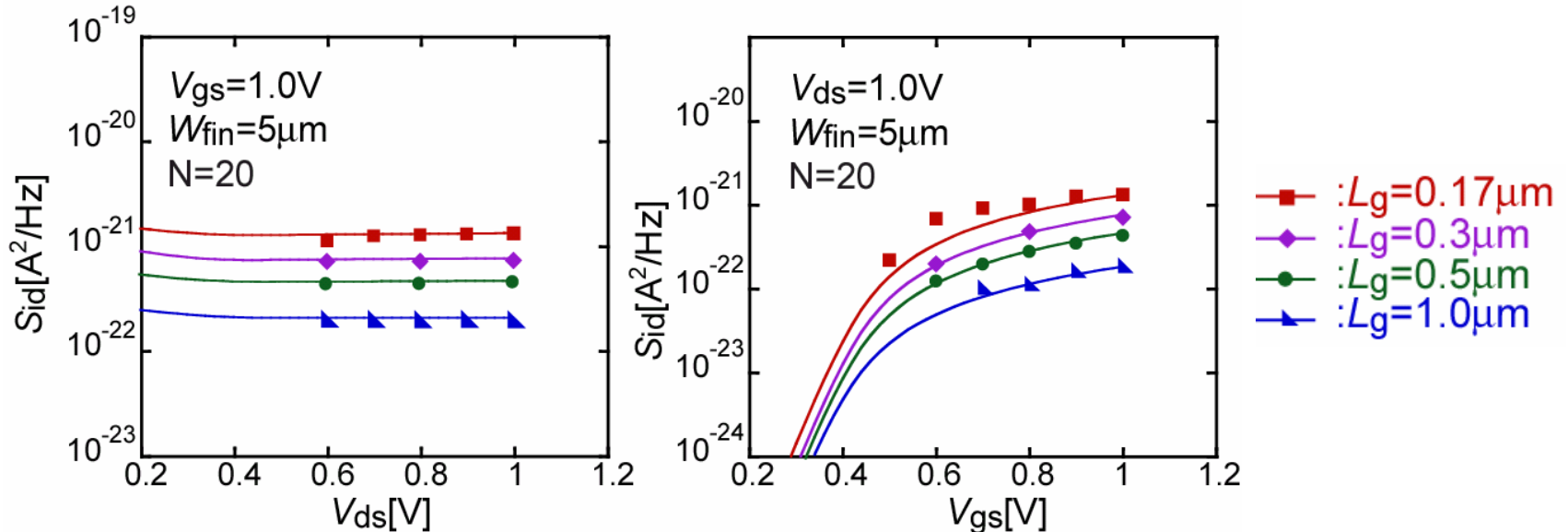
(3) Higher-Order Phenomena

**Thermal Noise: van der Ziel Description
based on Nyquist's Theorem**

$$S_{id} = \frac{4kT}{L_{eff}^2 I_{ds}} \int g_{ds}^2(y) dy$$

$g_{ds}(y)$: Channel Conductance
 g_{ds0} : at $V_{ds}=0$

Carrier distribution along the channel is required.



No additional fitting parameter required for surface-potential model