Surface-Potential-Based Modeling: Indispensable for Compact Models

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- Origin of MOSFET Behavior
  - Charges Induced on Nodes

- Origin of Induced Charges
  - Potential Distribution in the MOSFET
Surface Potential is the Basis for the Self-Consistent Modeling

\[ I_{ds} = q \frac{W}{L} \int vQ_{idy} \]

\[ Q_b(y) = -qN_{sub} \times W_d = -\sqrt{\frac{2\varepsilon_s qN_{sub}}{\beta}} \left\{ \beta \left( \phi_s(y) - V_{bs} \right) - 1 \right\}^{-\frac{1}{2}} \]

\[ \phi_s: \text{surface potential} \]
Surface-Potential Distribution Reflects Technology Dependence

Impurity Profile with Pocket Implant

Calculated Potential Distribution

Surface-Potential Distribution
Schematic Relationship

<Device>
Gate
Source
Drain

<Potential Distribution>

<Induced Charges>

<Device Characteristics>

\[ \phi_{S0} \]

\[ \phi_{SL} \]

\[ Q_x (10^{-12} \text{ C}) \]

\[ V_{gs} (\text{V}) \]

\[ I_{ds} (\times 10^{-4} \text{A}) \]

\[ V_{ds} (\text{V}) \]
Surface Potential is a Complicated Function of Applied Voltages
Surface-Potential Calculation

Solution of Poisson Equation:

\[ C_{ox}(V'_G - \phi_S(y)) = \sqrt{\frac{2\varepsilon_s q N_{sub}}{\beta}} \left[ \exp\left\{-\beta(\phi_s(y) - V_{bs})\right\} + \beta(\phi_s(y) - V_{bs}) - 1 \right. \\
\left. + \frac{n_{p0}}{p_{p0}} \left\{ \exp\left(\beta(\phi_s(y) - \phi_f(y))\right) - \exp\left(\beta(V_{bs} - \phi_f(y))\right) \right\} \right]^\frac{1}{2} \]

✧ Exact Iterative Solution: HiSIM
✧ Approximate Analytical Solution: PSP
Iteration does not Increase but Rather Decrease Simulation Time


- A/D Converter: #Element=59723; #MOST=59432

<table>
<thead>
<tr>
<th></th>
<th>memory[kb]</th>
<th># iteration</th>
<th>CPU time</th>
</tr>
</thead>
<tbody>
<tr>
<td>HiSIM</td>
<td>124234</td>
<td>30624</td>
<td>20:58:46</td>
</tr>
<tr>
<td>BSIM3v3</td>
<td>197634</td>
<td>51678</td>
<td>21:01:29</td>
</tr>
</tbody>
</table>
Why Surface-Potential-Based Modeling?

(1) Capacitances
(2) Technology Variations
(3) Higher-Order Phenomena
(1) Capacitances

Intrinsic capacitances are self-consistent (no parameters)
Capacitance Description Beyond the Pinch-off Point

for short-channel transistors

\[ C_{gd} \text{ (total)} \approx C_{Qy} + C_{ov} \]

Potential distribution beyond the pinch-off point is a key for determining advanced MOSFET capacitances.
Subthreshold characteristics are sensitive to technology variations.

<table>
<thead>
<tr>
<th></th>
<th>$\Delta N_{\text{sub}}$</th>
<th>$\Delta L_{\text{gate/0.6um}}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>Inter</td>
<td>7%</td>
<td>6.7%</td>
</tr>
<tr>
<td>Intra</td>
<td>1%</td>
<td>3.8%</td>
</tr>
</tbody>
</table>
(3) Higher-Order Phenomena

Thermal Noise: van der Ziel Description
based on Nyquist's Theorem

\[ S_{id} = \frac{4kT}{L_{\text{eff}}^2} \int g_{ds}(y)dy \]

\[ g_{ds}(y): \text{Channel Conductance} \]

\[ g_{ds0}: \text{at } V_{ds}=0 \]

Carrier distribution along the channel is required.

No additional fitting parameter required for surface-potential model