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# Modeling Snapback and Rise-Time Effects in TLP Testing for ESD MOS Devices Using BSIM3 and VBIC Models

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# Outline

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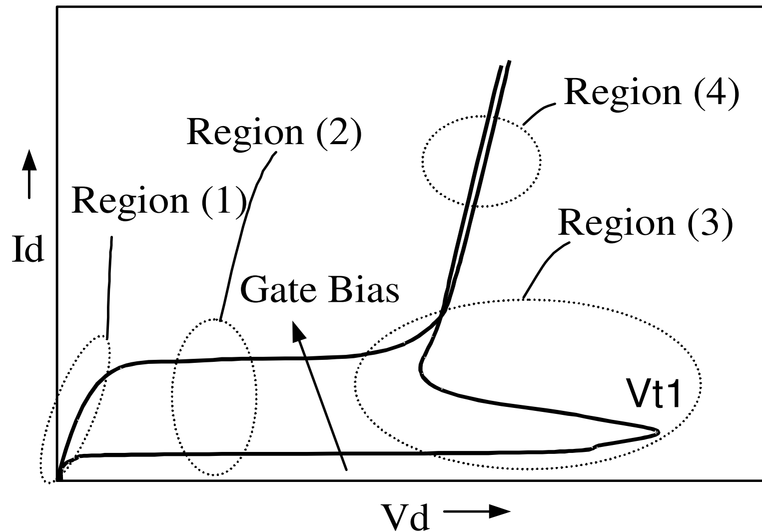
# Research Motivation

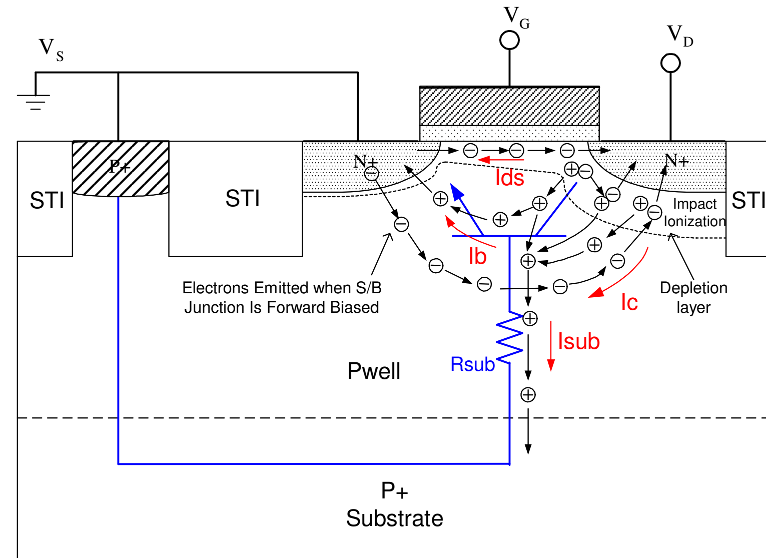
- ESD Is a Major IC Reliability Concern: Responsible for 30%~50% Customer Returns
- Accurate SPICE Models for Integrated ESD Simulation Can Reduce ESD Design Iteration
- MOSFETs in Snapback Operation Mode Are Widely Used as ESD Protection in CMOS Technology
- Rise Time of ESD Pulse Has Significant Impact on Performance of MOS ESD Protection
- A Practical SPICE Macro Model for Snapback of ESD MOS Devices is Needed and Good Understanding on the Rise Time Effect is Helpful.

# Snapback in MOS Devices

- Four Regions in I-V Curve
  - (1) Linear Region
  - (2) Saturation Region
  - (3) Avalanche Region
  - (4) Snapback Region



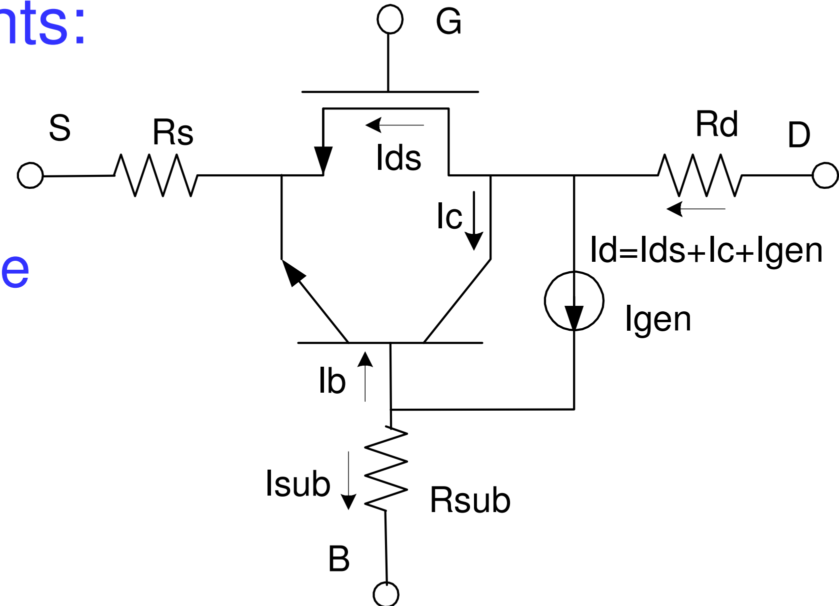

- Snapback due to Parasitic NPN
  - Holes Created by Impact Ionization in D/B Depletion Layer Are Injected Into Substrate
  - Parasitic NPN turns on when voltage drop cross Rsub ( Vbe of BJT) (Isub×Rsub) reaches ~0.7V



# Previous MOS Snapback Models(1)

- Numerical SPICE Models Have Been Publicly Reported

- Four Essential Components:
  - Main MOS
  - Parasitic BJT
  - Avalanche Current Source
  - Substrate Resistor




- The BJT Is Modeled
  With EM or GP Models

# Previous MOS Snapback Models(2)

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- The Explicit Current Source Is Given by

$$Igen = (M-1)\cdot(Ids + Ic)$$

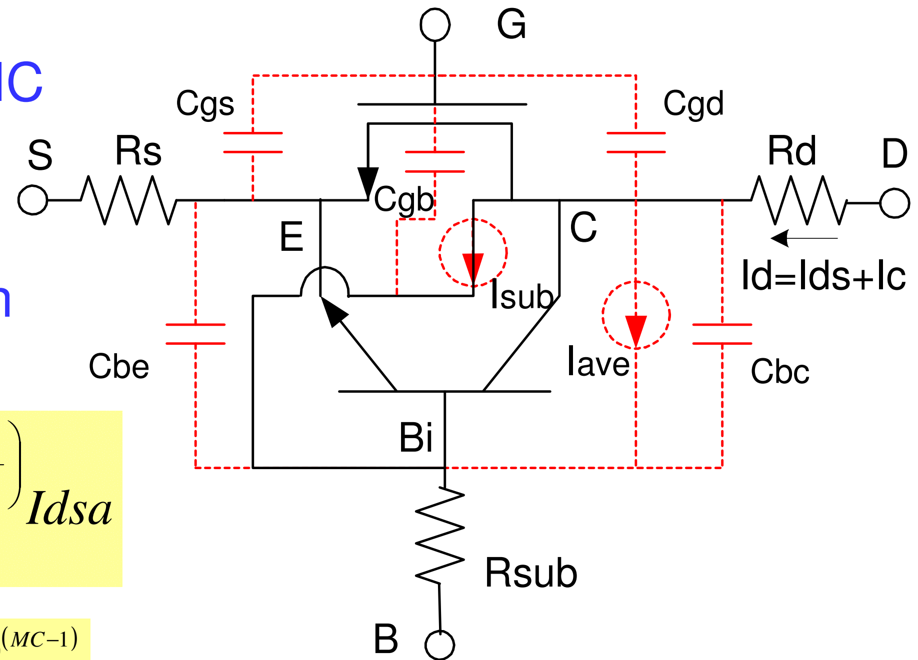
where M is multiplication fact, given by Miller formula

$$M = \frac{1}{1 - K1\cdot\exp\left(-\frac{K2}{Vd - Vdsat}\right)}$$ or $$M = \exp\left[k1(Vd - Vdsat - d1)\right] + \exp\left[k2(Vd - Vdsat - d2)\right]$$

- The Models Are Implemented either in Proprietary SPICE, or Using Behavior Language Verilog-A or VHDL-A
- The Verilog-A Models Can Have Low Simulation Speed and May Cause Serious Convergence Problems
- Proprietary SPICE Has Limited Accessibility to Designers and Needs Extra Support

# Macro Model Using BSIM3 and VBIC

- Our New Macro Model Structure Includes Three Main Components:
  - NMOS modeled by BSIM3
  - Parasitical NPN modeled by VBIC
  - Substrate resistance
- The Impact Ionization Current or Avalanche Current Source Is Built in BSIM3 and VBIC Models




$$Isub = \left(\alpha 1 + \frac{\alpha 0}{Leff}\right) \cdot (Vds - Vdeff) \cdot e^{\left(-\frac{\beta 0}{Vds - Vdeff}\right)} Idsa$$

$$Iave = Ic \cdot AVC1 \cdot (PC - Vbci) \cdot e^{-AVC2 \cdot (PC - Vbci)^{(MC-1)}}$$

- Equivalently, We Have

$Igen = Isub + Iave$ similar to $M = \exp[k1(Vd - Vdsat - d1)] + \exp[k2(Vd - Vdsat - d2)]$

# Advantages of New Snapback Macro Model

- Simple Structure and Strong Capability
  - Standard components only and no external current source
  - Partially decoupled substrate current for BJT and intrinsic MOS
  - Transient simulation capability from sophisticated capacitance modeling in BSIM3 and VBIC
  - High simulation speed since no Verilog-A or VHDL-A involved
  - Less convergence issues due to no Verilog-A and fine-tuned algorithms of BSIM3 and VBIC
  - VBIC offers simulation capability for self-heating effect
- A Practical Approach: Easy to Implement and Use
  - No need using behavior languages (Verilog-A, …)
  - No need for special SPICE implementation by individual Users
  - The availability is high since both BSIM3 and VBIC are widely included in various simulators.
  - CAD environment is compatible to non ESD models

# Simulation of Snapback and Rise Time Effect

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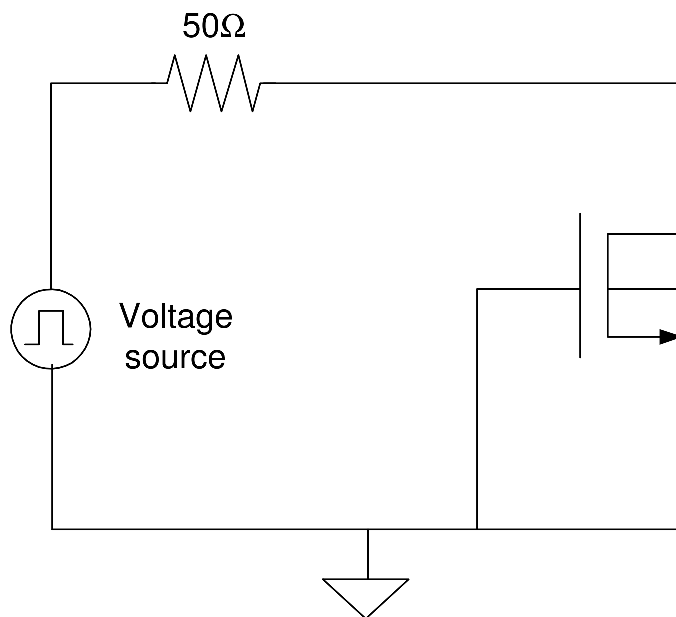
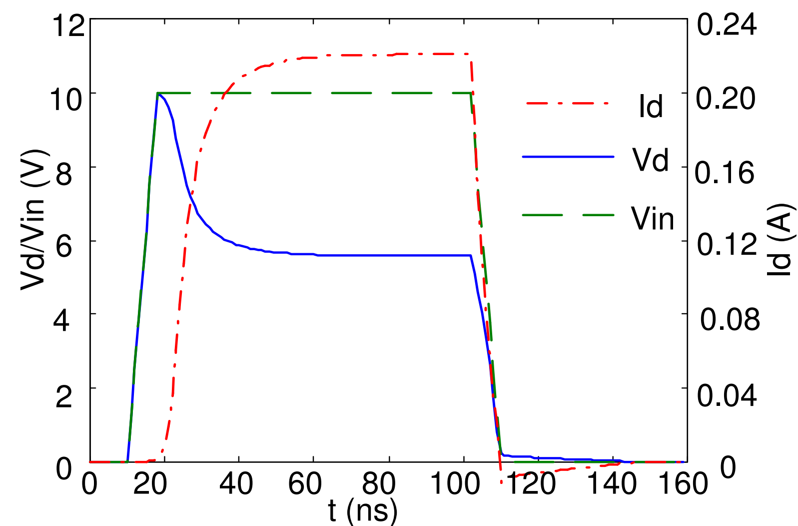
- Snapback was simulated with transient simulation using schematic below
- Voltage pulse sequences with varied rise time were used as the input
- The stabilized Vd and Id were measured as the simulation results




Schematic of TLP Simulation for ggNMOS




Input voltage *Vin*, drain voltage *Vd* and drain current *Id* vs. time *t* in a single pulse

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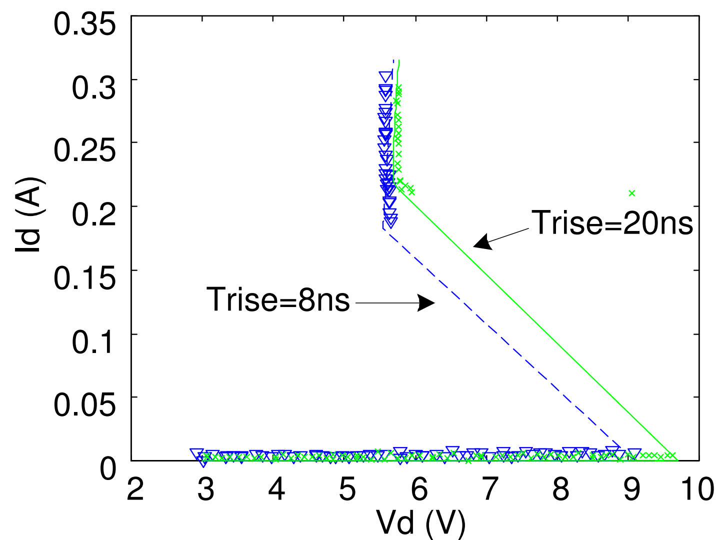
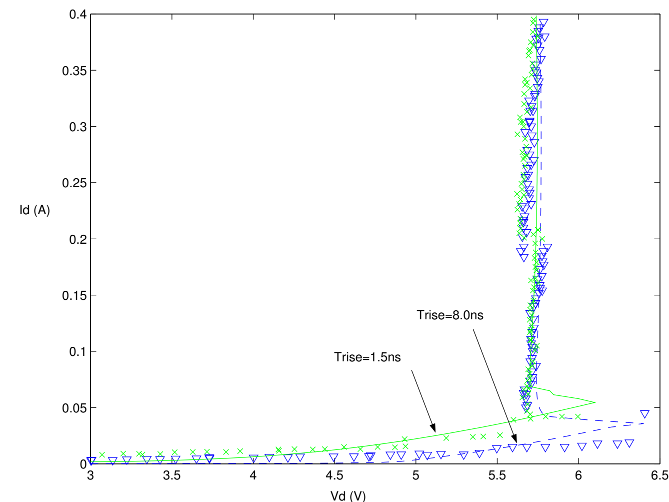
# Results and Discussions(1): Snapback Curves

- Snapback curves demonstrate that trigger voltage Vt1 decreases as the rise time of the input pulse is reduced
- The dependence of Vt1 on the rise time was observed in ggNMOS and gcNMOS configurations



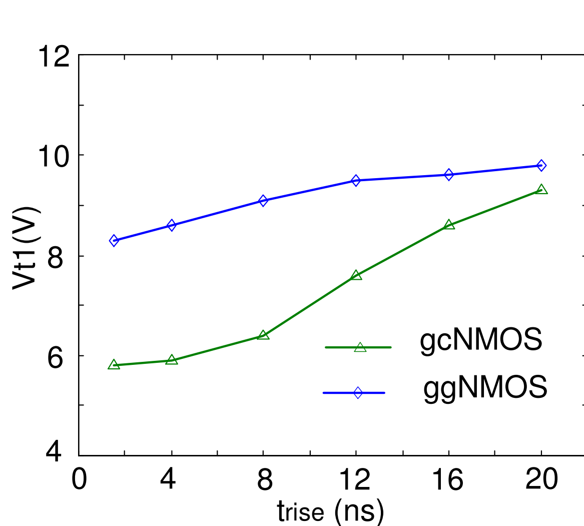

**Snapback curves of a ggNMOS structure (lines: simulation, symbols: measurement)**



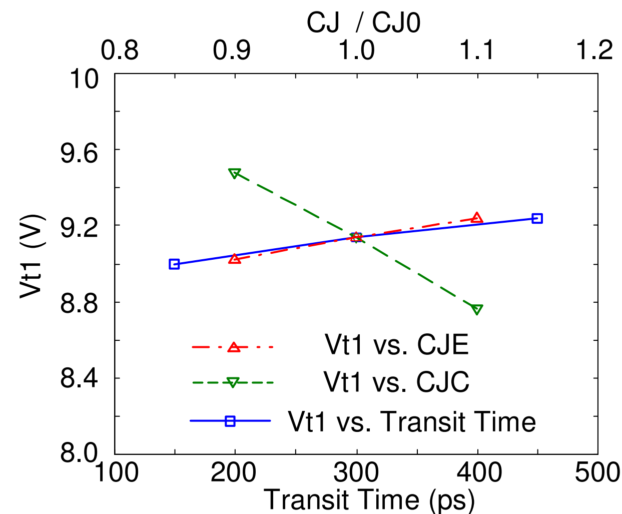

**Snapback curves of a NMOS with a 10k resistor between gate and ground (lines: simulation, symbols: measurement)**

# Results and Discussions(2): Trigger Voltage Vt1

- Vt1 of gcNMOS was observed much more sensitive to the rise time than Vt1 of ggNMOS
- Sensitivity simulation indicates that the overlap capacitance has no impact at all on Vt1 for ggNMOS but cause most variation for gcNMOS
- Vt1 for ggNMOS is affected by junction capacitance and transit time




**_Vt1_ vs. rise time for ggNMOS and gcNMOS observed in measurement**




**_Vt1_ vs. CJC and $t_F$ in a ggNMOS (Trise=8ns)**

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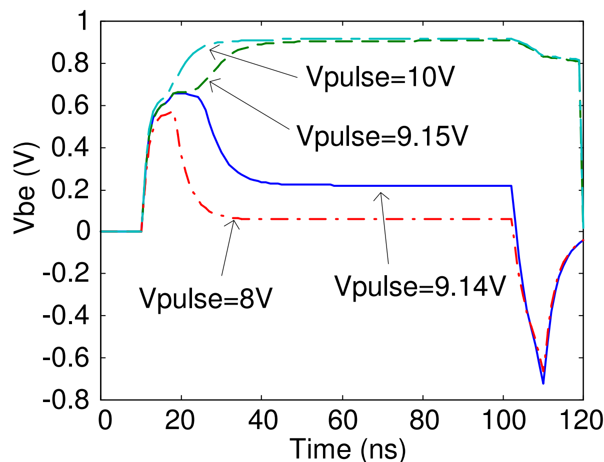
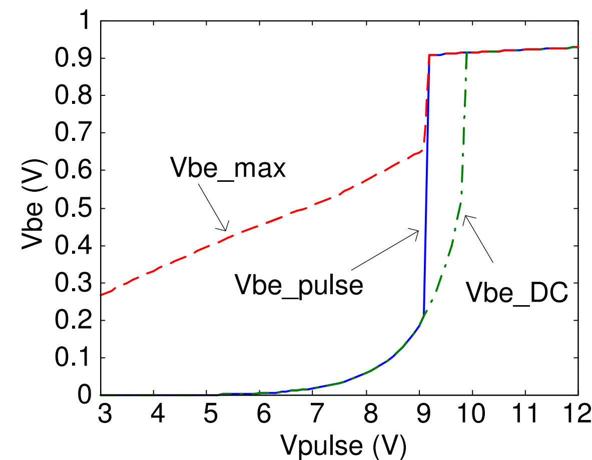
# Results and Discussions(3): Vbe Spike under ESD Pulse

- Vgs>0 due to gate coupling is the well-known cause of Vt1 drop in gcNMOS
- Vbe of NPN shows a spike at rising edge of input voltage pulse
- Vbe may drop back to a stabilized value or continue increasing. The dividing point is corresponding to the trigger voltage




**Vbe vs. Time in a single pulse for a ggNMOS**




***Vbe* vs. ESD stress voltage in transient (*Vbe_pulse* and *Vbe_max*) and quasi-static (*Vbe_DC*) events for ggNMOS**

# Results and Discussions (4)

- Displacement current through the Drain/Bulk junction causes a Vbe spike in the parasitic NPN in ggNMOS.
- Avalanche current in Drain/Bulk junction is enhanced by the Vbe spike, which eventually results in a lower trigger Vt1.
- Higher CJC and shorter rise time (higher dV/dt) cause bigger Vt1 reduction.
- It is important to properly model the Drain/Bulk junction capacitance as well the Source/Bulk junction capacitance and the base transmit time to achieve accurate simulation for the trigger voltage of ggNMOS snapback.
- For NMOS with a resistor between gate and drain, Drain/Gate overlap capacitance is the dominant parameter Vt1 dependence on rise time

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# Conclusion

- A unique macro model structure for snapback simulation of ESD MOS devices has been developed
- The model takes the advantage of built-in formulas and fine-tuned algorithms in sophisticated BSIM3v3 and VBIC models
- It offers advantages of high simulation speed, wider accessibility, and less convergence issues
- The model has been used for investigation of Vt1 dependence on the rise time of transmission line pulse (TLP)
- The simulation demonstrated that the $t_f$ and junction capacitance of parasitic BJT have impact on Vt1 even for ggNMOS
- The cause of Vt1 drop in ggNMOS is the displacement current due to dV/dt in TLP pulses