

Device Parameter Extraction from Fabricated Double-Gate MOSFETs

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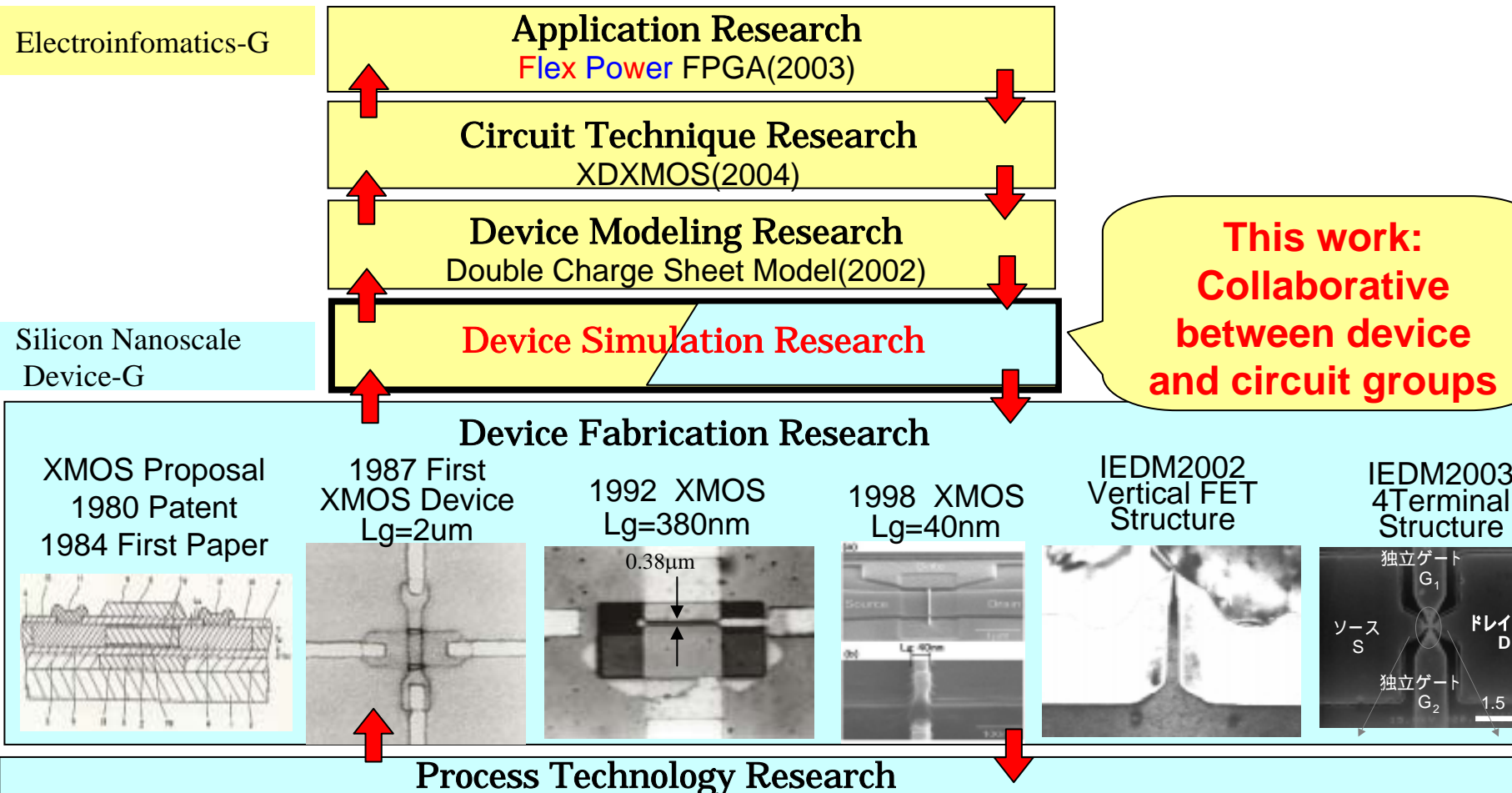
Outline

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 - 2. Source/drain Resistance Approximation**
 - 3. Step Doping Profile Approximation**
 - 4. Simple Device Simulation Model**
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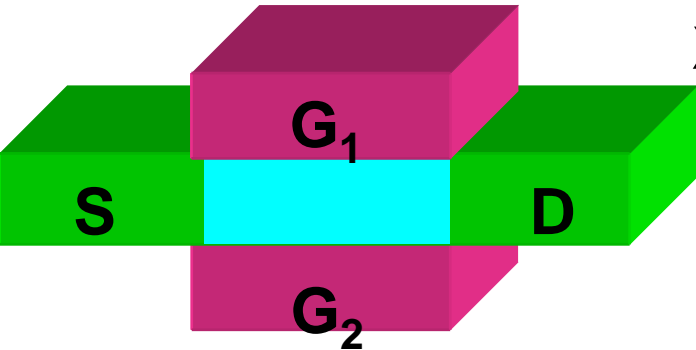


AIST Vertically Integrated Advanced Device Researches and Developments Environment

● AIST has a DG-MOSFETs-oriented Research Hierarchy.



XMOS also known as DG-MOSFET



XMOS* a.k.a Double-Gate MOSFET

T.Sekigawa et al., Solid-State Electronics, 1984.

* He first proposed a Double-Gate structured MOSFET and he named it XMOS.

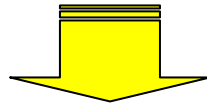
Advantages:

- (1) Short-channel effect immunity.
- (2) Double current drivability.
- (3) Ideal S-slope.

But, there is only one disadvantage.

Motivation

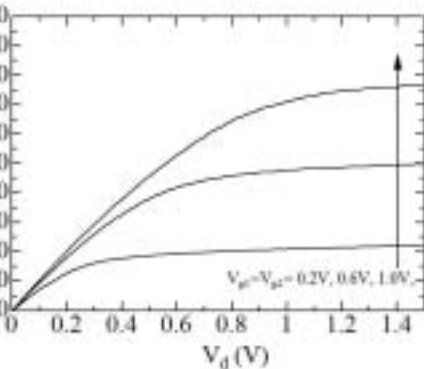
- It is difficult to fabricate a desired DG-MOSFET with good characteristics.
- As a result, it is difficult to make an actually well-matched DG-MOSFET compact model.



- We have successfully fabricated such an excellent DG-MOSFET already. (IEDM2003).
- Therefore, for the development of DG-MOSFET compact model, we have tried how to simplify its DG-MOSFET device simulation model in accordance with the fabricated device measurement.

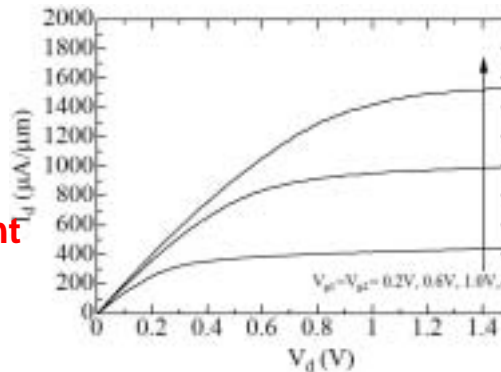
Methodology of Fabrication-based SPICE Model Development

Device Measurement



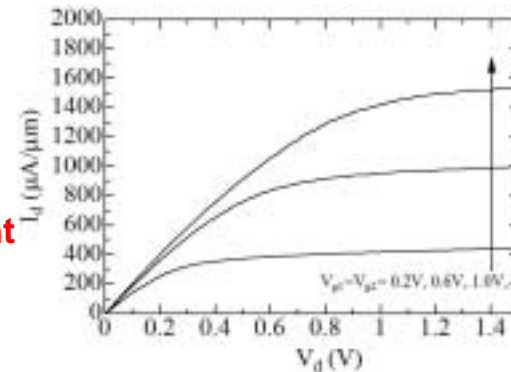
agreement

Device Simulation



agreement

SPICE Simulation



Fabricated DG-MOSGET

Conventional Device Simulation model

SPICE simulation model (Device Compact Model)

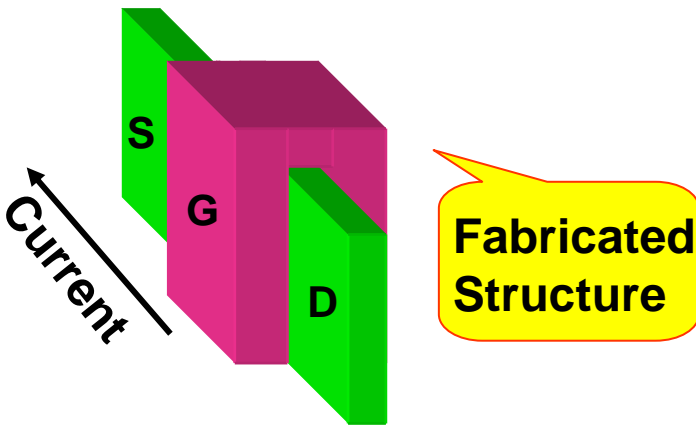
Simplification maintaining accuracy

Simple Device Simulation model

The Simplification of device simulation model strongly contributes to the development of accurate well-matched DG-MOSFET SPICE simulation model

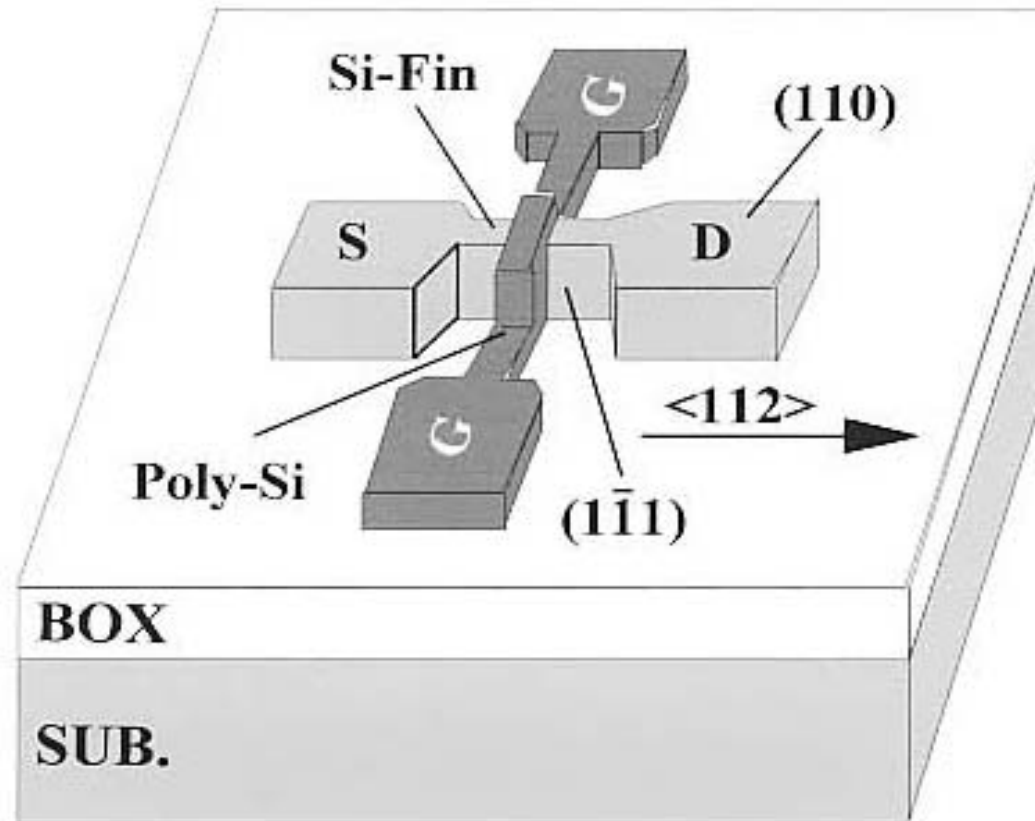


Fabricated Fin-type DG-MOSFET Structure



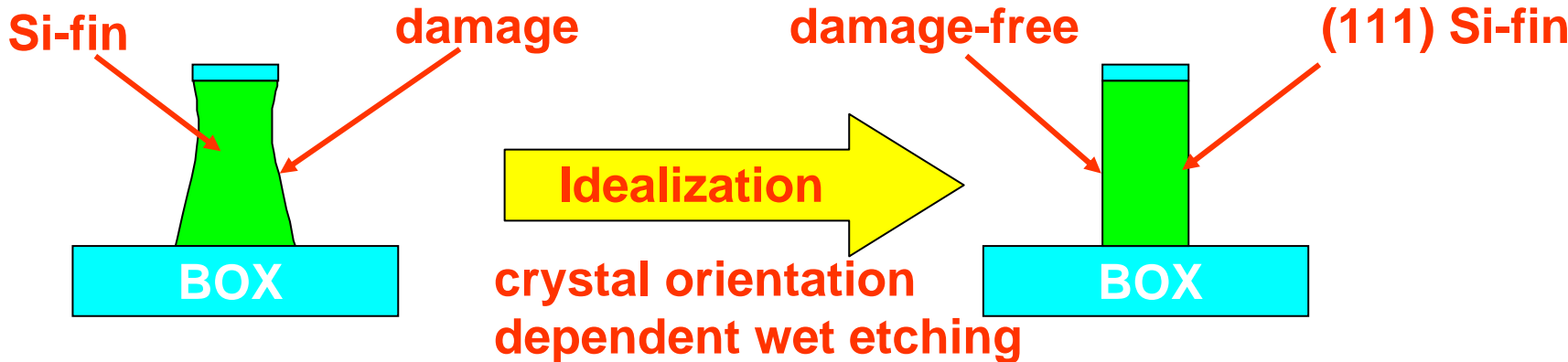
(a) Fin-type X MOS

Key issue is ultra-thin and uniform Si-fin channel fabrication.



(b) Design of DG-MOSFET crystal orientation

Si-fin Fabrication by Wet Etching



(a) Bell-shaped Si-fin by Reactive Ion Etching (Conventional)

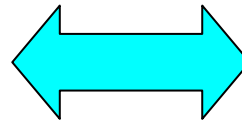
(b) Ideal rectangular Si-fin by wet etching (This work)

Issues

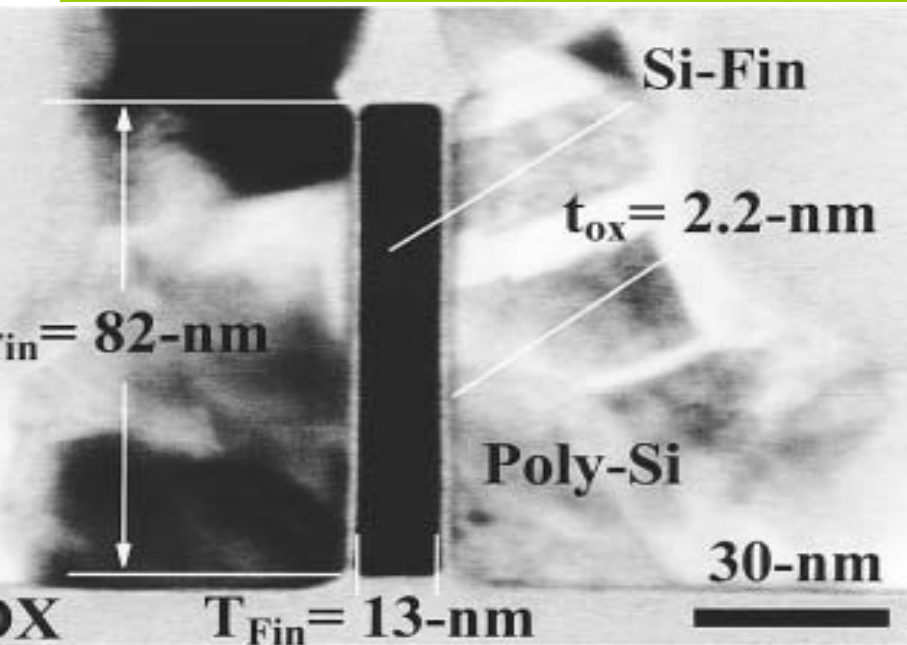
- (1) Damage
- (2) Non-uniform
- (3) Non-ultra-thin

Advantages

- (1) Damage-free
- (2) Uniform
- (3) Ultra-thin

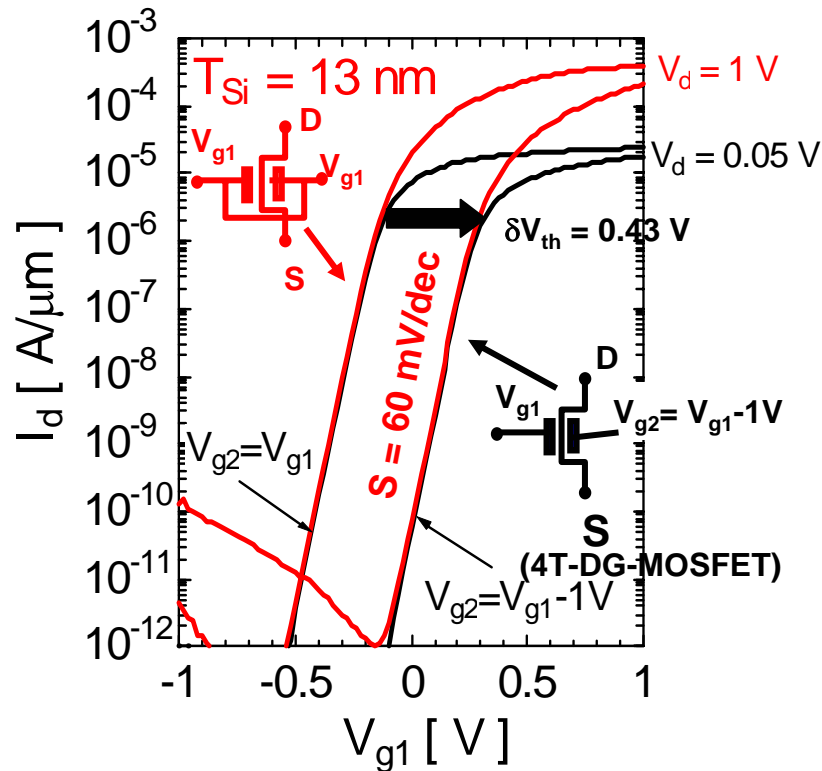


Fabricated 105-nm DG-MOSFET Photography and Characteristics



Fabricated DG-MOSFET channel XTEM image

Ultra-thin and ideal rectangular cross-sectional channel is successfully formed. This ideal channel leads to good characteristics with excellent S-slope



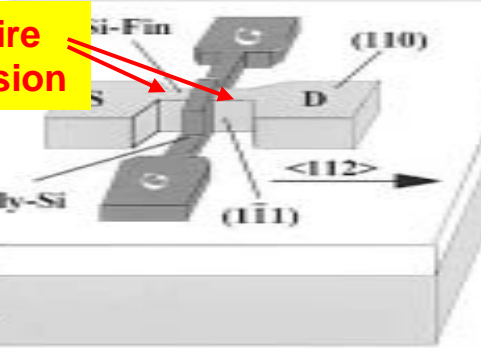
- ✓ Good characteristics with excellent S-slope $S=60\text{mV/dec}$.
- ✓ In 4T-DG-MOSFET, optimum V_{th} control is realized maintaining the excellent S-slope. (DRC2004)

Methodology of Device Simulation Model Simplification

Device Measurement



Device Simulation (Silvaco's ATLAS)



Fabricated 3-terminal DG-MOSFET structure

1

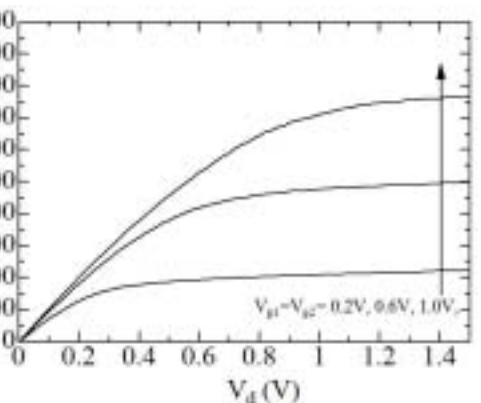
For obtaining device simulation parameters, Silvaco's automatic parameter fitting tool OPTIMIZER is employed.

Conventional Device Simulation Model A
(Gaussian doping profile model with source/drain extension)
with real device structure sizes and fabricated process conditions

Optimization of a Gaussian doping profile parameters

2

For simplifying the device simulation model, two approximations are applied to the conventional device simulation model, maintaining good agreement with device measurement.



(b) Real device characteristics

Source/drain Resistance Approximation Model B

Extraction of R_s and R_d

Step Doping Profile Approximation Model C

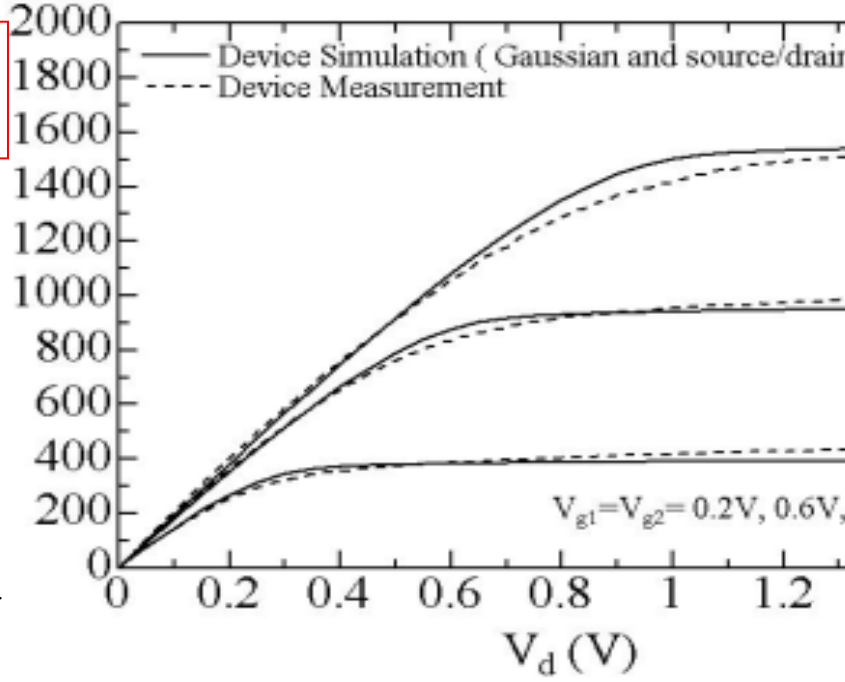
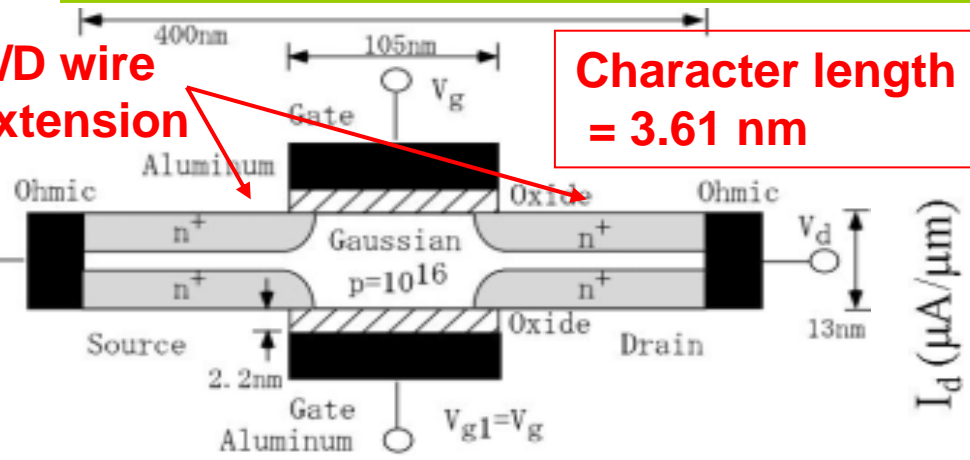
Extraction of N_a and L_{ov}

Unify two models using the extracted R_s , R_d , N_a , and L_{ov}

Simple Device Simulation Model D
(Step doping approximated Model with Source/drain resistance)



Conventional Device Simulation Model A



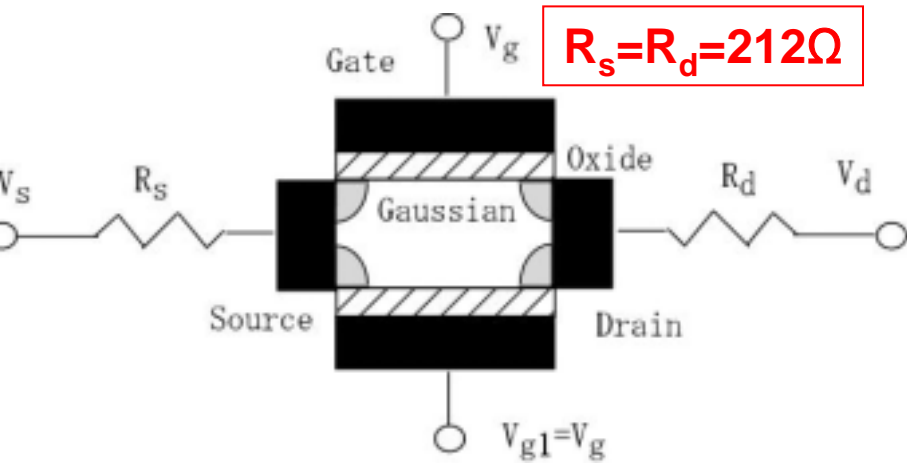
(a) Conventional Device Simulation Model A (Optimization of a Gaussian doping profile shape parameter)

Good agreement is obtained by fitting only a character length of Gaussian doping profile, even in the 105-nm DG-MOSFET.

(b) Comparison of characteristics between device measurement and device simulation (Conventional Device Simulation Model A)

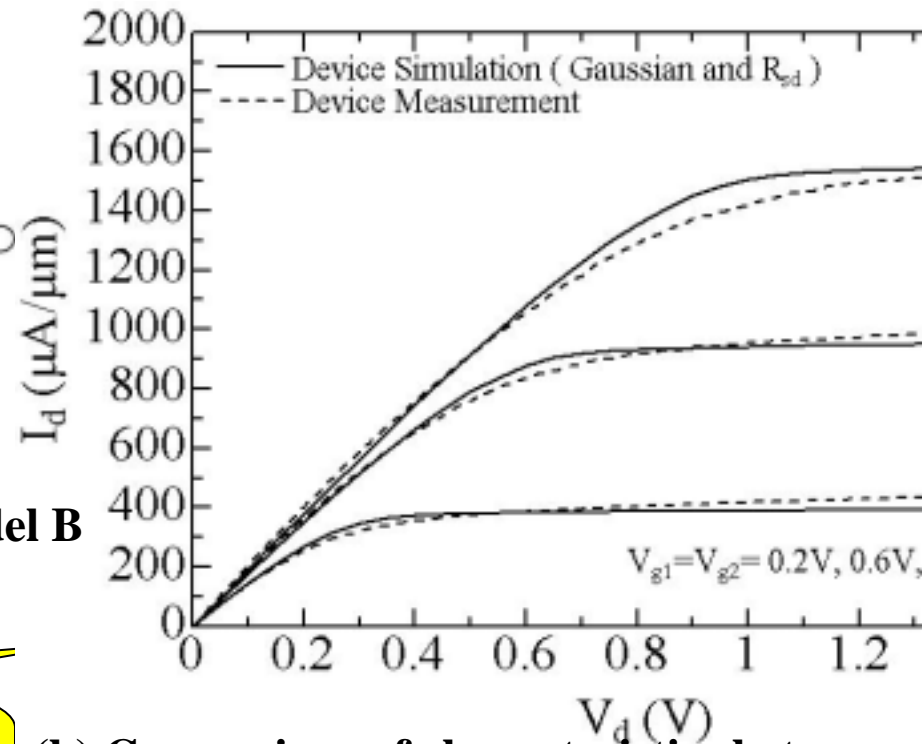


Source/drain Resistance Approximation Model B



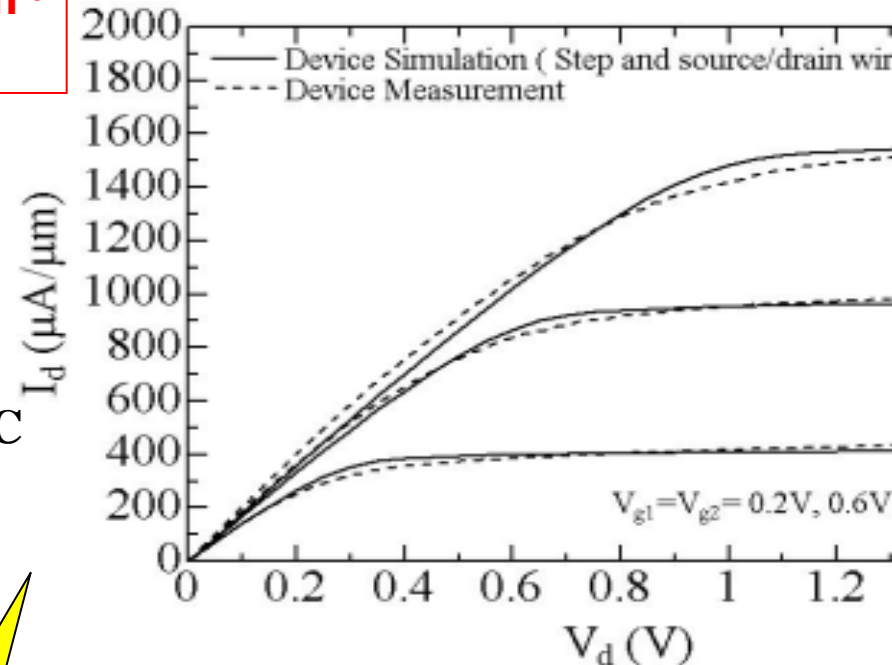
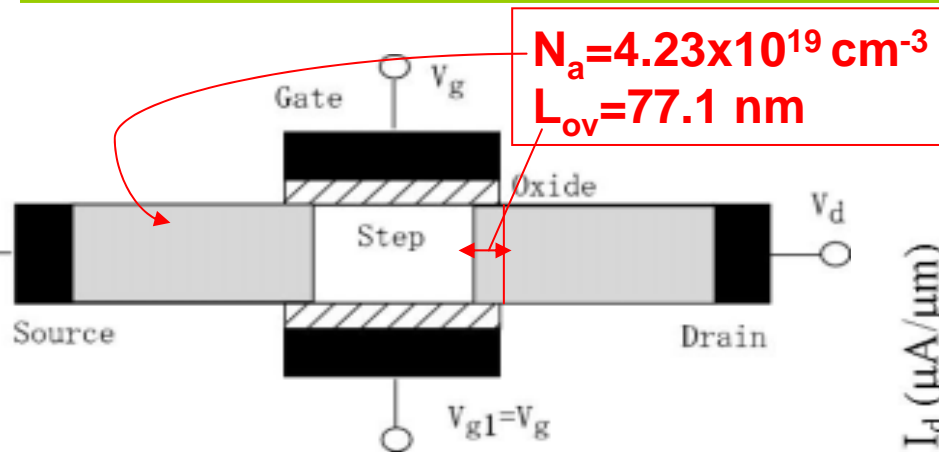
Source/drain Resistance approximation Model B
(Extraction of S/D Resistance)

Good agreement indicates that S/D wire extension is considered as a linear S/D resistance.



(b) Comparison of characteristics between device measurement and device simulation (S/D Resistance Approximation Model B)

Step Doping Profile Approximation Model C

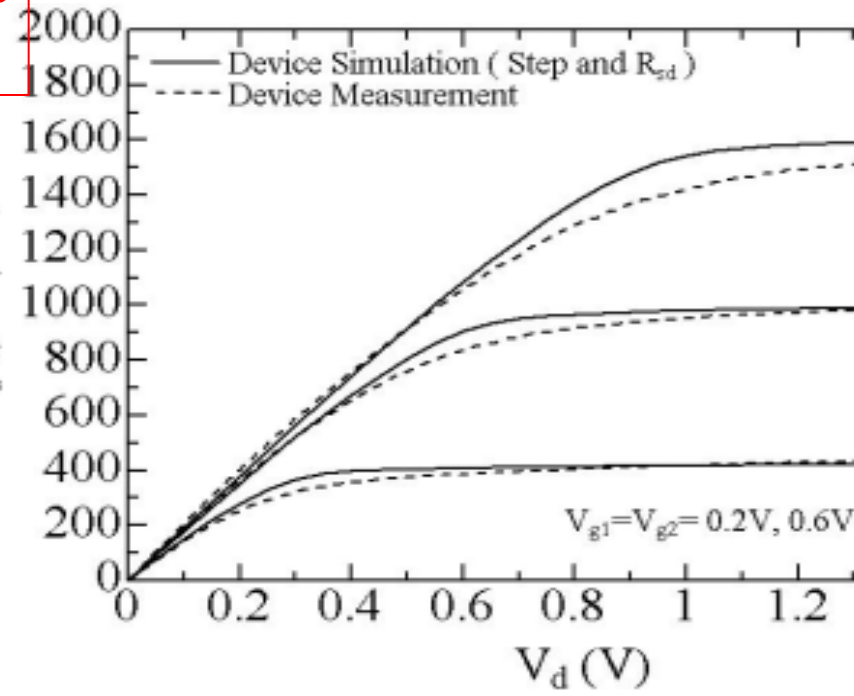
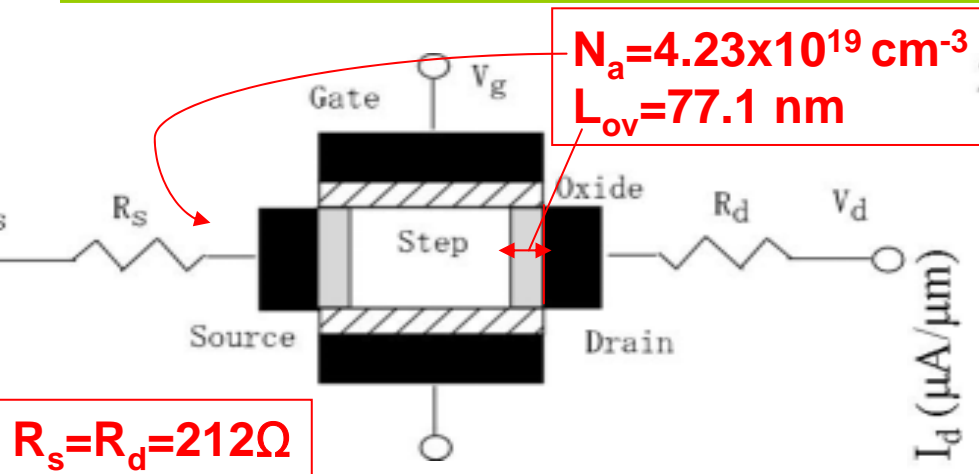


Step Doping Profile Approximation Model C
 (Extraction of step doping profile parameter)

Step Doping Model C can approximate
 device measurement fairly well.
 This indicates that the barrier height
 near source edge is not affected so
 much by drain potential, because of
 CE immunity effect.

(b) Comparison of characteristics between
 device measurement and device simulation
 (Step Doping Profile Approximation Model C)

Simple Device Simulation Model D



(a) Simple Device Simulation Model D (Application of R_s , R_d and N_a , L_{ov})

Good agreement indicates that S/D wire extension and Gaussian doping profile can be simultaneously approximated to S/D resistance and step doping profile respectively, even a 100-nm-size DG-MOSFET.

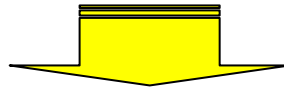
(b) Comparison of characteristics between device measurement and device simulation (Simple Device Simulation Model D).



Summary

Good agreement between device simulation and device measurement of the fabricated 105-nm DG-MOSFET has been obtained for the first time, by fitting only the shape parameter of Gaussian doping profile of the conventional device simulation model.

It is experimentally confirmed that 100-nm-size DG-MOSFET simulation device model can be simplified to step junction model separated by source/drain resistance. **This simplification is useful for SPICE model.**



DG-MOSFET is suitable for simplification of device simulation model due to the immunity of SCE.

DG-MOSFET source/drain extension can be separately considered as R_s / R_d .

Step doping profile can be applicable for DG-MOSFET spice model.

