

An A Priori Hysteresis Modeling Methodology for Improved Efficiency and Model Accuracy in Advanced PD SOI Technologies

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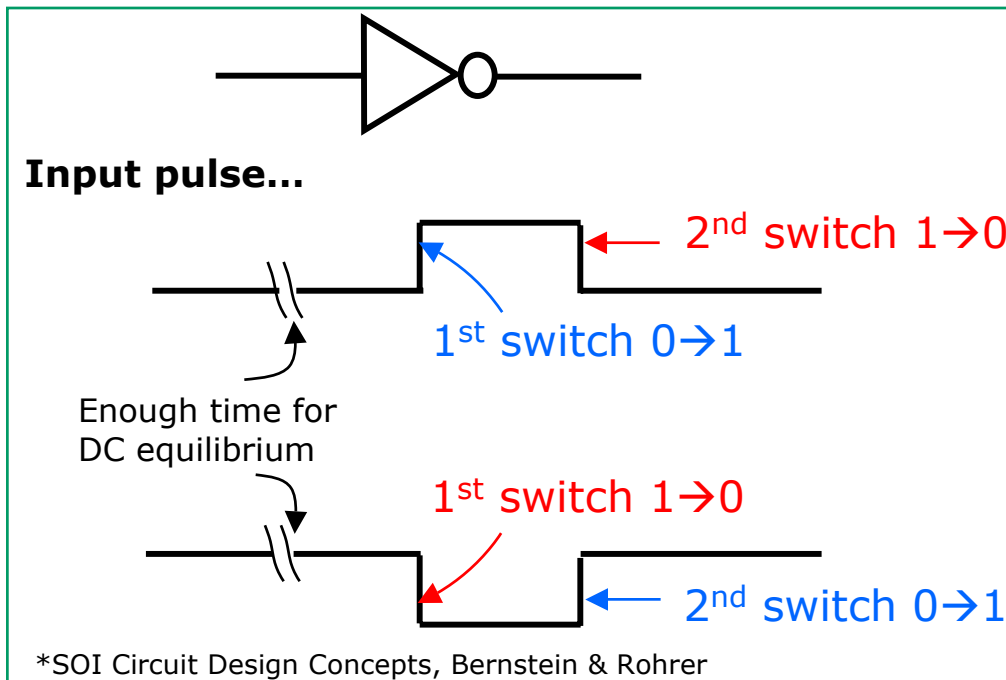
History Effect (Hysteresis) in Partially Depleted (PD) SOI Circuits



- History effect: dependence of propagation delay on the pre-switch state of the logic gate using floating-body (FB) devices

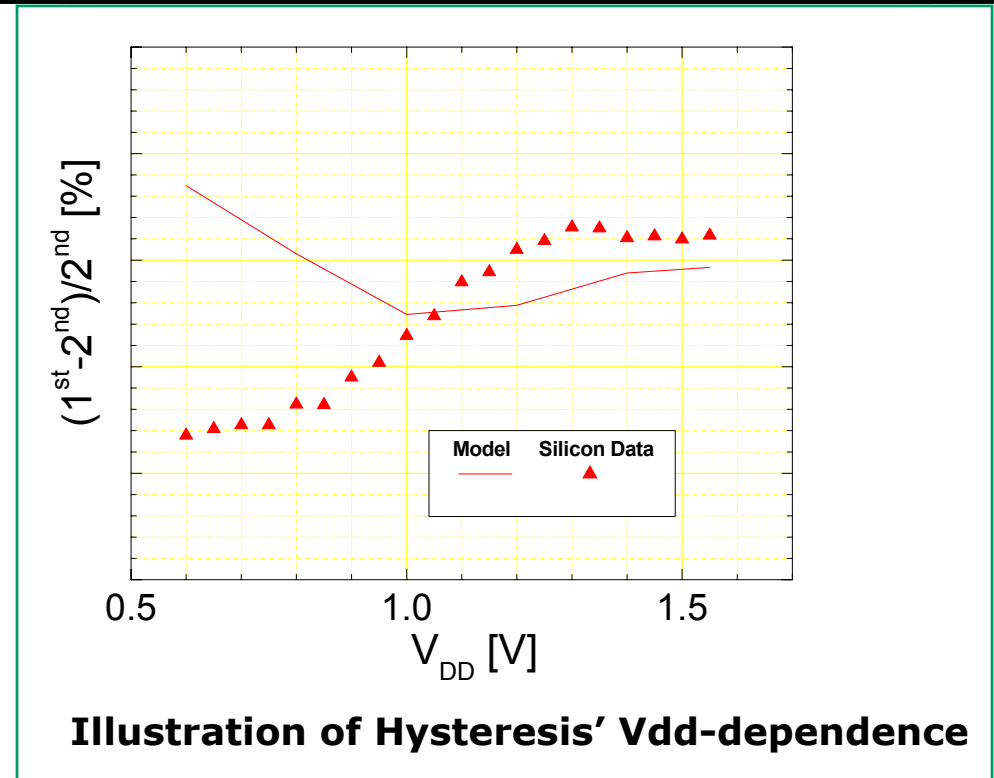
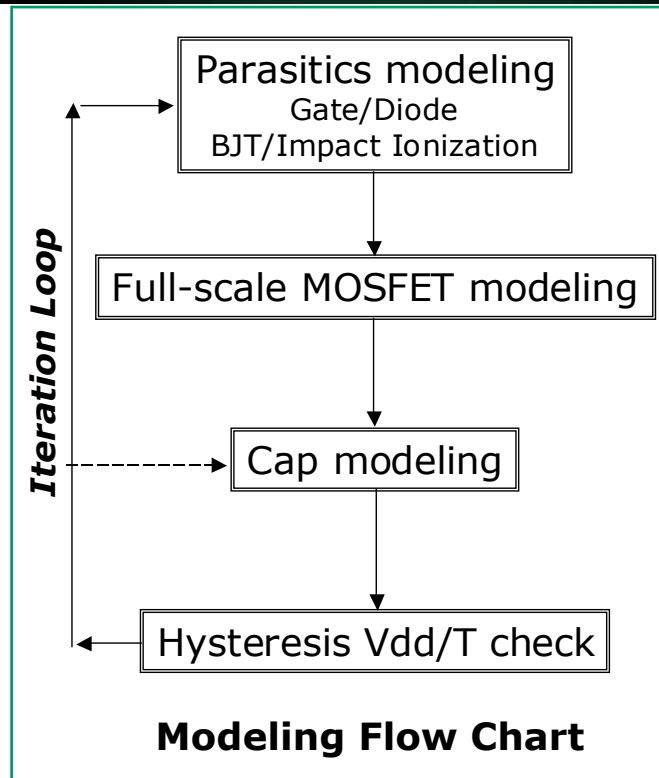
$$H = \frac{t_{pd,1} - t_{pd,2}}{t_{pd,2}} * 100\%$$

- Typically, slow 1st switch & fast 2nd switch



- Key causes to hysteresis
 - Parasitic currents
 - Gate tunneling current
 - Diode current
 - Parasitic BJT current
 - Capacitance network (gate-body-source/drain)
 - Body effect

Conventional Modeling Flow w/ Hysteresis

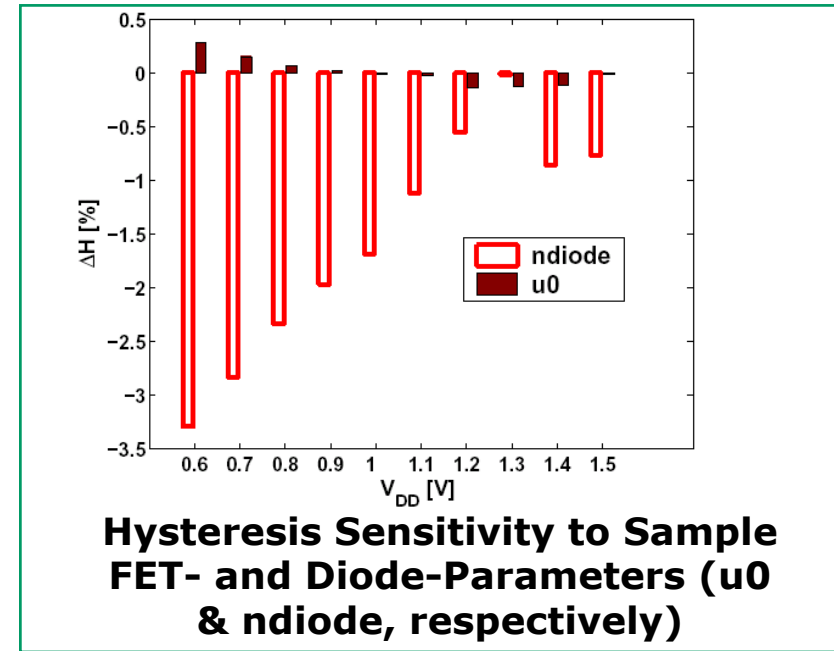
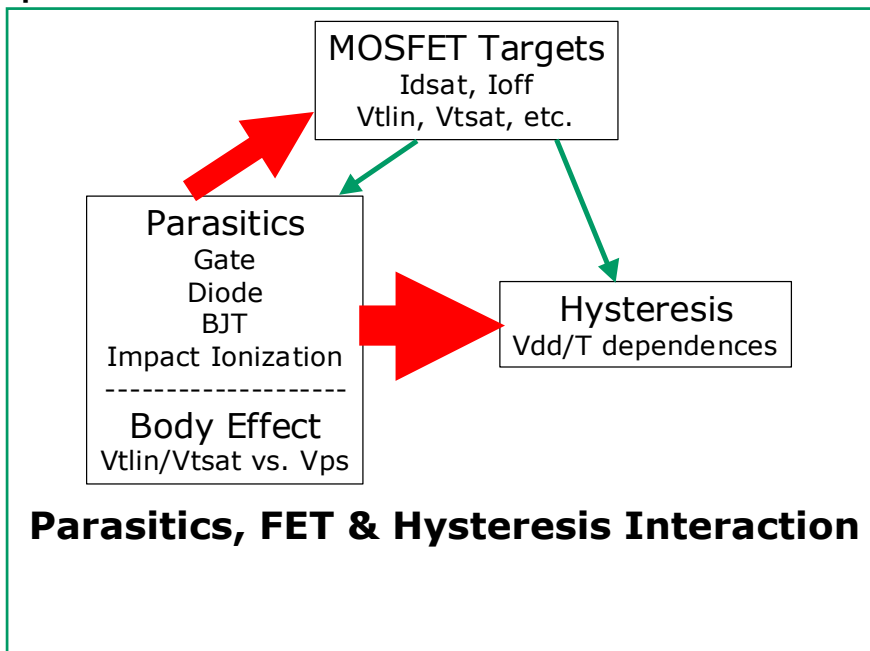


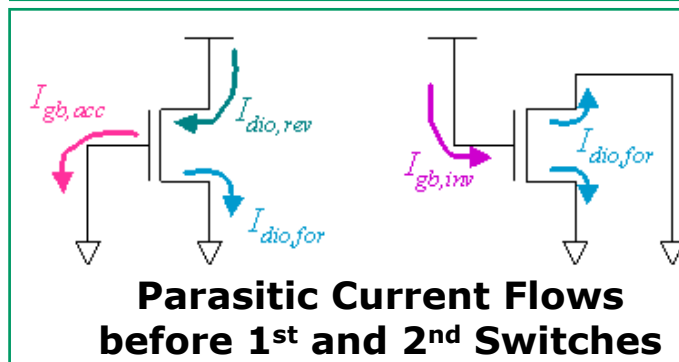
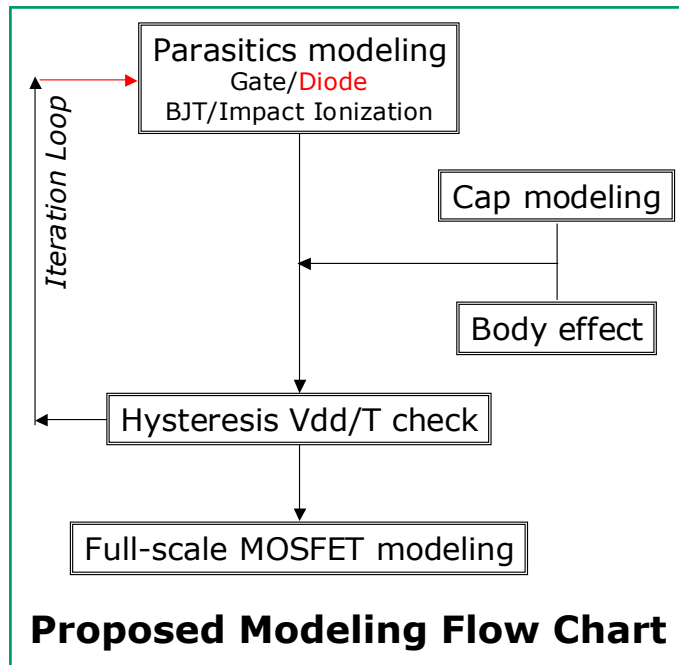
- ❑ Hysteresis levels checked toward the end of modeling flow
- ❑ Single Vdd/Temperature check may not be sufficient

Challenges and Opportunities of Hysteresis-FET Co-Modeling

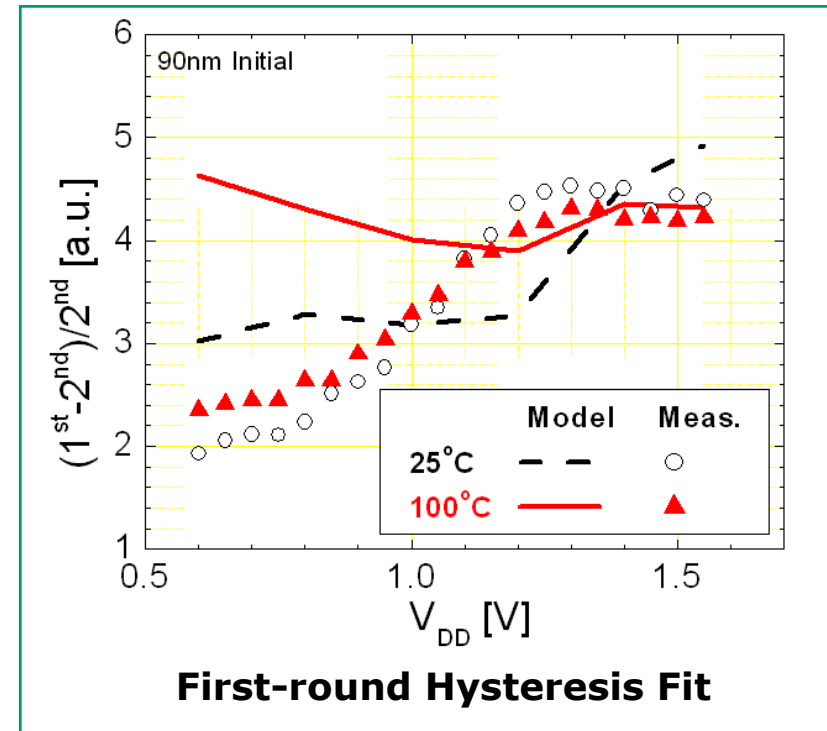
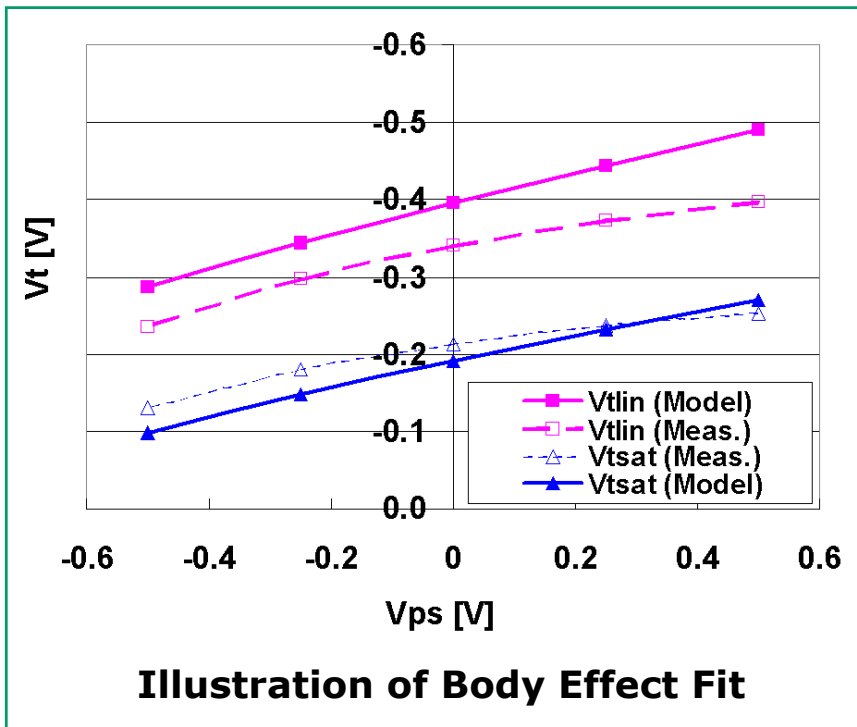


- ❑ Major tuning knobs (parasitic currents & body effect) for hysteresis modeling considerably impact FET modeling
 - Numerous and time-consuming FET-hysteresis iterations
 - Compromised hysteresis fit and parasitics fit because of limited resources
- ❑ FET model refinement has limited impact on hysteresis as well as parasitic currents

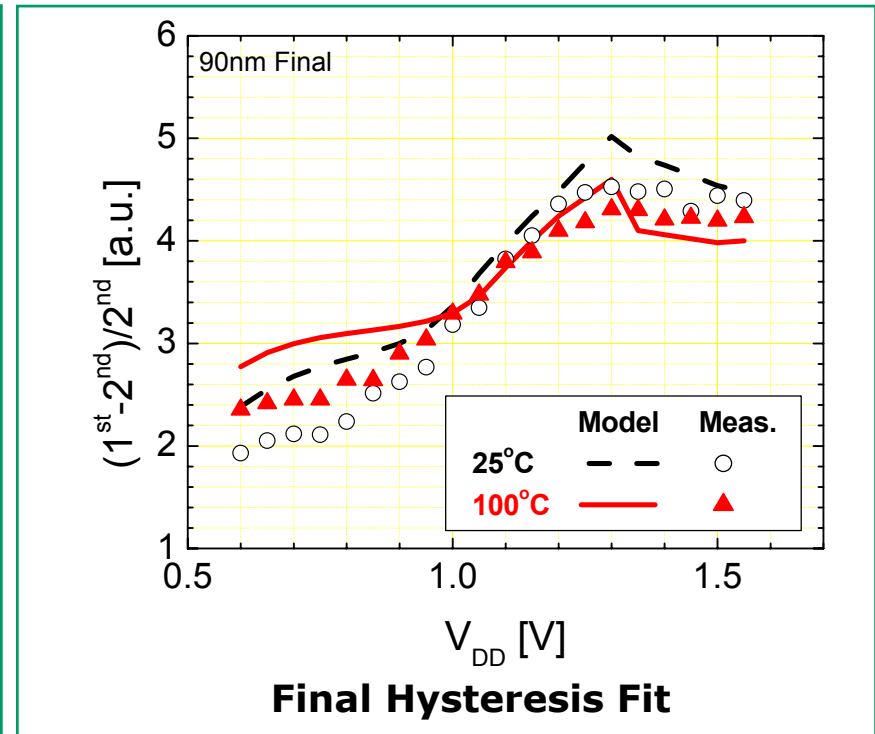
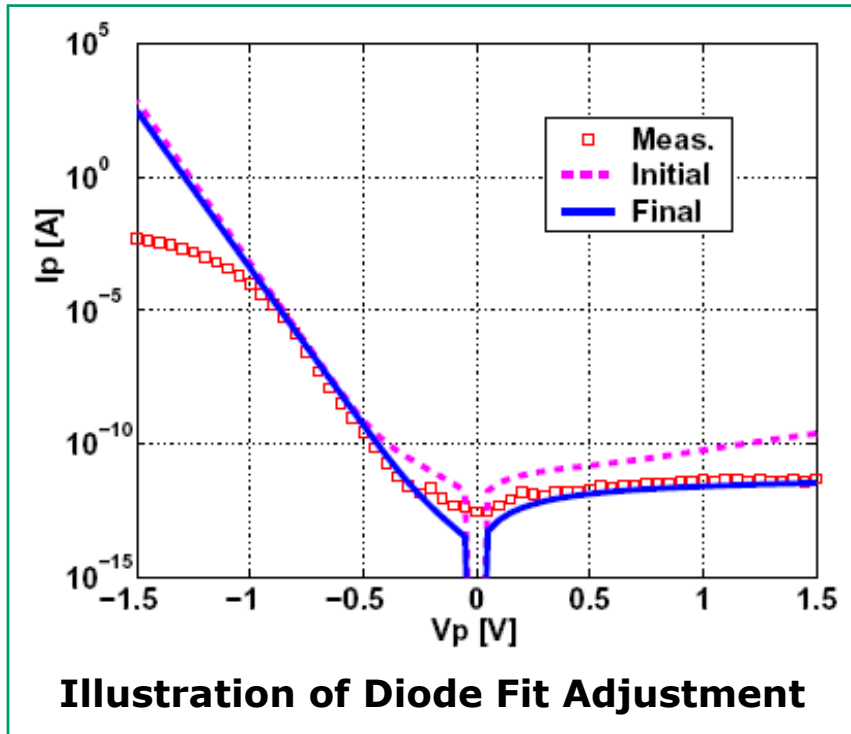




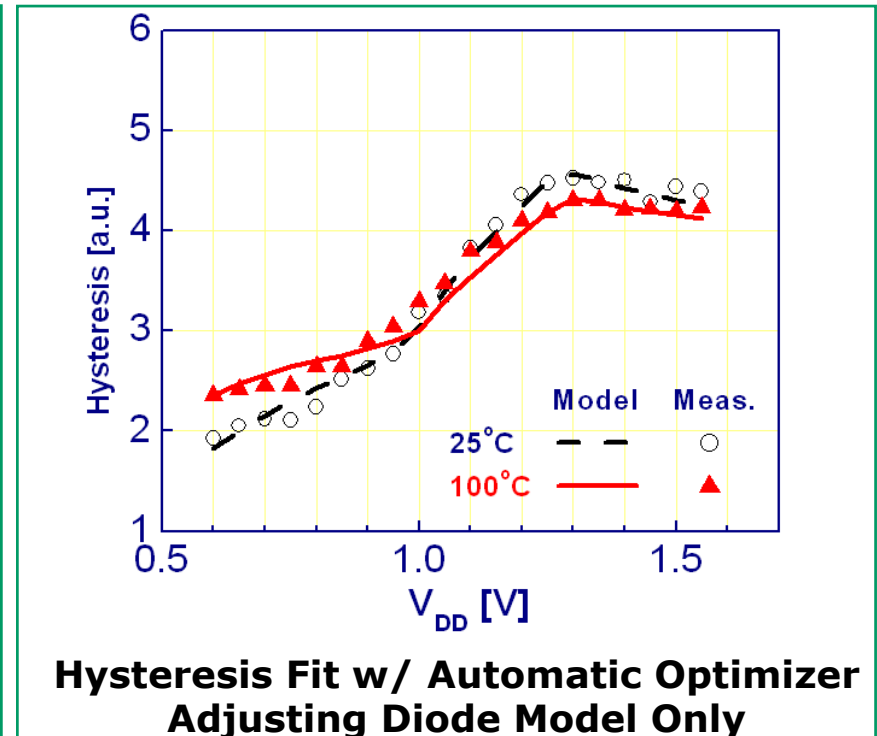
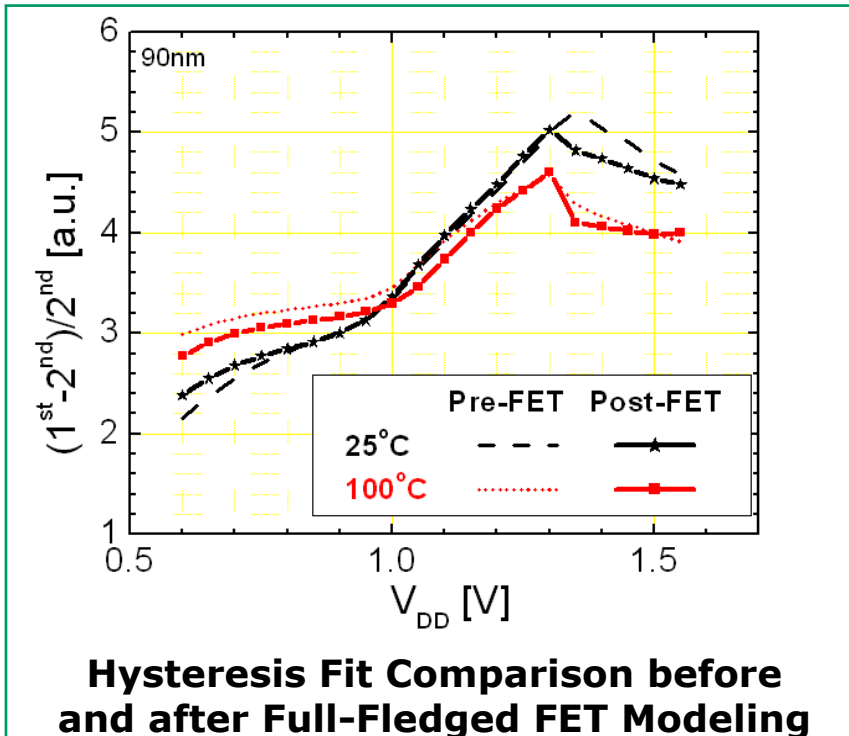
- ❑ Complete hysteresis level check *prior* to full-fledged FET modeling
 - Shortened iteration cycle
 - Reduced model closure time
- ❑ Modeling of parasitic currents, caps, and body effect to the best available data or estimate
- ❑ Diode current to exploit as the primary tuning knob for hysteresis fit
 - Unique role in determining body voltages for both switches
 - Effective for Vdd/T dependences adjustment
 - Accurate measurement available
- ❑ Reduced parameter set for hysteresis fit optimization



- ❑ Parasitic currents (except diode), caps, & body effect modeled to fit silicon data
- ❑ Initial hysteresis fit reasonable at high Vdd's, but significantly off at low Vdd's



- ❑ Diode current modeling adjustment in the low- and reverse-bias regions
- ❑ Diode model behavior in the low-bias region is intentional and justified for low current levels



- ❑ Limited changes in hysteresis levels and Vdd/T dependences from full-fledged FET modeling → in line with expectations
- ❑ Feasibility shown of automatic hysteresis fit optimization w/ diode model adjustment only

- An *a priori* hysteresis modeling methodology has been proposed as part of an improved compact model extraction flow.

- The new methodology has been successfully implemented on a 90nm PD SOI technology, demonstrating
 - Improved overall model extraction efficiency and reduced model closure time
 - Improved hysteresis fit accuracy over wide Vdd/T ranges
 - Minimum deviation of parasitic characteristics from silicon
 - Feasibility of automatic hysteresis fit optimization