Modeling and Characterization of High Frequency Effects in ULSI Interconnects

Narain Arora and Li Song

narain@cadence.com

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Outline

- Interconnect High Frequency Effects
  - Resistance effect
  - Inductance effect
  - Capacitance effect
- Characterization of High Frequency Effects
  - RC Delay
  - Crosstalk Noise
  - Power/Ground Bounce
- Conclusions
An Overview

- **Aggressive Scaling**
  - Interconnect dominates IC performance

- **Manufacturing Related Issues**
  - Electron scattering
  - CMP etc.

- **High Frequency Effects**
  - Timing/Delay
  - Ringing/Reflection
  - Signal integrity/Crosstalk
  - Power/Ground bounce etc.

Source: ITRS Roadmap 1999
Electron Scattering

\[ \rho = \rho_0 \left( \frac{1}{3} \sqrt{\frac{1}{2} - \alpha^2 + \alpha^3 \ln \left(1 + \frac{1}{\alpha}\right)} \right) + 1.2 \left(1 - p\right) \frac{U}{S} l \]

\[ \alpha = \frac{l}{d} \frac{r}{1 - r} \]

Resistivity increase due to surface and grain boundary scattering

U is the perimeter and S is the cross-section area of the wire.
Inductance Effects

Wire inductance effects

- **Ringing and overshoot** - problematic for clocks since glitches can be observed as transitions leading to faulty switching
- Increased delay
- Inductive **crosstalk** and reflections of signals due to impedance mismatch
- **Switching noise** due to voltage drops
  \[ L \frac{di}{dt} \]
  - problematic for **power distribution network**

32-bit bus lines, left most line is active

After M. Beattie and L. T. Pileggi, DAC 2001
Resistance (Skin) Effect

More pronounced skin effect at high frequencies
- Due to cladding
- CMP fills

\[ R = \frac{\rho l}{w \delta(1 - \exp\left(\frac{t}{\delta}\right))} \]

\( \delta: \) Skin Depth

- Co-planar
- Floating Parallel Lines
- Ground Crossing Lines

- Al Model \( \rho = 33 \, m\Omega \cdot \mu m \)
- Al Model \( \rho = 29 \, m\Omega \cdot \mu m \)

Highly resistive cladding
Cu Wire
Skin Effect Modeling

- SPICE simulations with/without Skin Effect
- Skin effect influence both reflection and signal propagation
CMP metal fills blocks provide current return loop at high frequencies.
SPICE Modeling

Previous Ladder and Branch models can’t predict both R and L values well.
High Frequency Capacitance (Cu)

- Relatively constant at high frequencies (peaks are resonant peaks, the resonant frequency is smaller for structure with high capacitance)
Interconnect High Frequency Effect Characterization

- Two ways of characterizing interconnects are:
  1. Use the Field Solvers that are based on Maxwell’s equations (soft validation).

   Inherent assumption is that process parameters that are input to the solver are correct (from silicon prospective).

   2. Test chips fabricated on Silicon Wafers for a given technology, measuring the RCL of those structures (Silicon validation). Though expensive and time consuming, it is the only way to do correct model validation.

- Characterization Techniques
  - S Parameter Measurement
  - TDR Measurement
  - Ring Oscillator Technique
S Parameter Measurement

- S parameters are measured on test structures (HP 8510C network analyzer (50MHz-50GHz), (Short, Open, Load and Through) SOLT calibration on Cascade standard*).
- Test Structure pads are de-embedded and parasitic are corrected.
- Propagation constant and characteristic impedance are extracted from S parameters measured as shown in Figure.
- Resistance and inductance are extracted from the propagation constant and characteristic impedance.

* See Cascade Microtech website: www.cmicro.com
S parameter response from a transmission line

\[
[S] = \frac{1}{D_s} \begin{bmatrix}
(Z^2 - Z_0^2) \sinh \gamma l & 2ZZ_0 \\
2ZZ_0 & (Z^2 - Z_0^2) \sinh \gamma l
\end{bmatrix}
\]

\[D_s = 2ZZ_0 \cosh \gamma l + (Z^2 + Z_0^2) \sinh \gamma l\]

Solving for propagation constant and characteristic impedance

\[
e^{-\gamma l} = \left\{ \frac{1 - S_{11}^2 + S_{21}^2}{2S_{21}} \pm K \right\}^{-1}, \quad K = \left\{ \frac{(S_{11}^2 - S_{21}^2 + 1)^2 - (2S_{11})^2}{(2S_{21})^2} \right\}^{\frac{1}{2}}, \quad Z^2 = Z_0^2 \frac{(1 + S_{11})^2 - S_{21}^2}{(1 - S_{11})^2 - S_{21}^2}
\]

From

\[
\gamma = \alpha + j\beta = \sqrt{(R + j\omega L)(G + j\omega C)}
\]

\[\alpha \text{ attenuation constant} \quad \beta \text{ phase constant} \quad Z_0 = R_0 + jX_0 = \sqrt{\frac{R + j\omega L}{G + j\omega C}}
\]

Then

\[R = \text{Re}\{\gamma Z\} \quad G = \text{Re}\{\gamma/Z\} \quad L = \text{Im}\{\gamma Z\}/\omega \quad C = \text{Im}\{\gamma/Z\}/\omega
\]

For wire length 6mm:

<table>
<thead>
<tr>
<th>R (Ohm)</th>
<th>L (nH)</th>
<th>C(fF)</th>
<th>RC Delay (ns)</th>
<th>LC Delay (ns)</th>
<th>RO Delay (ns)</th>
<th>RO $f_0$ (MHz)</th>
</tr>
</thead>
<tbody>
<tr>
<td>2400</td>
<td>3.00</td>
<td>0.30</td>
<td>0.720</td>
<td>0.030</td>
<td>0.750</td>
<td>667</td>
</tr>
</tbody>
</table>
## RC Delays

<table>
<thead>
<tr>
<th>Process Node (nm)</th>
<th>180</th>
<th>130</th>
<th>90</th>
<th>65</th>
<th>45</th>
</tr>
</thead>
<tbody>
<tr>
<td>Width /Spacing</td>
<td>280</td>
<td>200</td>
<td>140</td>
<td>100</td>
<td>80</td>
</tr>
<tr>
<td>Metal Thickness</td>
<td>580</td>
<td>350</td>
<td>320</td>
<td>270</td>
<td>200</td>
</tr>
<tr>
<td>Dielectric Thickness</td>
<td>800</td>
<td>360</td>
<td>270</td>
<td>200</td>
<td>140</td>
</tr>
<tr>
<td>Dielectric Constant</td>
<td>4.00</td>
<td>3.60</td>
<td>3.10</td>
<td>2.90</td>
<td>2.70</td>
</tr>
<tr>
<td>Resistivity ($\mu\Omega \cdot \text{cm}$)</td>
<td>3.70</td>
<td>2.20</td>
<td>2.20</td>
<td>2.60</td>
<td>2.90</td>
</tr>
<tr>
<td>$R$ ($\Omega/\mu$m)</td>
<td>0.246</td>
<td>0.314</td>
<td>0.476</td>
<td>0.815</td>
<td>1.813</td>
</tr>
<tr>
<td>$C$ (fF/µm)</td>
<td>0.122</td>
<td>0.083</td>
<td>0.093</td>
<td>0.095</td>
<td>0.080</td>
</tr>
<tr>
<td>SoC Freq. (KHz)</td>
<td>500</td>
<td>1000</td>
<td>1500</td>
<td>2000</td>
<td>3000</td>
</tr>
<tr>
<td>$jwL$ ($/\mu$m)</td>
<td>0.013</td>
<td>0.023</td>
<td>0.033</td>
<td>0.044</td>
<td>0.063</td>
</tr>
<tr>
<td>RC delay (fs/µm)</td>
<td><strong>0.030</strong></td>
<td><strong>0.026</strong></td>
<td><strong>0.044</strong></td>
<td><strong>0.077</strong></td>
<td><strong>0.145</strong></td>
</tr>
</tbody>
</table>

- RC delay decreased at 130nm node due to the introduction of Cu and low $k$ material
- Inductance effect increases as operating frequency increases
- RC delay increases again as resistivity of Cu wire increases (cladding and electron scattering)
Manhattan vs. X Architecture Routing

Lower cost and Higher performance

Manhattan

A Better Way

Chip Impact: 20% Less Interconnect 30% Fewer Vias

30% shorter
X Architecture Layout

A typical layout and SEM picture

Pervasive use of diagonal wires
Power Grid effects on Inductance

- L increases for increasing spacing because more flux is enclosed between the signal line and the return path.
- In a realistic test structure, L becomes less dependent on the spacing to the intended return ground. Local lines and capacitive coupling provide alternative return paths.


Manhattan Signal

X Architecture Signal
Small variation for diagonal signal line
Crosstalk

- Capacitive Crosstalk

- Inductive Crosstalk

- Total Crosstalk

\[ V_{NE} = K_{NE} v_0 \quad K_{NE} = \frac{1}{4} \left( \frac{C_c}{C} + \frac{L_m}{L} \right) \quad V_{FE} = \frac{1}{2} d \left( Z_0 c_c - \frac{L_m}{Z_0} \right) d \frac{dV_s}{dt} \]
Inductive Impact at Clock Signal

- Clock carries multi-gigahertz frequency signals with short rise/fall time
- Inductive effects actually reduce rise time at near end, but increases clock skews
- Modeled as co-planar wave guide (CPWG)

Distributed RC/RLC SPICE model, inductance is frequency dependent in the parallel model
Inductive Impact on Bus Lines

- Simultaneous signal switch increase timing push-out
- Leading to inductive noise

Qi, et al (GLSVLSI'03)
Power/Ground Bounce

- On-chip power/ground grid noise is the Vdd/Vss fluctuation due to Ldi/dt

Qi, et al (GLSVLSI’03)
Conclusion

• Accurate characterization of high frequency effect such as skin effect, inductance impact on clock, buses and power/ground grid are essential in VLSI design.

• High frequency skin effects, inductance and capacitance effects and their impacts on clock, bus and power grids are studied.

• Modeling of RC delay, crosstalk and power/ground bounce are presented.

• RLC extraction and modeling in sub-90nm technologies with consideration of manufacturing effects such as electron scattering in nanometer wires, high aspect ratio wires and CMP effects.
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how big can you dream?