

*how big can you dream?*<sup>™</sup>



# Modeling and Characterization of High Frequency Effects in ULSI Interconnects

**Narain Arora and Li Song**

[narain@cadence.com](mailto:narain@cadence.com)

**May 11, 2005**

# Outline

---

- **Interconnect High Frequency Effects**
  - Resistance effect
  - Inductance effect
  - Capacitance effect
- **Characterization of High Frequency Effects**
  - RC Delay
  - Crosstalk Noise
  - Power/Ground Bounce
- **Conclusions**

# An Overview

- **Aggressive Scaling**

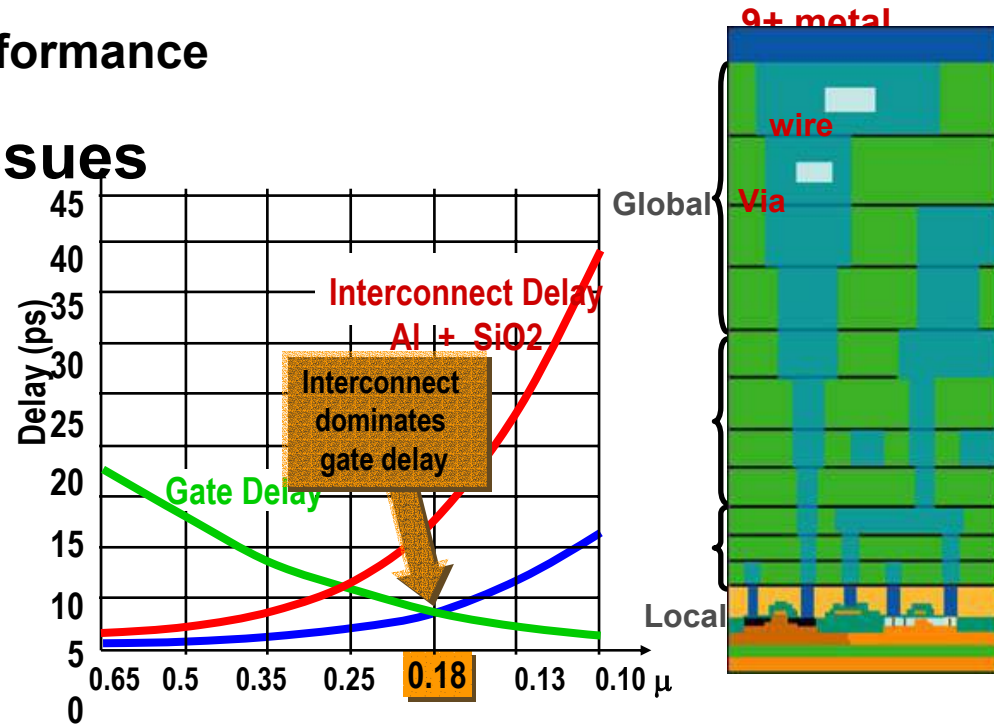
→ Interconnect dominates IC performance

- **Manufacturing Related Issues**

- Electron scattering
- CMP etc.

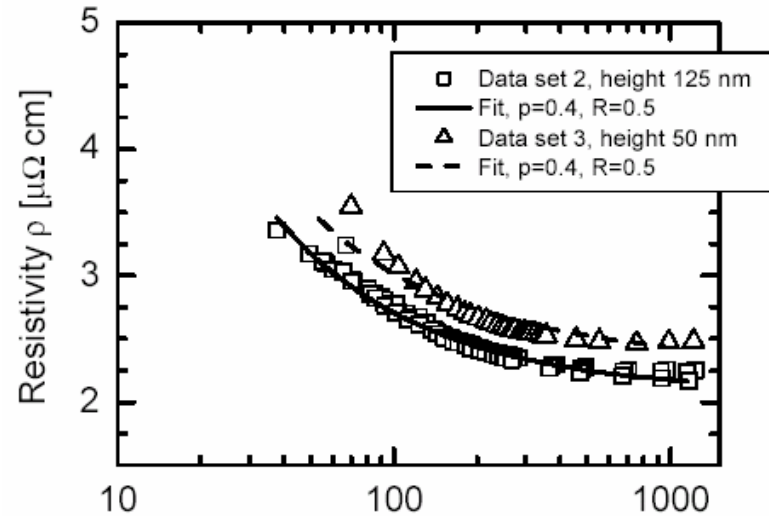
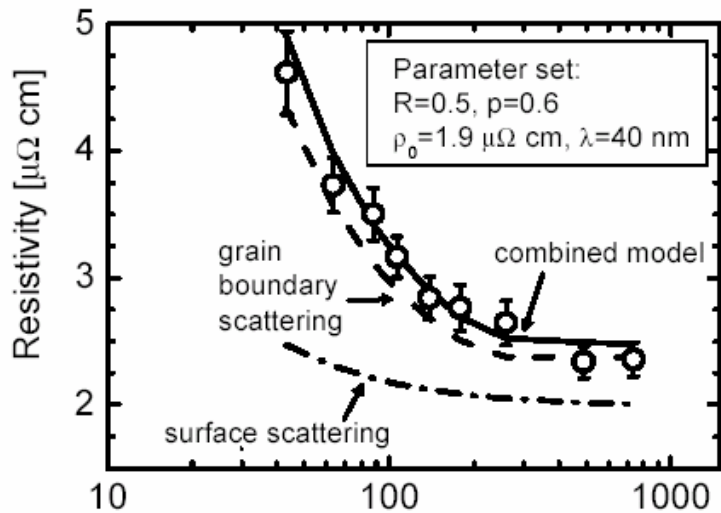
- **High Frequency Effects**

- Timing/Delay
- Ringing/Reflection
- Signal integrity/Crosstalk
- Power/Ground bounce etc.



Source: ITRS Roadmap 1999

# Electron Scattering

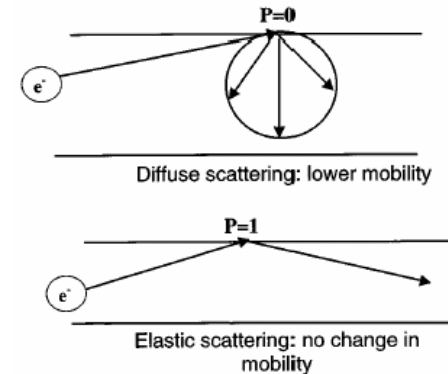


W. Steinhoegl et al., SISPAD 2003

$$\rho = \rho_0 \left( \frac{1}{3} / \left( \frac{1}{3} - \frac{\alpha}{2} + \alpha^2 - \alpha^3 \ln \left( 1 + \frac{1}{\alpha} \right) \right) + 1.2(1-p) \frac{U}{S} l \right)$$

$$\alpha = \frac{l}{d} \frac{r}{1-r}$$

Resistivity increase due to surface and grain boundary scattering



U is the perimeter and S is the cross-section area of the wire

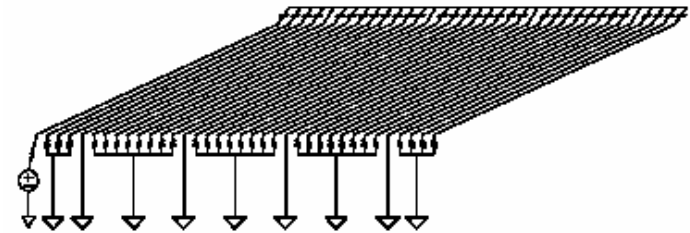
# Inductance Effects

## Wire inductance effects

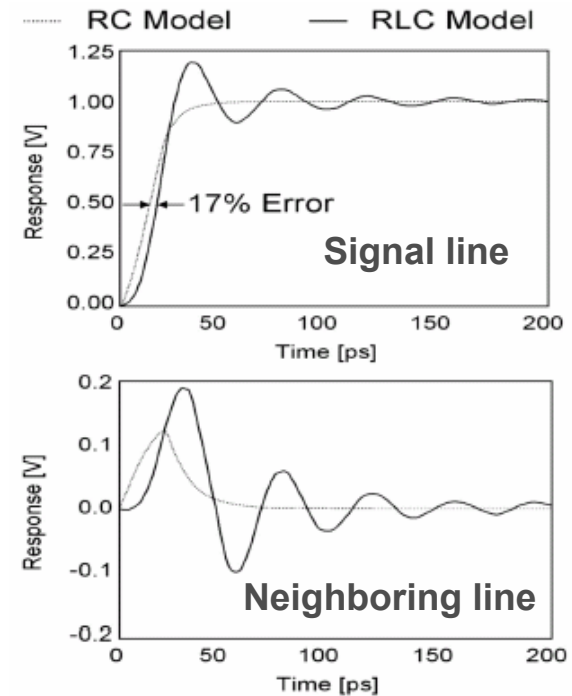
- Ringing and overshoot - problematic for clocks since glitches can be observed as transitions leading to faulty switching
- Increased delay
- Inductive crosstalk and reflections of signals due to impedance mismatch
- Switching noise due to voltage drops

$$L \frac{di}{dt}$$

- problematic for power distribution network



32-bit bus lines, left most line is active



After M. Beattie and L. T. Pileggi, DAC 2001

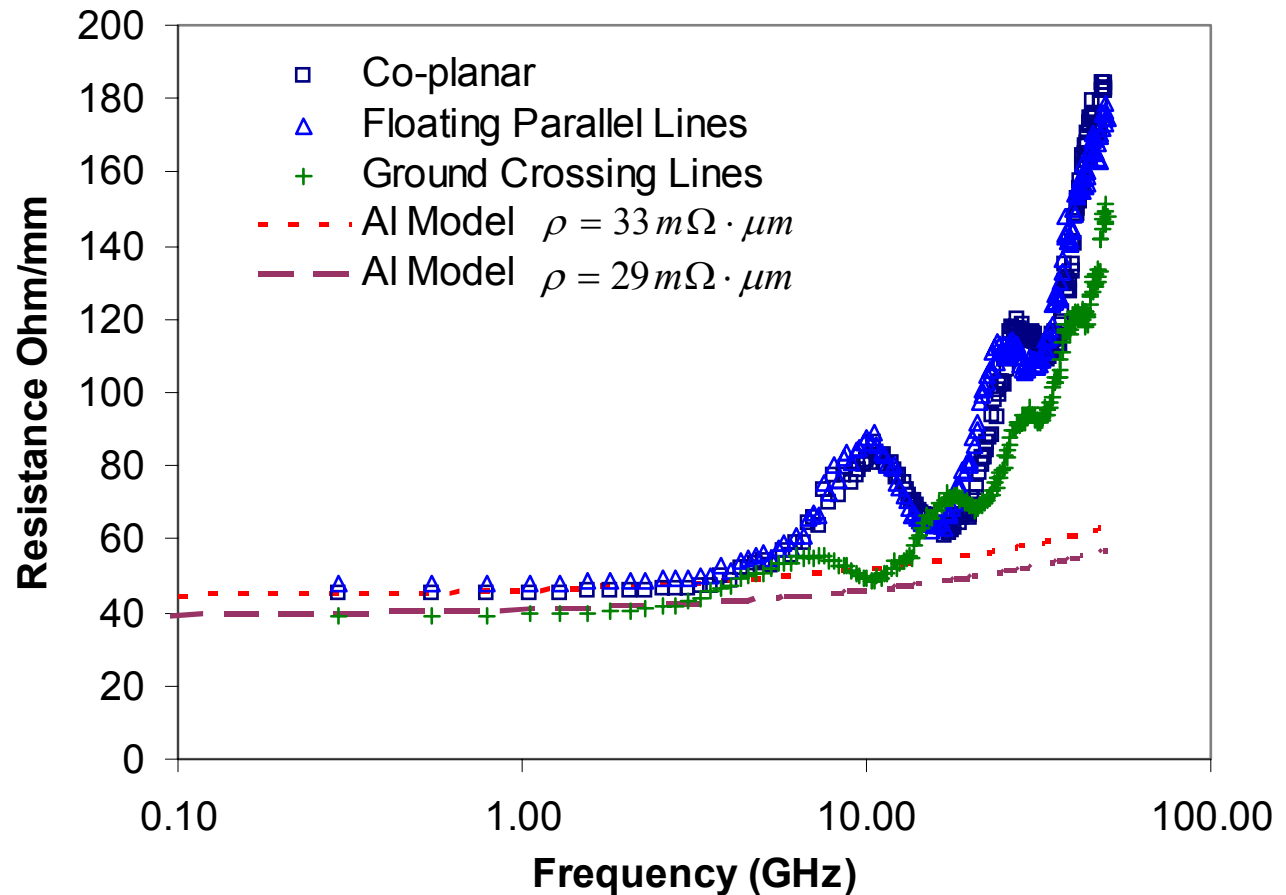
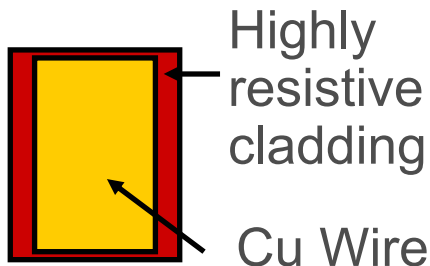
# Resistance (Skin) Effect

$$R = \frac{\rho l}{w \delta \left(1 - \exp\left(-\frac{t}{\delta}\right)\right)}$$

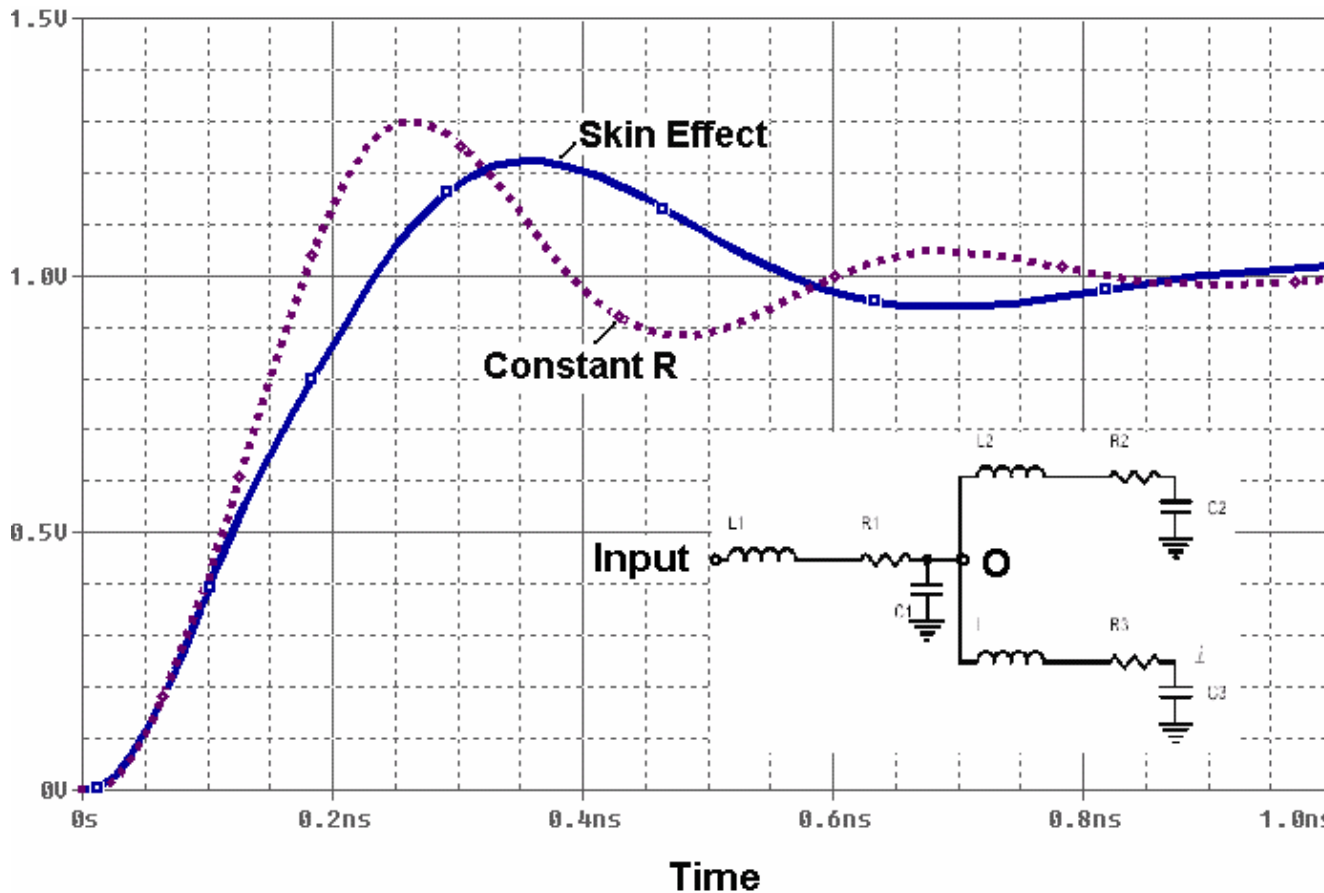
$\delta$ : Skin Depth

More pronounced skin effect at high frequencies

- Due to cladding
- CMP fills



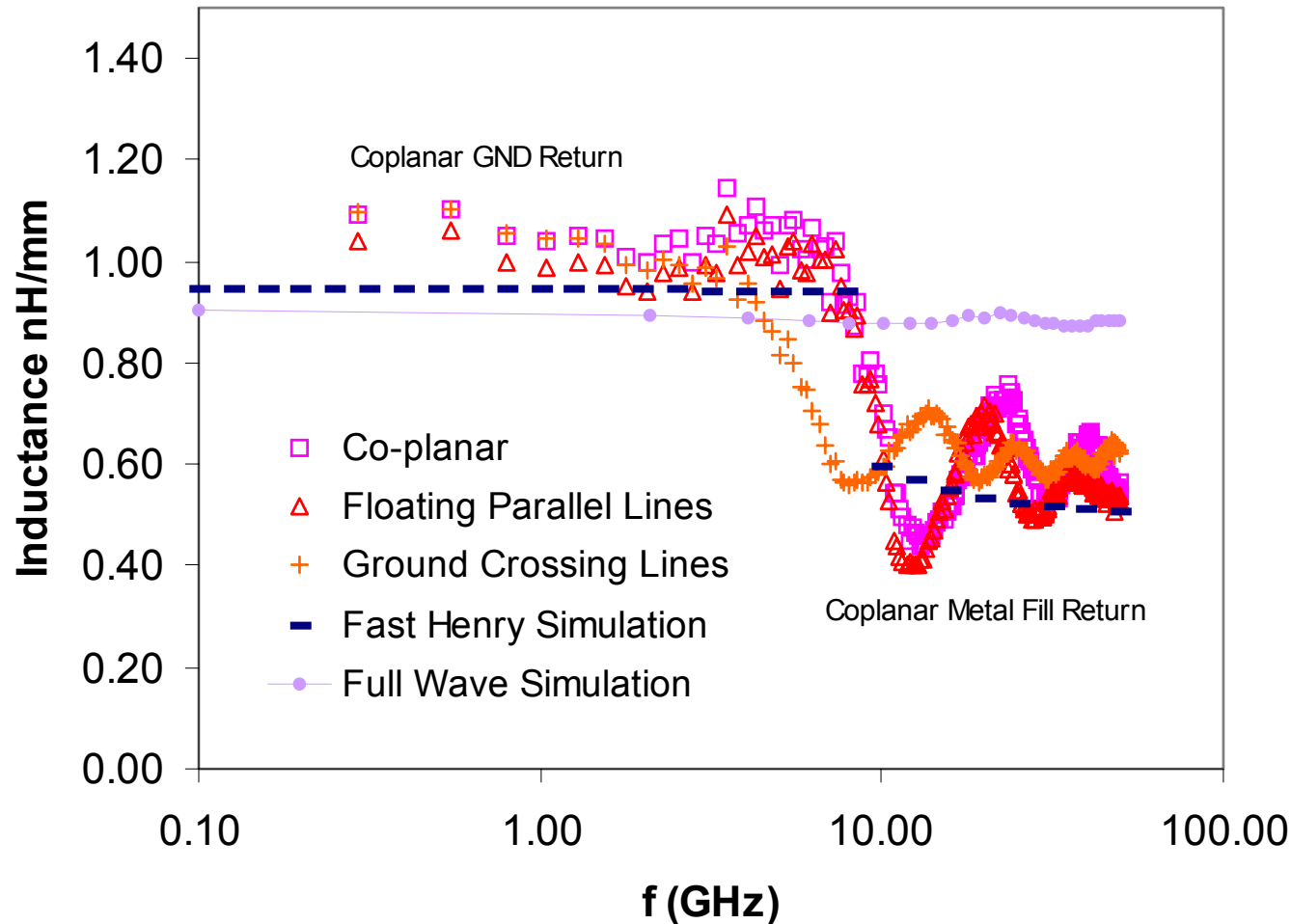
# Skin Effect Modeling



- SPICE simulations with/without Skin Effect
- Skin effect influence both reflection and signal propagation

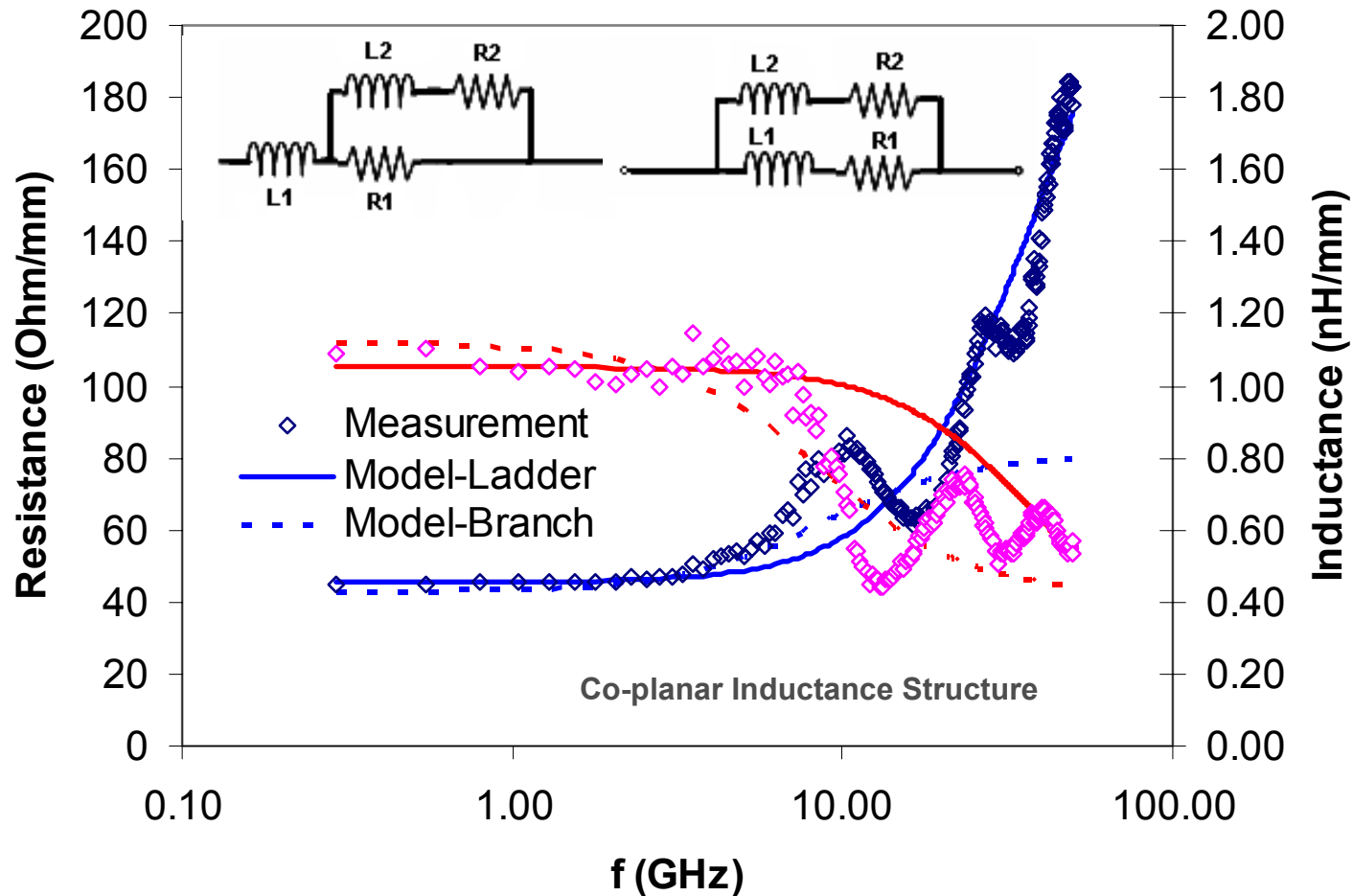
# Field Solver Simulation and Modeling

CMP metal fills blocks provide current return loop at high frequencies

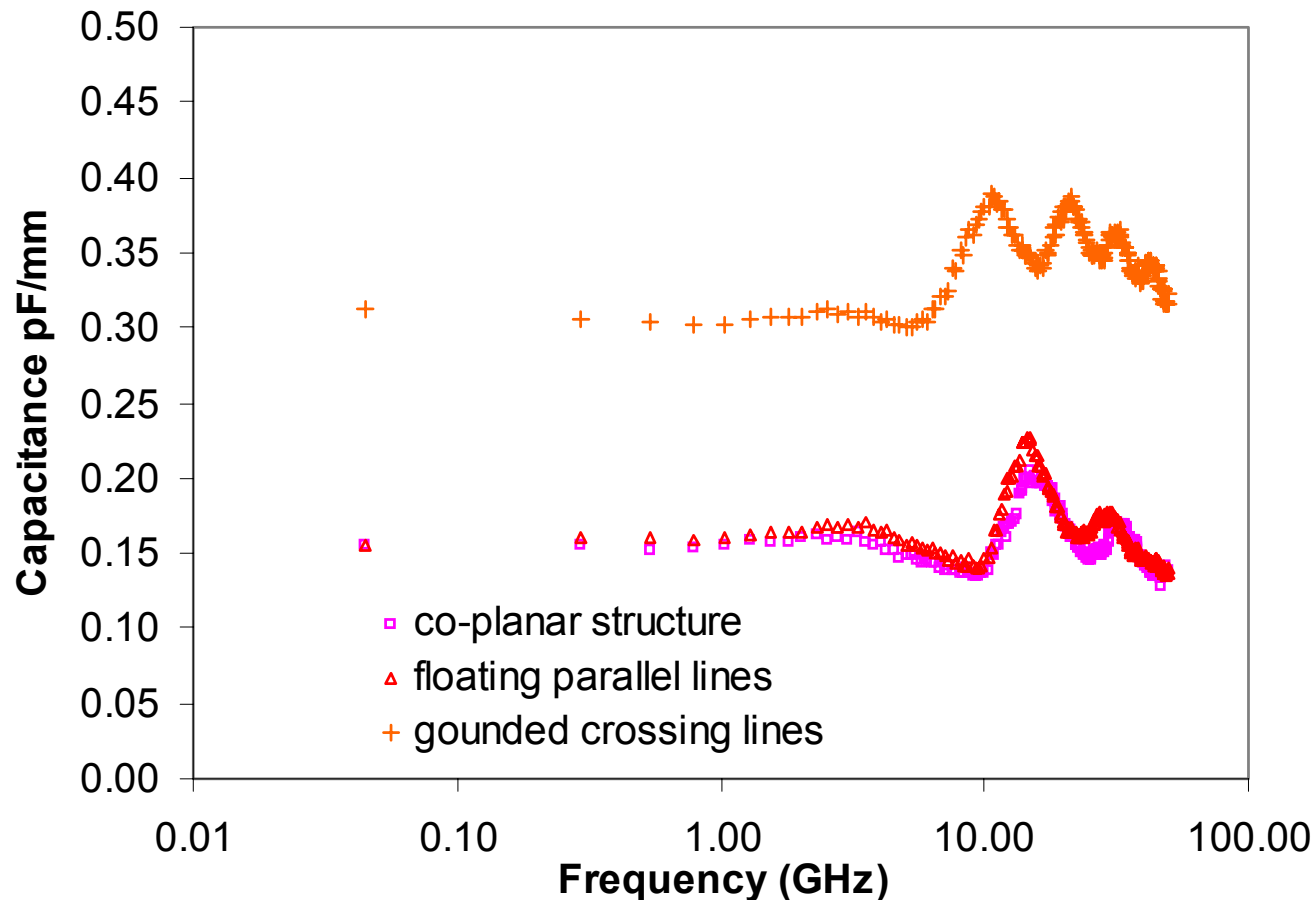


# SPICE Modeling

Previous Ladder and Branch models can't predict both R and L values well



# High Frequency Capacitance (Cu)



- Relatively constant at high frequencies (peaks are resonant peaks, the resonant frequency is smaller for structure with high capacitance)

# Interconnect High Frequency Effect Characterization

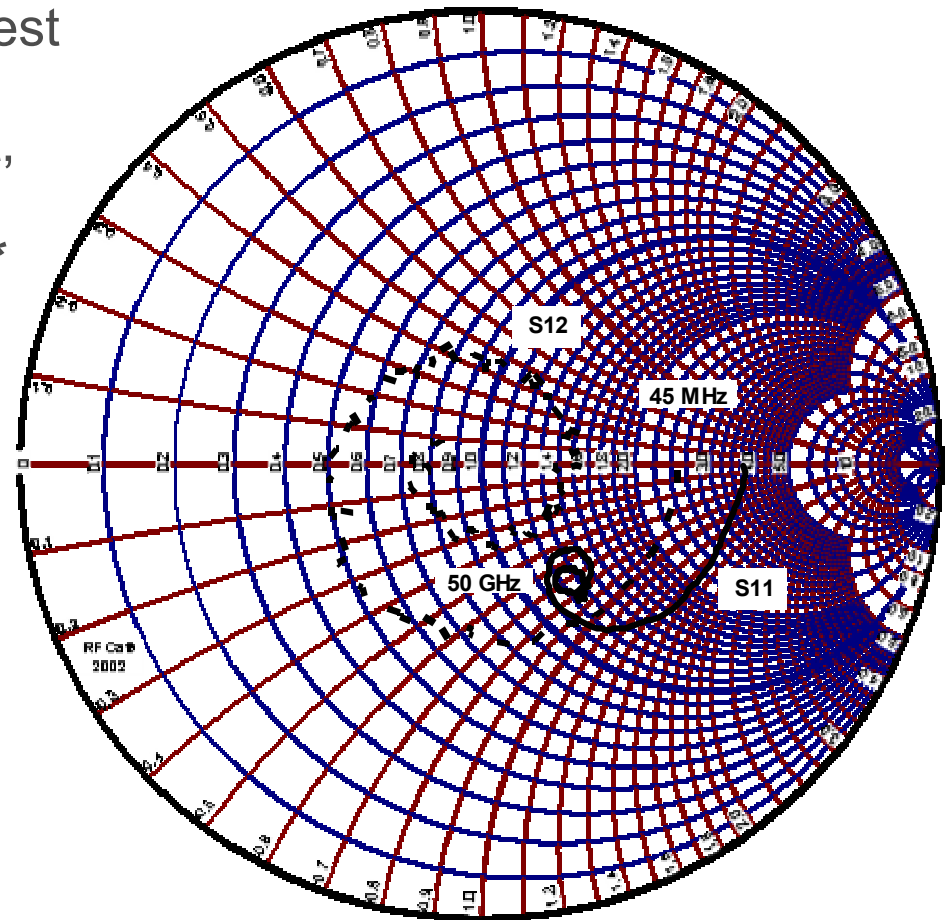
---

- Two ways of characterizing interconnects are :
  1. Use the **Field Solvers** that are based on Maxwell's equations (**soft validation**).

Inherent assumption is that process parameters that are input to the solver are correct (from silicon prospective).
  2. **Test chips** fabricated on Silicon Wafers for a given technology, measuring the RCL of those structures (**Silicon validation**). **Though expensive and time consuming, it is the only way to do correct model validation.**
- **Characterization Techniques**
  - S Parameter Measurement
  - TDR Measurement
  - Ring Oscillator Technique

# S Parameter Measurement

- S parameters are measured on test structures (HP 8510C network analyzer (50MHz-50GHz), (Short, Open, Load and Through) SOLT calibration on Cascade standard\*
- Test Structure pads are de-embedded and parasitic are corrected
- Propagation constant and characteristic impedance are extracted from S parameters measured as shown in Figure
- Resistance and inductance are extracted from the propagation constant and characteristic impedance



Smith Chart of Co-planar structure #1

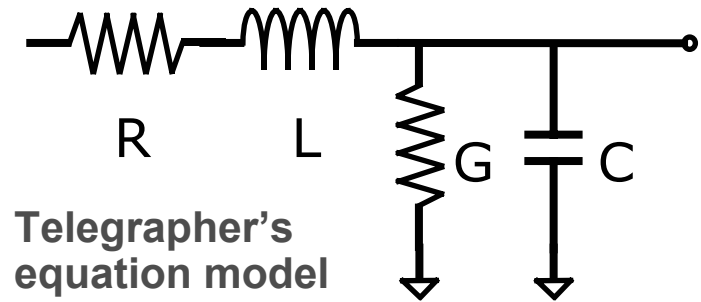
\* See Cascade Microtech website: [www.cmicro.com](http://www.cmicro.com)

# RLCG Extraction

S parameter response from a transmission line

$$[S] = \frac{1}{D_s} \begin{bmatrix} (Z^2 - Z_0^2) \sinh \gamma l & 2ZZ_0 \\ 2ZZ_0 & (Z^2 - Z_0^2) \sinh \gamma l \end{bmatrix}$$

$$D_s = 2ZZ_0 \cosh \gamma l + (Z^2 + Z_0^2) \sinh \gamma l$$



Solving for propagation constant and characteristic impedance

$$e^{-\gamma l} = \left\{ \frac{1 - S_{11}^2 + S_{21}^2}{2S_{21}} \pm K \right\}^{-1}, \quad K = \left\{ \frac{(S_{11}^2 - S_{21}^2 + 1)^2 - (2S_{11})^2}{(2S_{21})^2} \right\}^{\frac{1}{2}}, \quad Z^2 = Z_0^2 \frac{(1 + S_{11})^2 - S_{21}^2}{(1 - S_{11})^2 - S_{21}^2}$$

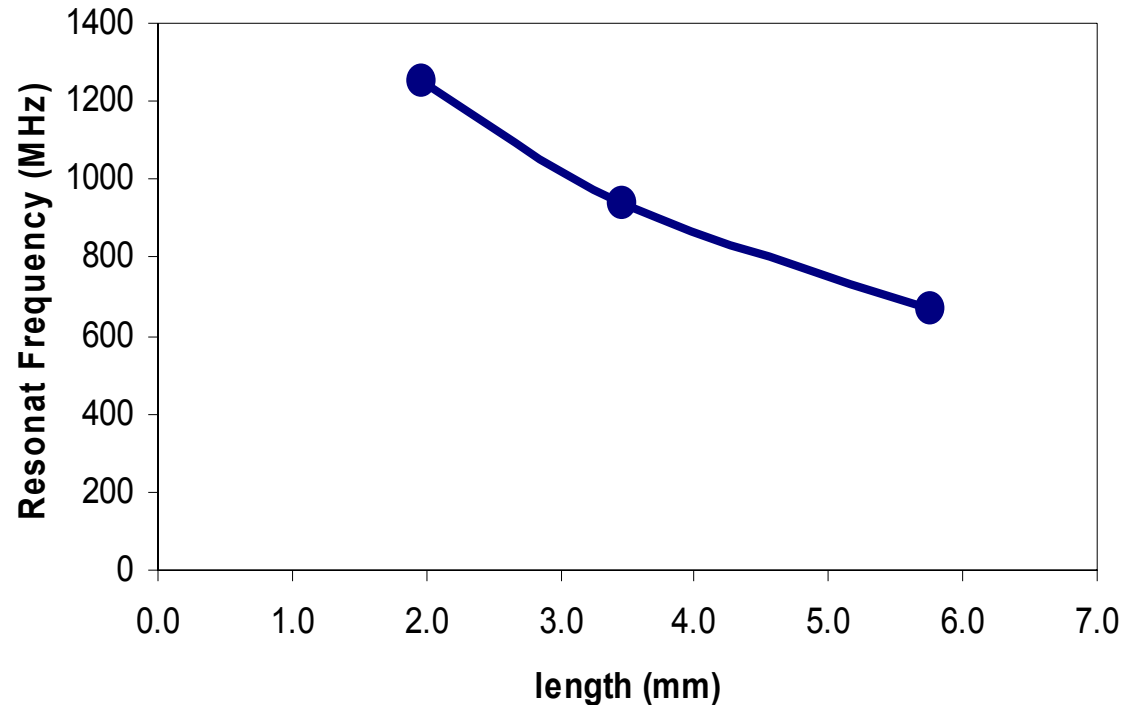
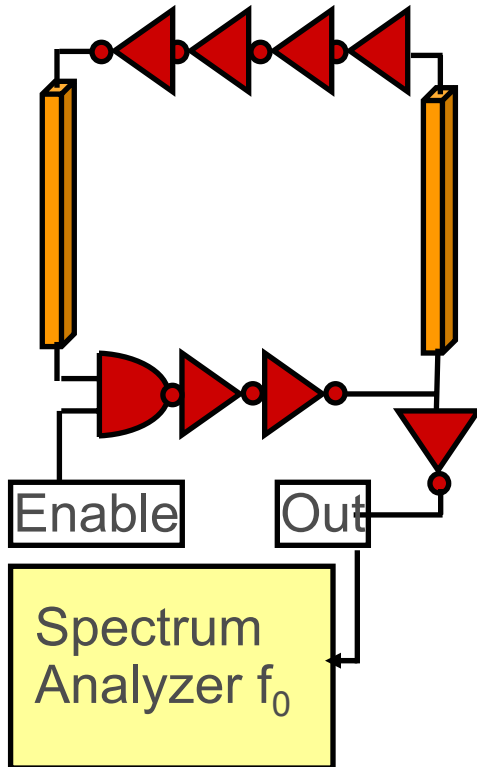
From  $\gamma = \alpha + j\beta = \sqrt{(R + j\omega L)(G + j\omega C)}$        $\alpha$  attenuation constant  
 $\beta$  phase constant       $Z_0 = R_0 + jX_0 = \sqrt{\frac{R + j\omega L}{G + j\omega C}}$

Then  $R = \text{Re}\{\gamma Z\}$        $G = \text{Re}\{\gamma/Z\}$   
 $L = \text{Im}\{\gamma Z\}/\omega$        $C = \text{Im}\{\gamma/Z\}/\omega$

Eisenstadt, et. Al. IEEE Tran. Component, Hybrids and Manufacturing Tech. pp483-490, Vol. 15, No. 4 Aug., 1992

# Ring Oscillators

RC delay dominates for 0.14um wide Cu wire delays



For wire length 6mm:

R (Ohm)	L (nH)	C (fF)	RC Delay (ns)	LC Delay (ns)	RO Delay (ns)	RO $f_0$ (MHz)
2400	3.00	0.30	0.720	0.030	0.750	667

# RC Delays

Process Node (nm)	180	130	90	65	45
Width /Spacing	280	200	140	100	80
Metal Thickness	580	350	320	270	200
Dielectric Thickness	800	360	270	200	140
Dielectric Constant	4.00	3.60	3.10	2.90	2.70
Resistivity ( $\mu\Omega\cdot\text{cm}$ )	3.70	2.20	2.20	2.60	2.90
R ( $\Omega/\mu\text{m}$ )	0.246	0.314	0.476	0.815	1.813
C (fF/ $\mu\text{m}$ )	0.122	0.083	0.093	0.095	0.080
SoC Freq. (KHz)	500	1000	1500	2000	3000
j $\omega$ L ( $/\mu\text{m}$ )	0.013	0.023	0.033	0.044	0.063
RC delay (fs/ $\mu\text{m}$ )	0.030	0.026	0.044	0.077	0.145

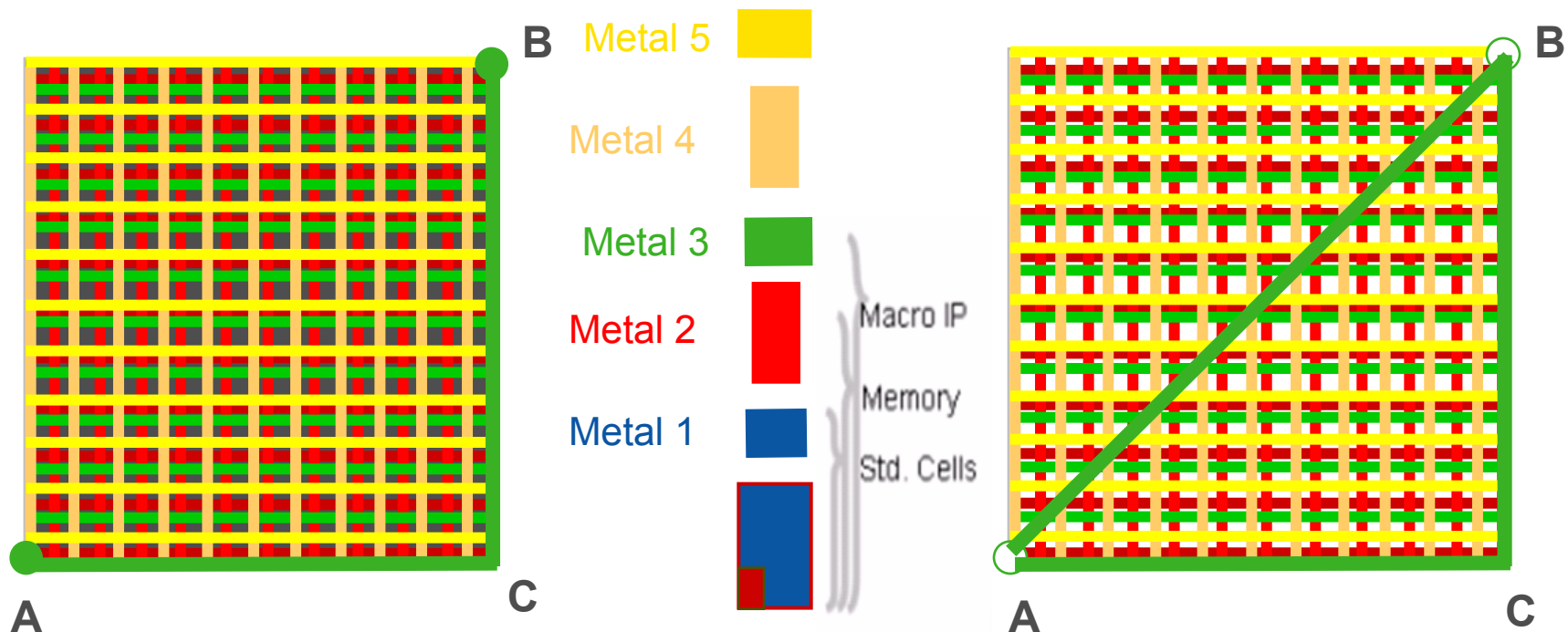
- RC delay decreased at 130nm node due to the introduction of Cu and low k material
- Inductance effect increases as operating frequency increases
- RC delay increases again as resistivity of Cu wire increases (cladding and electron scattering)

# Manhattan vs. X Architecture Routing

*Lower cost and Higher performance*

Manhattan

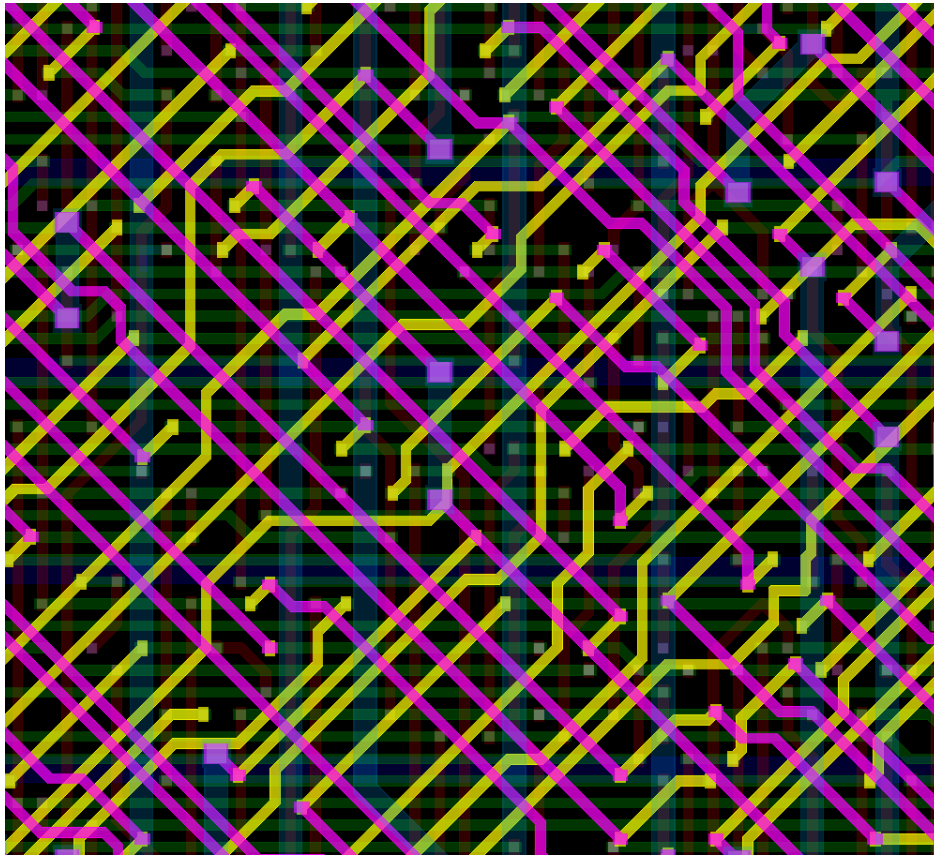
**A Better Way**



30% shorter

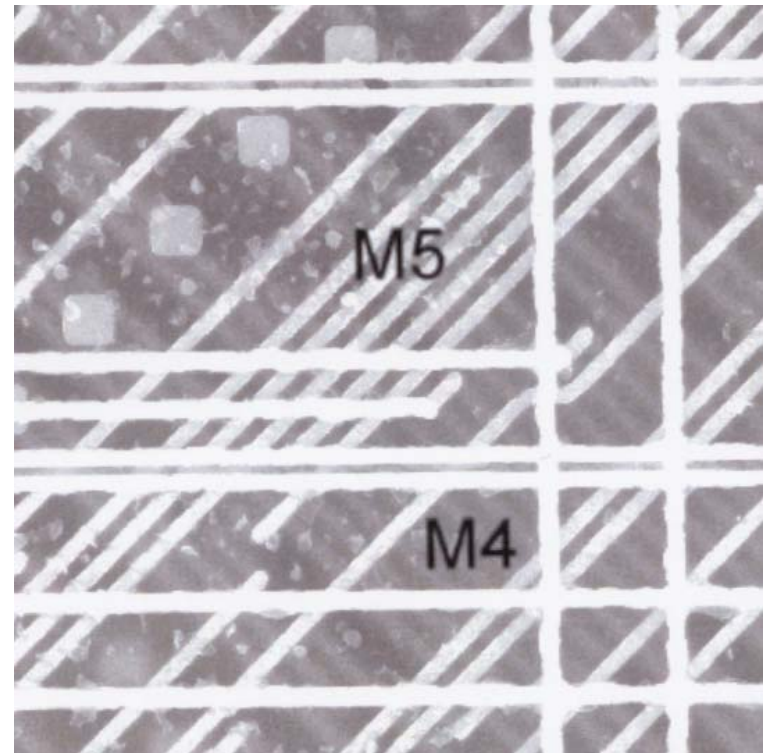
**Chip Impact: 20% Less Interconnect 30% Fewer Vias**

# X Architecture Layout



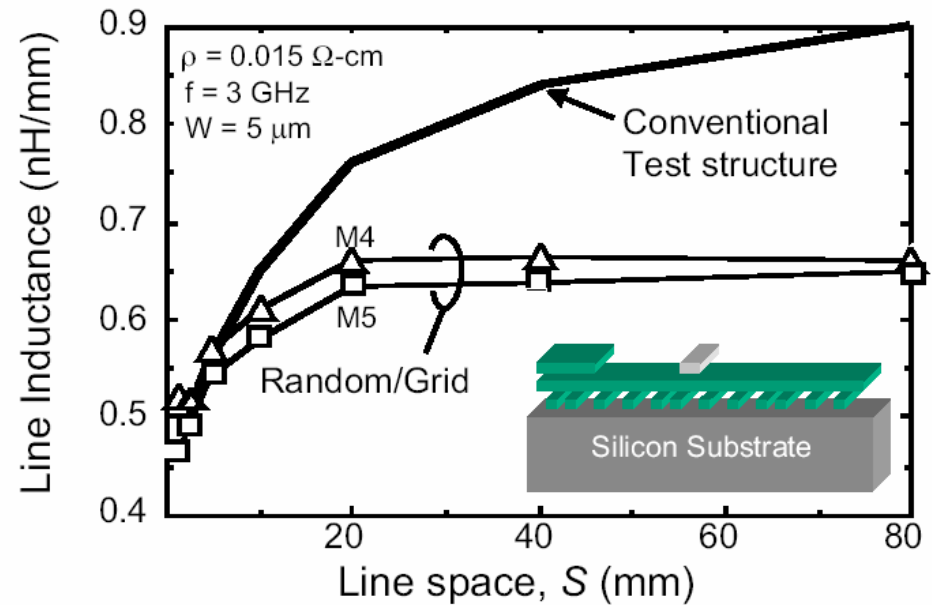
Pervasive use of diagonal wires

A typical layout  
and SEM picture

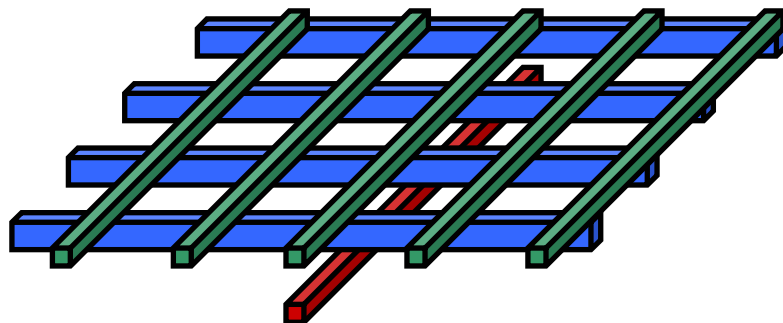


# Power Grid effects on Inductance

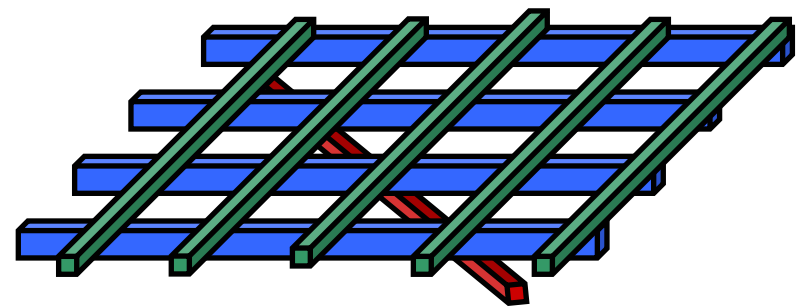
- L increases for increasing spacing because more flux is enclosed between the signal line and the return path
- In a realistic test structure, L becomes less dependent on the spacing to the intended return ground. Local lines and capacitive coupling provide alternative return paths



S. S. Wong et. al. *Proc. IEEE ISQED*, pp. 389-394, 2003

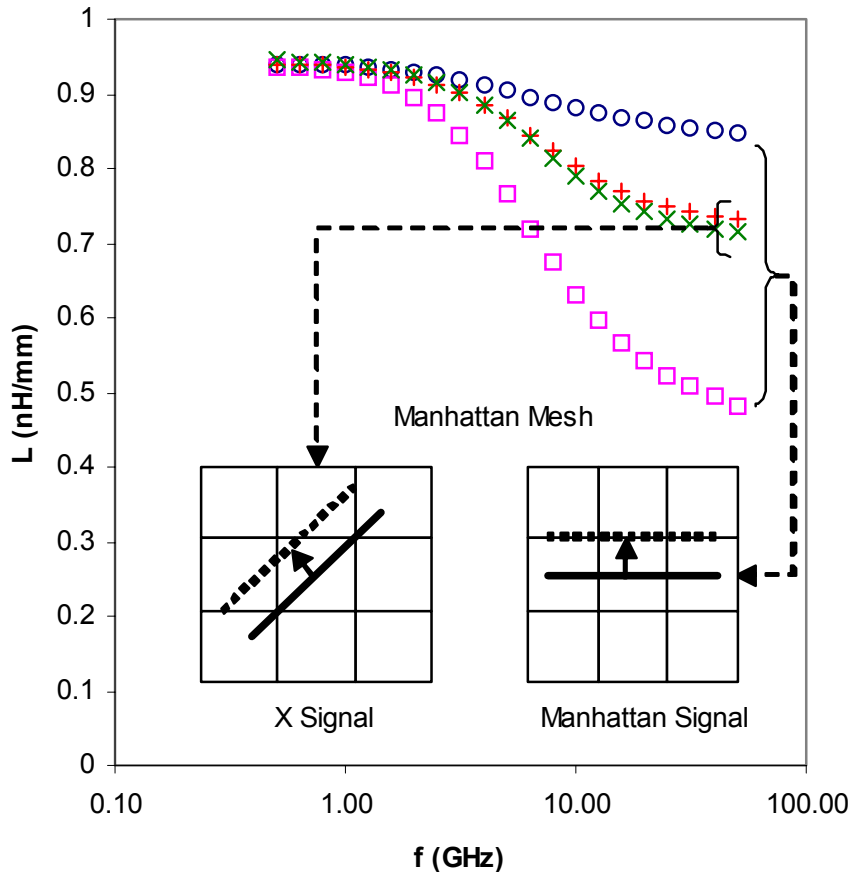


Manhattan Signal

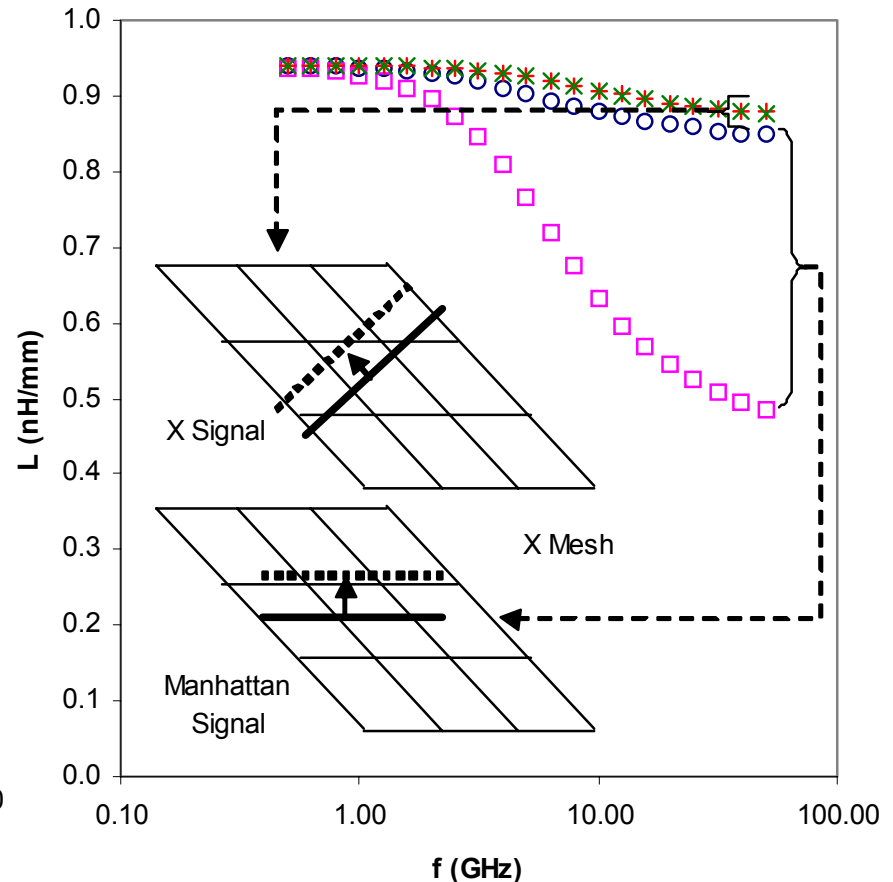


X Architecture Signal

# FastHenry Simulation - Self Inductance



Manhattan Power Grid

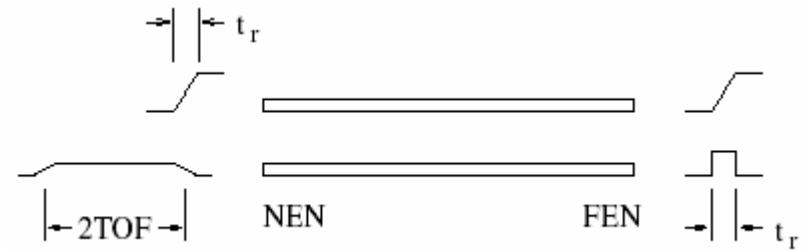
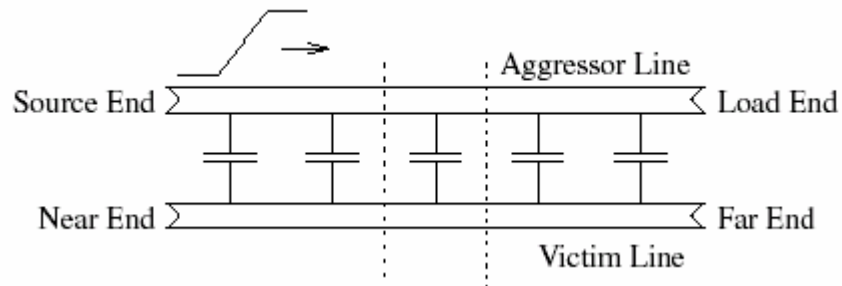


X Architecture Power Grid

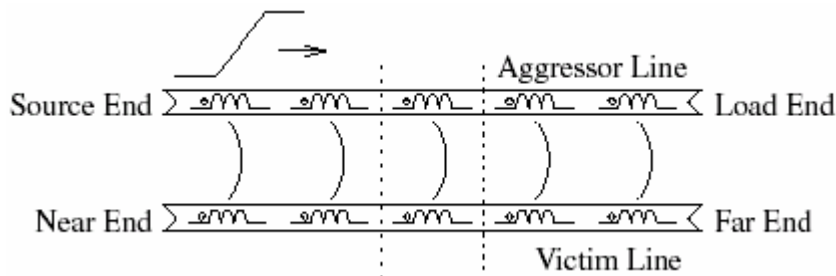
Small variation for diagonal signal line

# Crosstalk

- Capacitive Crosstalk



- Inductive Crosstalk

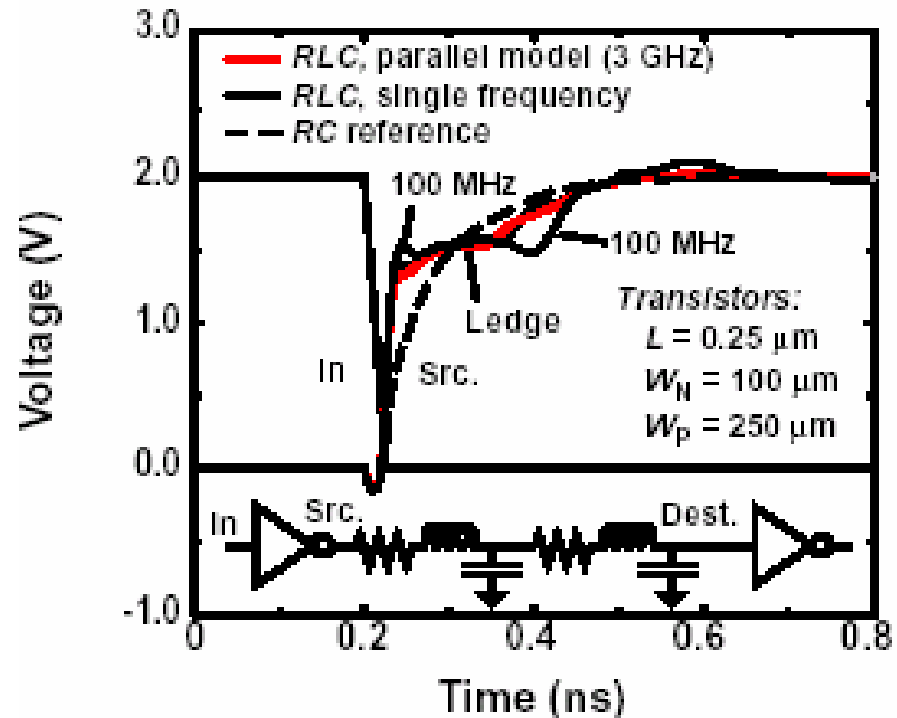


- Total Crosstalk

$$V_{NE} = K_{NE} v_0 \quad K_{NE} = \frac{1}{4} \left( \frac{C_c}{C} + \frac{L_m}{L} \right) \quad V_{FE} = \frac{1}{2} d \left( Z_0 c_c - \frac{L_m}{Z_0} \right) d \frac{dV_s}{dt}$$

# Inductive Impact at Clock Signal

- Clock carries multi-gigahertz frequency signals with short rise/fall time
- Inductive effects actually reduce rise time at near end, but increases clock skews
- Modeled as co-planar wave guide (CPWG)

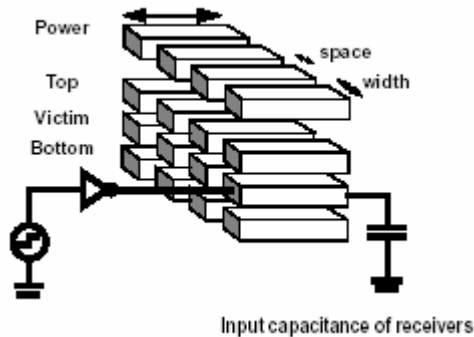


Kleveland, et al (JSCC, June, 02)

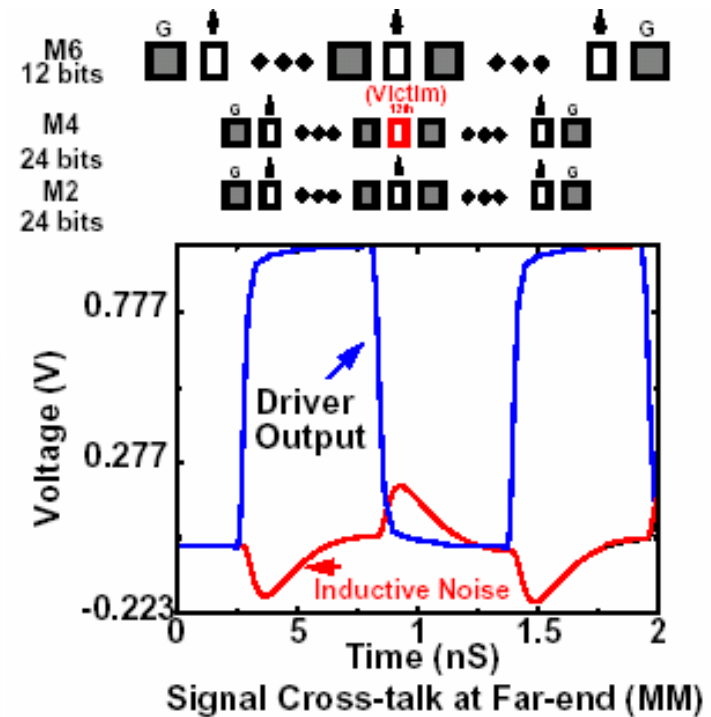
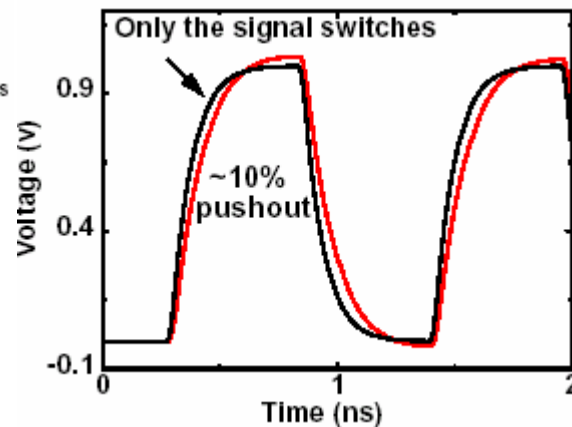
Distributed RC/RLC SPICE model, inductance is frequency dependent in the parallel model

# Inductive Impact on Bus Lines

- Simultaneous signal switch increase timing push-out
- Leading to inductive noise

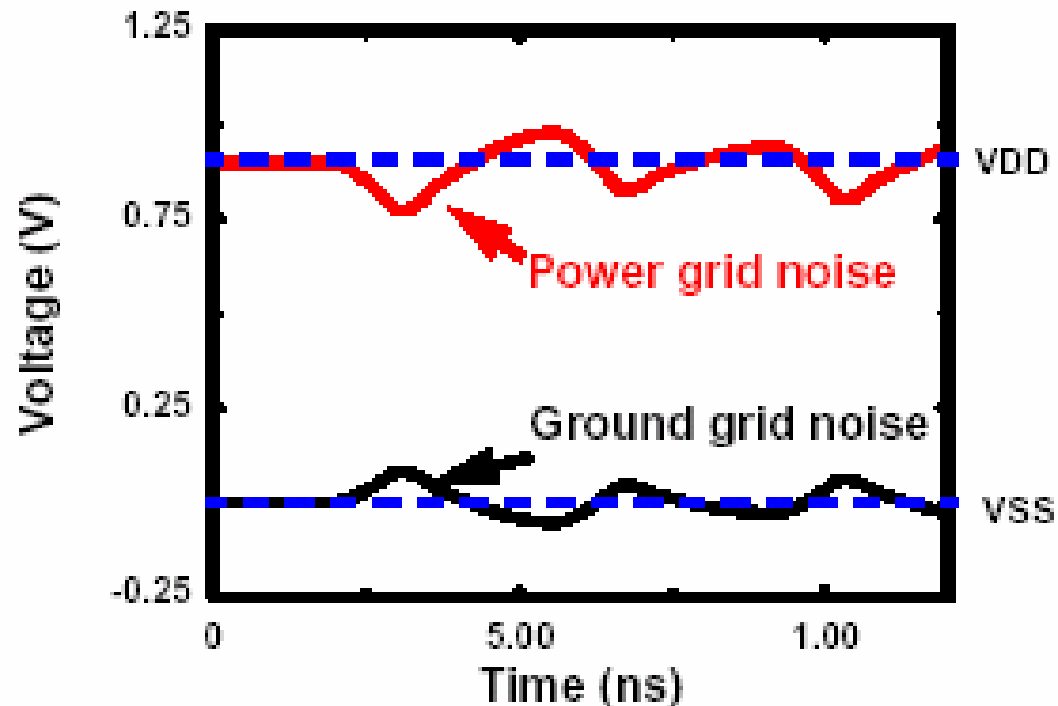


Qi, et al (GLSVLSI'03)



# Power/Ground Bounce

- On-chip power/ground grid noise is the Vdd/Vss fluctuation due to  $L di/dt$



Qi, et al (GLSVLSI'03)

## Conclusion

---

- Accurate characterization of high frequency effect such as skin effect, inductance impact on clock, buses and power/ground grid are essential in VLSI design.
- High frequency skin effects, inductance and capacitance effects and their impacts on clock, bus and power grids are studied.
- Modeling of RC delay, crosstalk and power/ground bounce are presented.
- RLC extraction and modeling in sub-90nm technologies with consideration of manufacturing effects such as electron scattering in nanometer wires, high aspect ratio wires and CMP effects

**cadence**<sup>®</sup>

*how big can you dream?*<sup>™</sup>