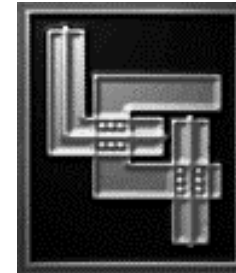


Unambiguous Extraction of MOSFET Threshold Voltage Based on the Transconductance-to-Current Ratio



Ana Isabela Araújo Cunha *
Márcio Cherem Schneider
Carlos Galup Montoro
Cleber D. C. Caetano
Márcio Bender Machado



LCI – EEL - Universidade Federal de Santa Catarina

*** DEE - Universidade Federal da Bahia**

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ACM model

Simple expressions valid in all operating regions

$$I_D = I_S (i_f - i_r) \qquad I_S = \mu C'_{ox} n \frac{\phi_t^2}{2} \frac{W}{L}$$

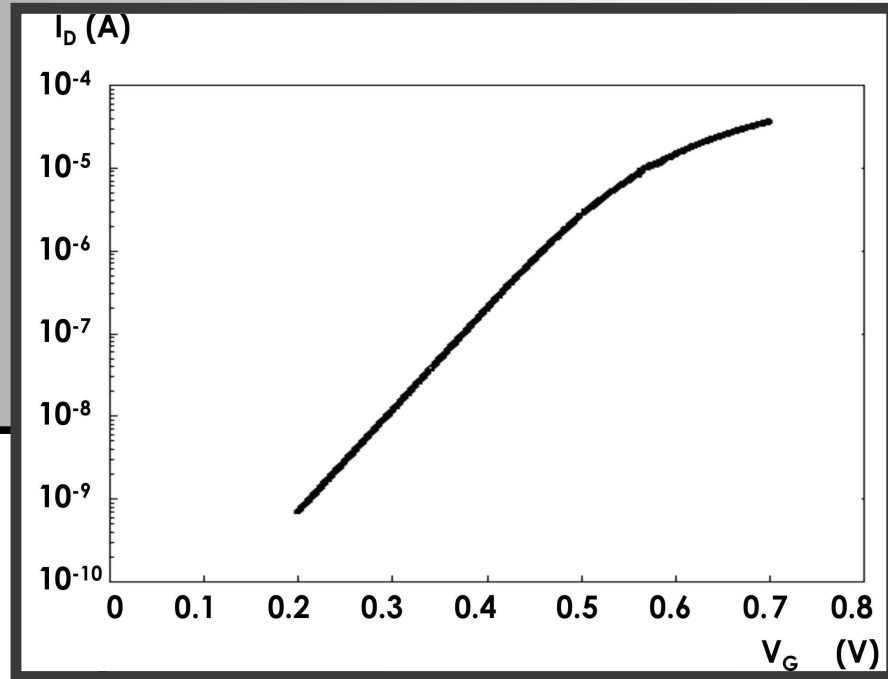
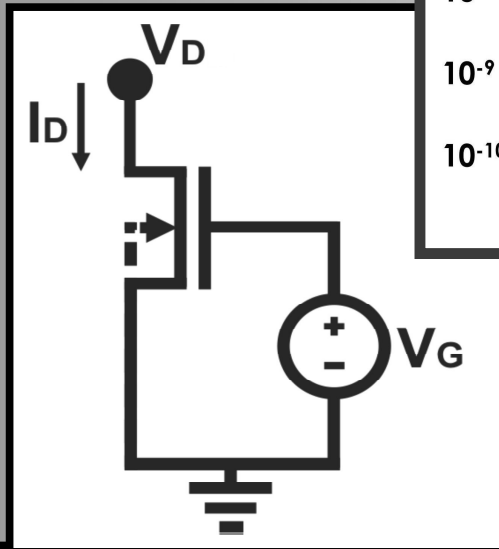
$$V_P - V_{S(D)} = \phi_t \left[\sqrt{1 + i_{f(r)}} - 2 + \ln \left(\sqrt{1 + i_{f(r)}} - 1 \right) \right]$$

$$V_P = \frac{V_G - V_{T0}}{n}$$

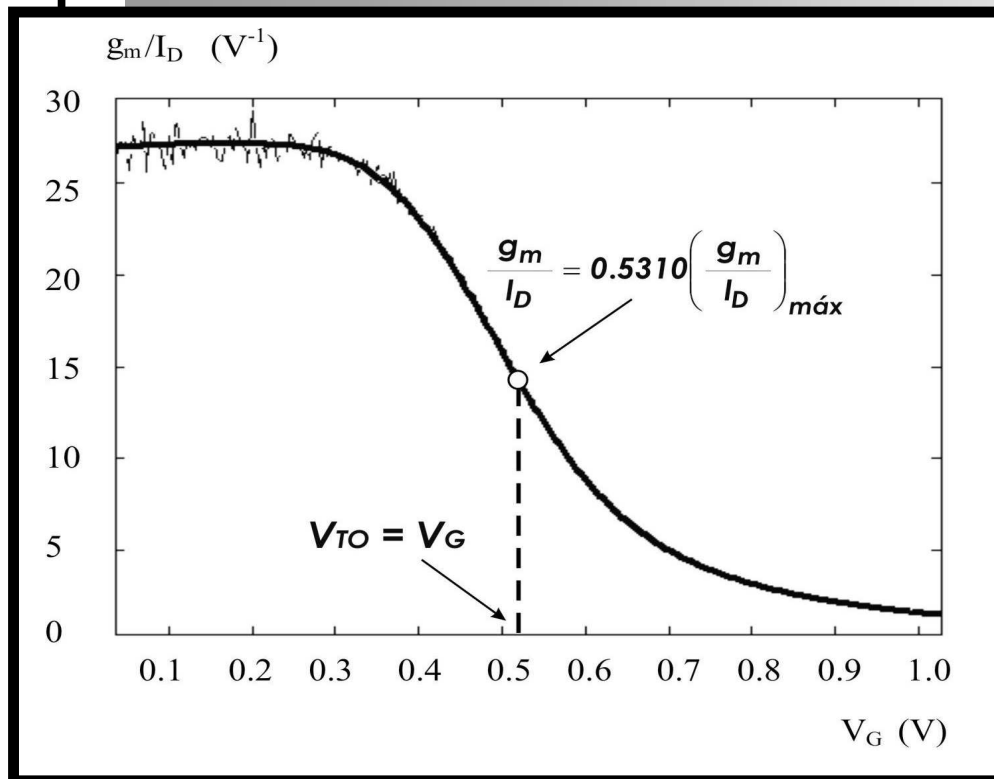
$$\frac{g_m}{I_D} = \left(\frac{g_m}{I_D} \right)_{\max} \frac{2}{\left(\sqrt{1 + i_f} + \sqrt{1 + i_r} \right)}$$

Extraction of V_T

$$V_{DS} = \phi_t/2$$



Extraction of V_T



Using $V_D = \phi_t/2$,
we find $i_r = 2.112$
for $i_f = 3$ and \Rightarrow

$$\frac{g_m}{I_D} = 0.5310 \left(\frac{g_m}{I_D} \right)_{\max}$$

Experimental results - VT

NMOS

<i>Mask channel length</i>	<i>ELR</i>	<i>SDL</i>	<i>g_m / I_D</i>	<i>CC</i>
0.2 μm	481	490	520	501
0.3 μm	483	478	510	508
0.4 μm	482	468	503	509
0.5 μm	476	463	495	504
0.6 μm	473	455	493	501
0.8 μm	462	448	483	491
2.0 μm	435	423	458	466

0.18 μm CMOS technology

PMOS

<i>Mask channel length</i>	<i>ELR</i>	<i>SDL</i>	<i>g_m / I_D</i>	<i>CC</i>
0.2 μm	-486	-490	-523	-493
0.3 μm	-453	-455	-480	-471
0.4 μm	-449	-440	-470	-468
0.5 μm	-446	-443	-468	-468
0.6 μm	-442	-433	-463	-465
0.8 μm	-438	-420	-455	-461
2.0 μm	-424	-410	-443	-451

Conclusions

- **Very simple methodology for determining the MOSFET threshold voltage**
- **Negligible influence of parasitic resistance, transversal field degradation and short-channel effects.**