Statistical simulations of oxide leakage current in MOS transistor and Floating Gate memories

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INTRODUCTION

- Oxide leakage current is a serious issue for MOS transistor and Floating Gate memories: its characterization and modeling is very important!
- In MOS transistors: 1-2 nm thick gate oxide leads to an exponential leakage current increase
  - The correct understanding of physical mechanisms in oxide degradation is crucial for technology improvement
  - SILC modeling is fundamental to forecast circuit functionality: statistical simulations are required given the large number of devices in modern ICs!

INTRODUCTION /2

- **In Flash memories:** the tunnel oxide reduction and the Flash memory scaling are strongly limited by SILC related reliability issues
  - understanding SILC dependencies on process and cell parameters improves Flash memories
  - the large capacity of today Flash devices (up to 512 Mb and increasing) demands for simulation tools with statistical capabilities

❑ Usual testing does not comply properly with SILC statistics, as SILC is either measured on large area capacitors (statistics is neglected!) or derived from V_{TH} measured on Flash cells (the number of samples is limited!)

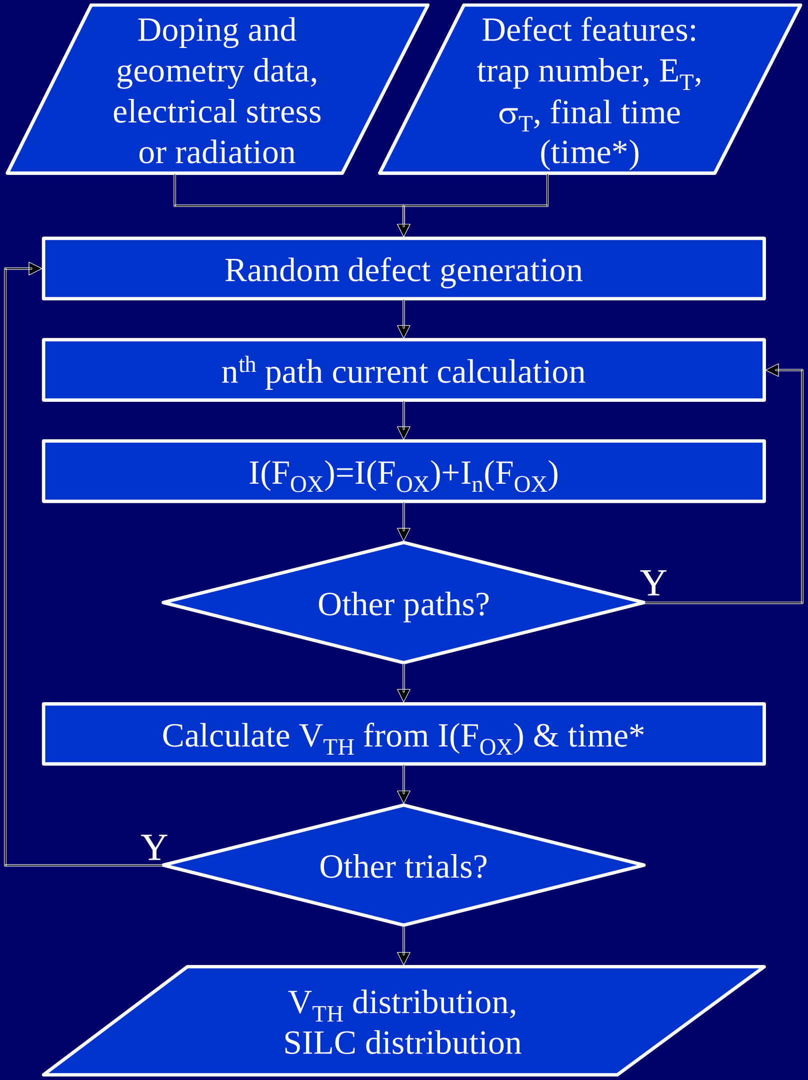
PURPOSES OF THIS WORK

- **Illustrate a physically-based statistical SILC model which allows:**
  - **to calculate leakage current distributions in gate (MOS) and tunnel (Flash) oxides**
  - **to evaluate threshold voltage (V_{TH}) distributions of Flash cells in reliability (retention) conditions**
  - **to correlate (statistically) oxide defect characteristics to SILC and Flash memory V_{TH} distributions**
  - **to predict T_{OX} scaling effects on Flash memory data retention**

1 L. Larcher, IEEE Transaction on Elect. Dev., Vol. 50(5), pp. 1246-1253

SIMULATION MODEL

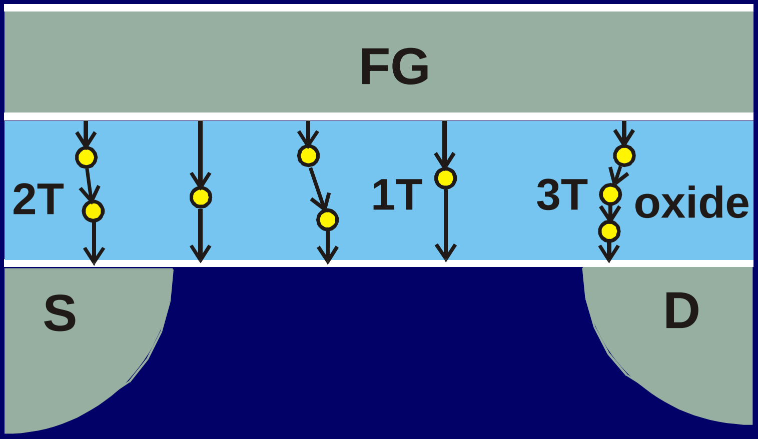
- **Block diagram of model for SILC and V_{TH} simulation**
- **This model is based on the physical-statistical SILC model [1]**
- **This model includes a new V_{TH} calculation procedure, allowing to evaluate V_{TH} distribution in retention conditions**



SILC MODEL

- Features of the proposed physical-statistical SILC model:

1. statistical computation capabilities
2. conduction mechanism = multi-phonon trap-assisted tunneling: trapped electrons are coupled to oxide phonons, resulting in a series of virtual states broadening the energy trap level
3. SILC contributions driven by percolation paths are taken into account



SILC MODEL /2

- The model calculates the total leakage current by summing SILC contributions driven by every oxide paths formed by one or more aligned traps
- Under steady-state conditions, the rate electrons pass through a *n*-trap paths is

$$R_j = \frac{1}{\max_j\left(\tau_{c,j} + \tau_{e,j}\right)}$$

- $\tau_{c,j}$ ($\tau_{e,j}$) is the time constants of the capture (emission) of electrons by (from) the j^{th} trap

$$I_{SILC} = \sum_j q \cdot R_j$$

SILC MODEL /3

- Capture (emission) time constants are given by the maximum of single phonon time constants, evaluated over discrete energies $E_{j,n}=E_{C,j}+n \cdot E_p$
  - $E_{C,j}$ = conduction band when j = 0 or j = trap_number+1
  - $E_{C,j}$ = trap energy level when 0 < j < trap_number+1
  - E_P = effective phonon energy

$$\tau_{c,j} = \max_n\left(\tau_{c,j,n}\right) = \max_n\left[N\left(E_{j-1,n}\right) \cdot f\left(E_{j-1,n}\right) \cdot P_T\left(E_{C,j} - E_{j-1,n}, F_{j-1,j}, D_{j-1,j}\right) \cdot Ca_{j,n}\right]$$

$$\tau_{e,j} = \max_n\left(\tau_{e,j,n}\right) = \max_n\left[N\left(E_{j+1,n}\right) \cdot P_T\left(E_{C,j} - E_{j,n}, F_{j,j+1}, D_{j,j+1}\right) \cdot Em_{j,n}\right]$$

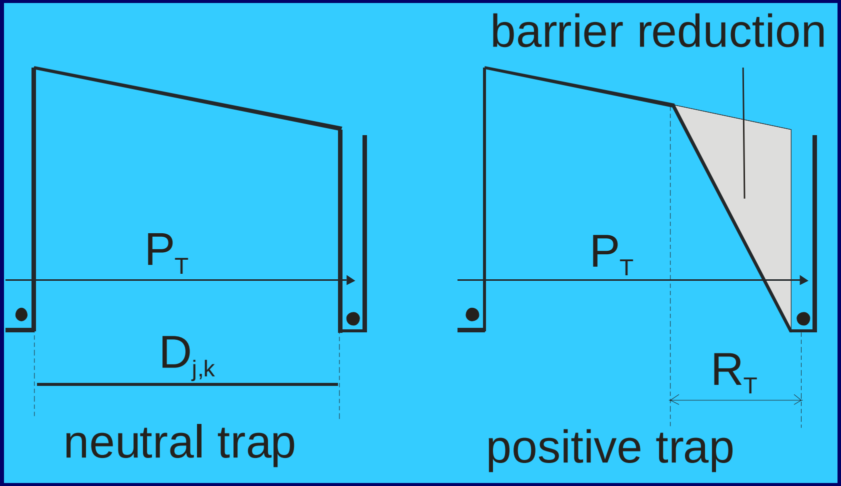
  - $N(E_{j,n})$ = density of states
  - $f(E_{j,n})$ = state (Maxwell-Boltzmann) occupation probability
  - $Ca_{j,n}$ ($Em_{j,n}$) = trap capture (emission) rate
  - P_T = tunnel probability ….

TUNNEL PROBABILITY

$$P_T\left(E_j - E_i, F_{j,i}, D_{j,i}\right)$$

- $D_{j,i}$ = distance between jth and ith trap
- $F_{i,j}$ = equivalent oxide field between jth and ith trap

- Electron tunneling probability P_T is calculated by applying the **WKB method**
  - Tunneling through positively charged traps is simply accounted for
  - The oxide barrier reduction is modeled by a linear decrease of the conduction band profile when the distance from the trap is smaller than its **capture radius, R_T**



STATISTICAL CAPABILITIES

- To enable statistical simulations, a random generator supplying spatial and energy defect coordinates is integrated with the SILC model

- An ad-hoc procedure calculates leakage current contributions driven by every trap, checking if whatever j^th trap belongs to a percolation path

1. $R_{j,anode}$ (i.e. the rate electrons pass from the trap to the anode) is compared to $R_{j,k}$, k being the generic trap located between the j^{th} one and the anode

2. If $\max(R_{j,k}) > R_{j,anode} \Rightarrow j^{th}$ and k^{th} traps belong to the same percolation path

This procedure is repeated for every trap!

V_{TH} CALCULATION

- **SILC induced V_{TH} reduction occurring in Flash memories after electrical stress or radiation can be calculated as follows:**

1. **I_G-F_{OX} curves is provided by SILC model, F_{OX} being the oxide field**
2. **From the F_{OX}-V_{FG} relation (calculated by taking into account both polysilicon depletion and quantization effects), I_G-V_{FG} curve is determined**
3. **Floating Gate voltage after t* retention time, $V_{FG,FIN}$, is determined by solving**

$$\frac{t^*}{C_T} = \int_{V_{FG,IN}}^{V_{FG,FIN}} \frac{dv_{fg}}{I_G\left(v_{fg}\right)}$$

C_T and $V_{FG,IN}$ being the total FG capacitance and the initial FG voltage

V_{TH} CALCULATION /2

4. Final threshold voltage $V_{T,FIN}$ can be calculated from basic FG device equation,

$$V_{T,FIN}=V_{T0}-V_{FG,FIN}/\alpha_G,$$

V_{T0} and α_G being the UV threshold voltage and the control gate capacitive coupling

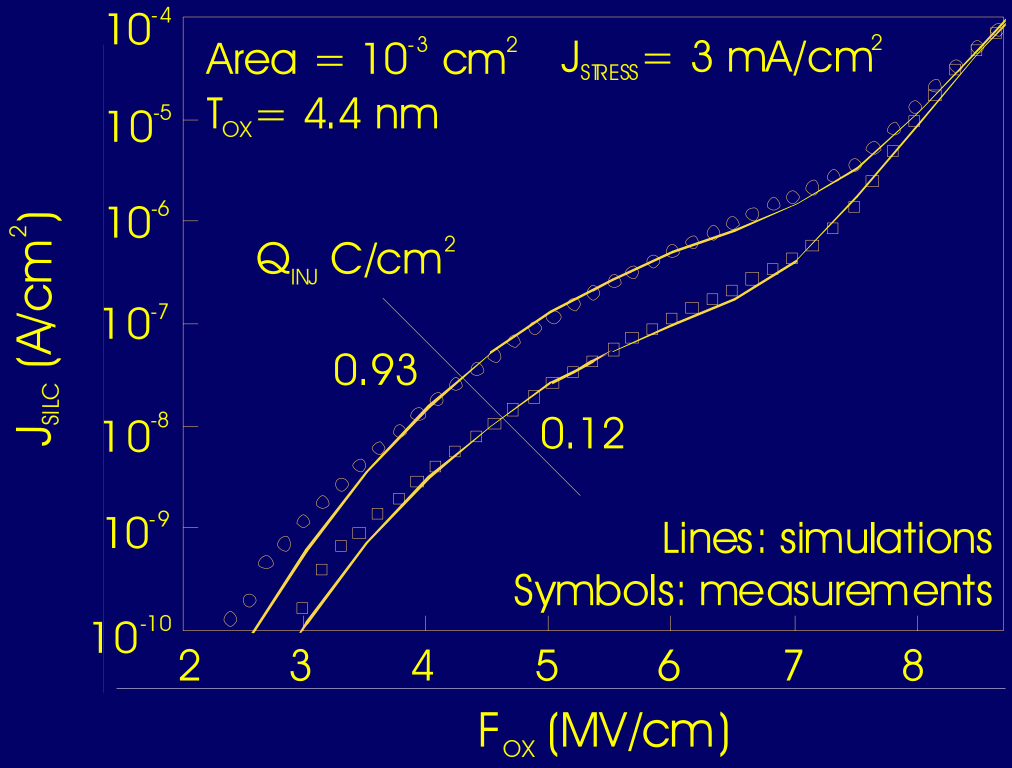
- V_T distribution can be calculated by repeating this procedure for every I_G-F_{OX} curve, that are statistically generated in the same defect conditions

SIMULATIONS RESULTS

- Capabilities of the model allowed to successfully simulate:
  - SILC on capacitors with different oxide thicknesses (T_{OX}= 3.3–10.5 nm)
  - V_{TH} distributions measured on unbiased Flash cells irradiated by heavy ions (Ag, I)
  - V_{TH} distribution in Flash cells that underwent P/E stresses after ten years (retention)

SILC ON CAPACITORS

- **SILC statistical simulations: $N_T \cdot Area \cdot T_{OX}$ defects are randomly generated within the oxide: $N_T = 10^{16}$ and 10^{17} cm^{-3} are the defect density**
- **Excellent fit of experimental SILC after CCS!**



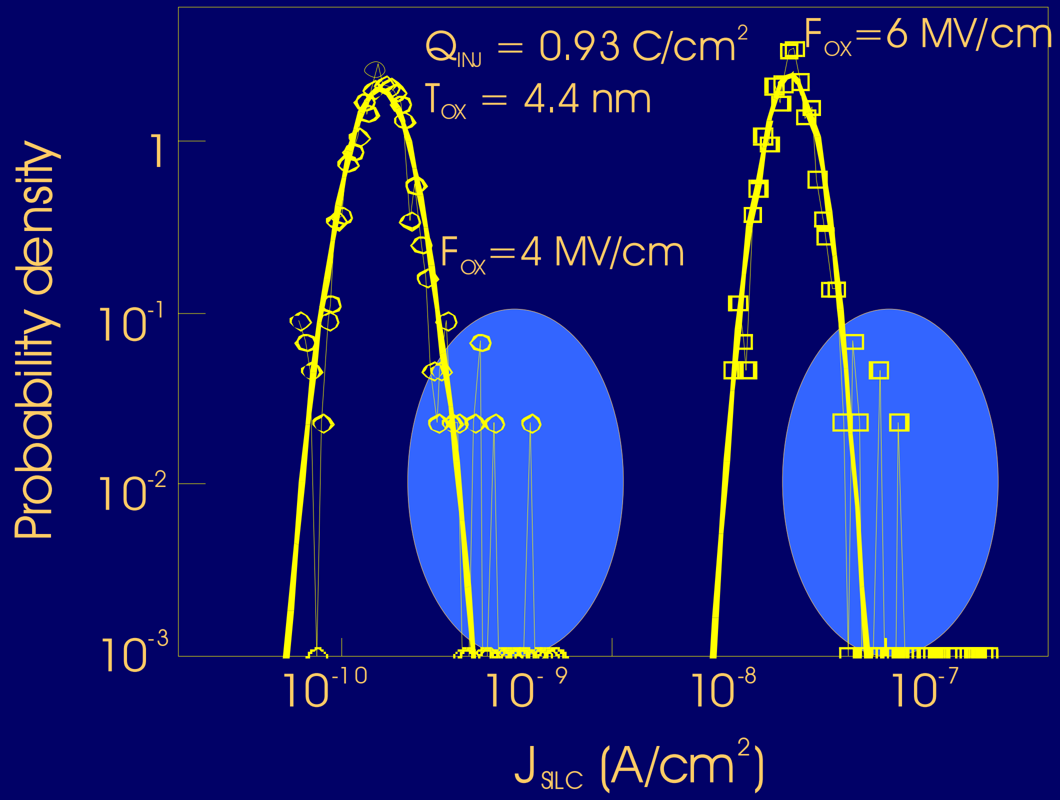
SILC ON CAPACITORS /2

- **Spatial coordinates and energy levels of defects are generated by assuming a uniform and a Gaussian distribution, respectively**
  - **E_T = 2.4 eV (below the oxide conduction band) and ΔE_T = 0.15eV are the mean and the standard deviation of the Gaussian energy distribution**

- ☐ **Usually, SILC was simulated by taking into account just the average defect contribution, $N_T \cdot \sigma_T$**
  - ☐ **This approach works with large area devices, but it falls when considering small area samples**
  - ☐ **With smaller area, total SILC is more sensitive against single spatial-energy trap variations!**

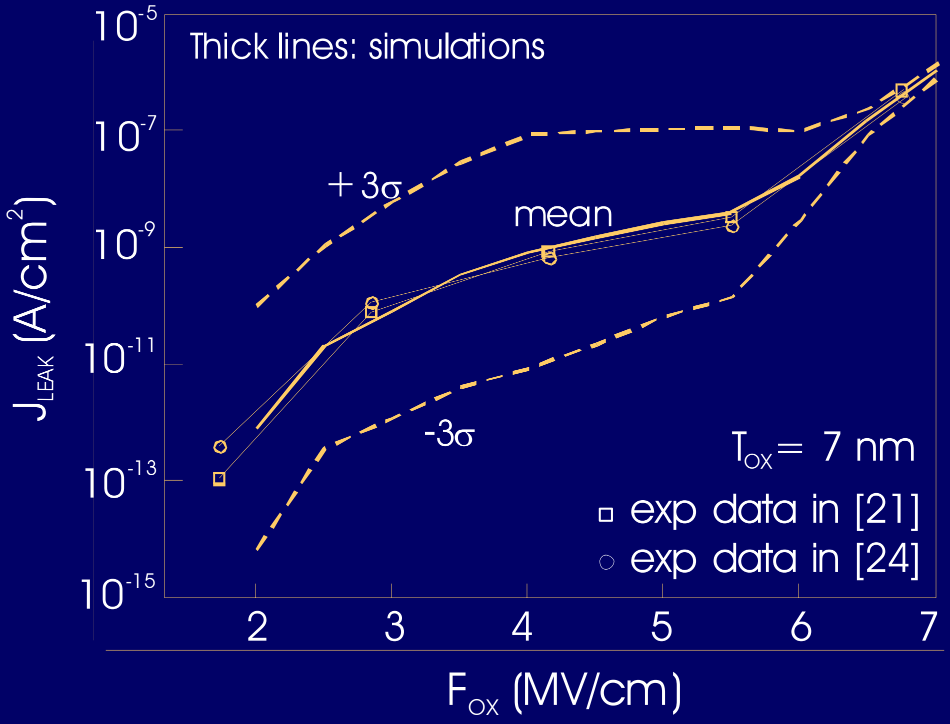
SILC ON CAPACITORS /3

- **SILC standard deviation increase** when device area scales down (device area = 1 μm^2)!
- SILC probability densities are fitted well by a **log-normal curve**, although tails appear at high J_{SILC}



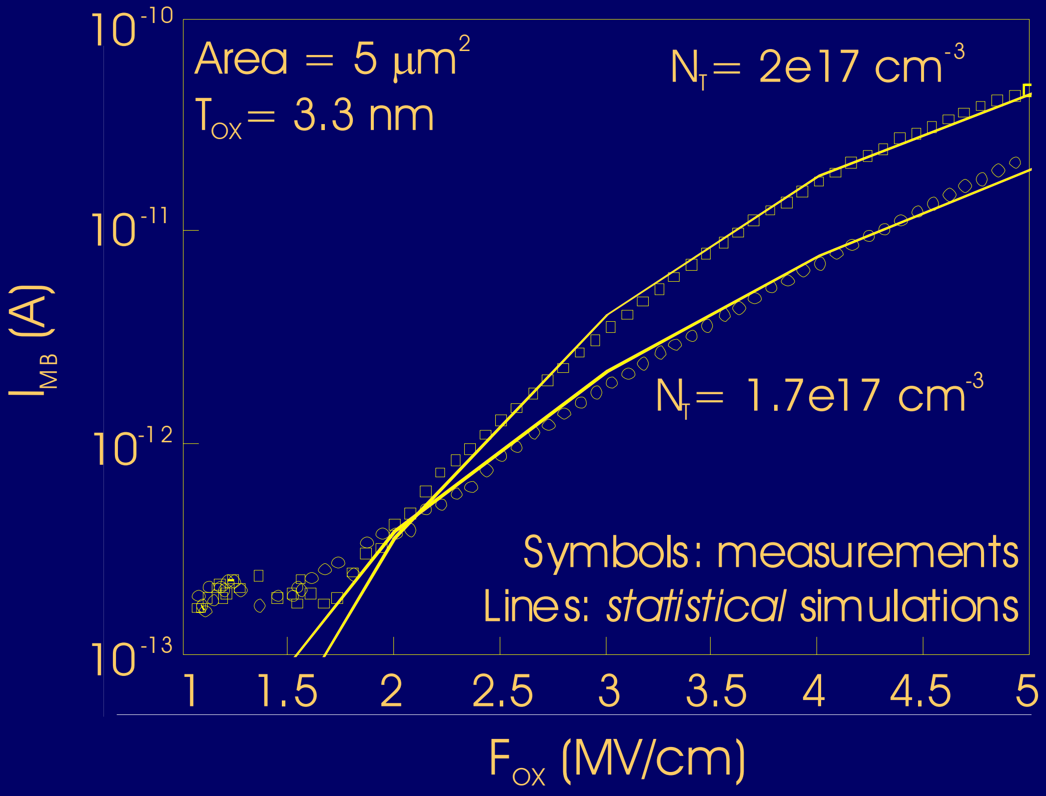
SILC ON CAPACITORS /4

- Simulations of SILC across a T_{OX}=7nm Flash tunnel oxide (10^3 simulation trials)
  - Mean reproduces accurately experimental curves
  - Standard deviation accounts for statistical variations among samples



SILC ON CAPACITORS /5

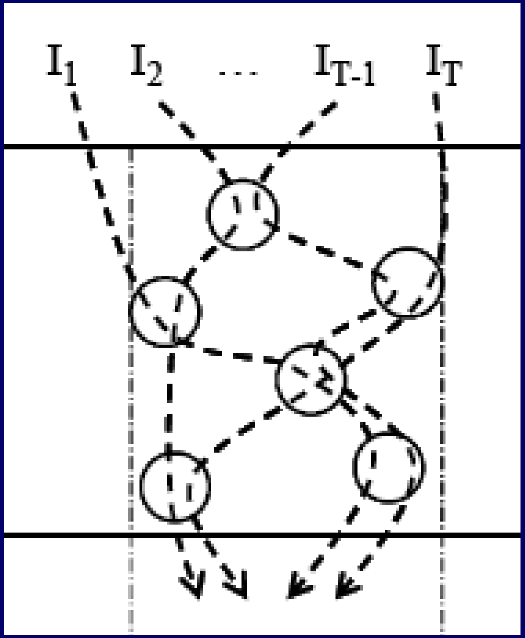
- **Micro-breakdown current** **simulations on T_{OX}=3.3nm capacitors agrees nicely with experiments**
- **Uniform distribution of** **neutral traps** **are assumed ($\sigma_T=10^{-14}$ cm^2)**



V_{TH} DISTRIBUTION

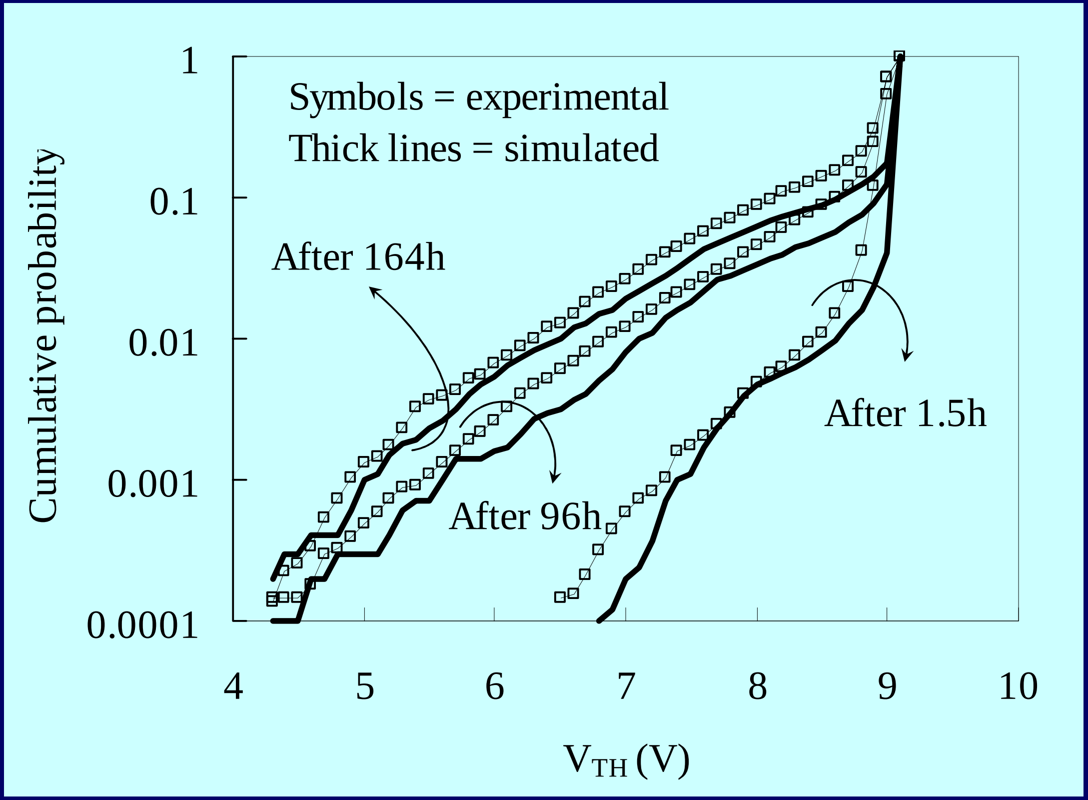
- **Flash cells hit by a heavy ion feature degraded data retention properties [2]**
  - **V_{TH} cumulative distribution shows a large tail at low threshold voltage increasing with time**
  - **V_{TH} reduction is driven by defects generated by ion passing through the oxide**
  - **The model is extended to account for the radiation defect generation process**
  - **Defects are concentrated near the ion track, i.e. in a cylinder with a 12 nm diameter [2]**

[2] L. Larcher et al., *IEEE Transaction on Nuclear Science*,Vol. 50(6), pp. 2176-2183, 2003



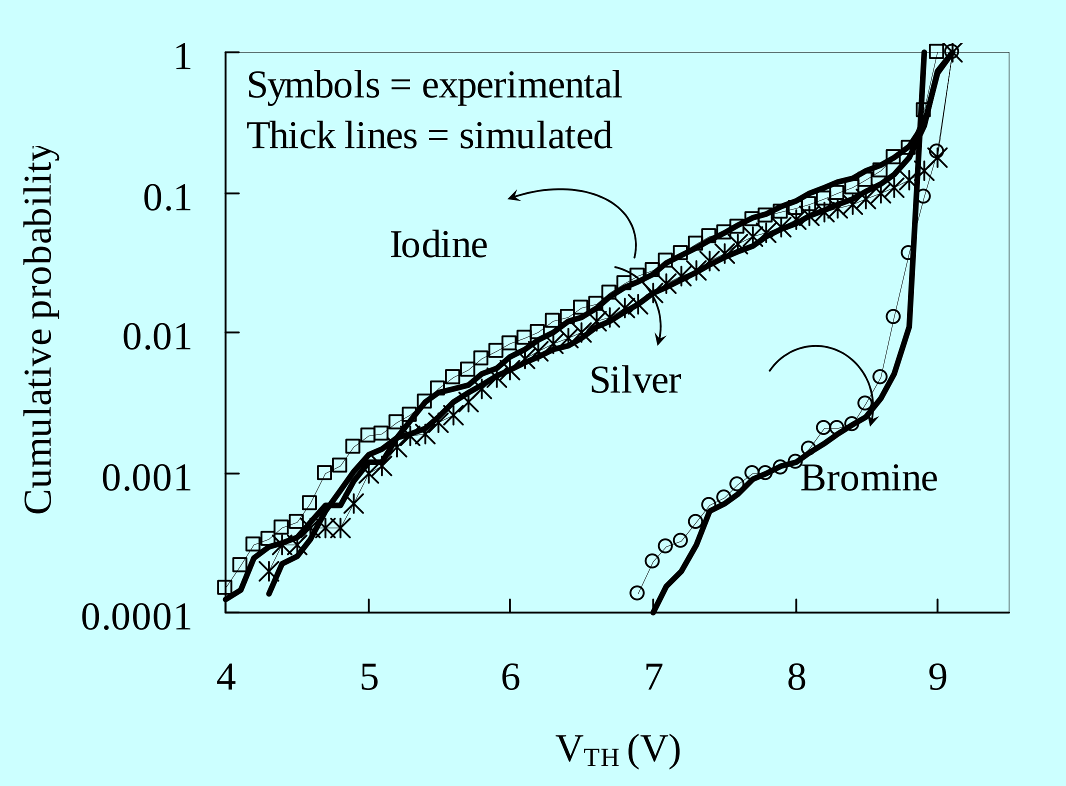
V_{TH} DISTRIBUTION /2

- V_{TH} distribution of unbiased T_{OX}=10nm Flash after a Iodine irradiation (E=286 MeV; LET=64MeV/cm^{2}mg)
- Nice fitting by assuming 12 defects generated in the ion track, a cylinder with 12 nm diameter



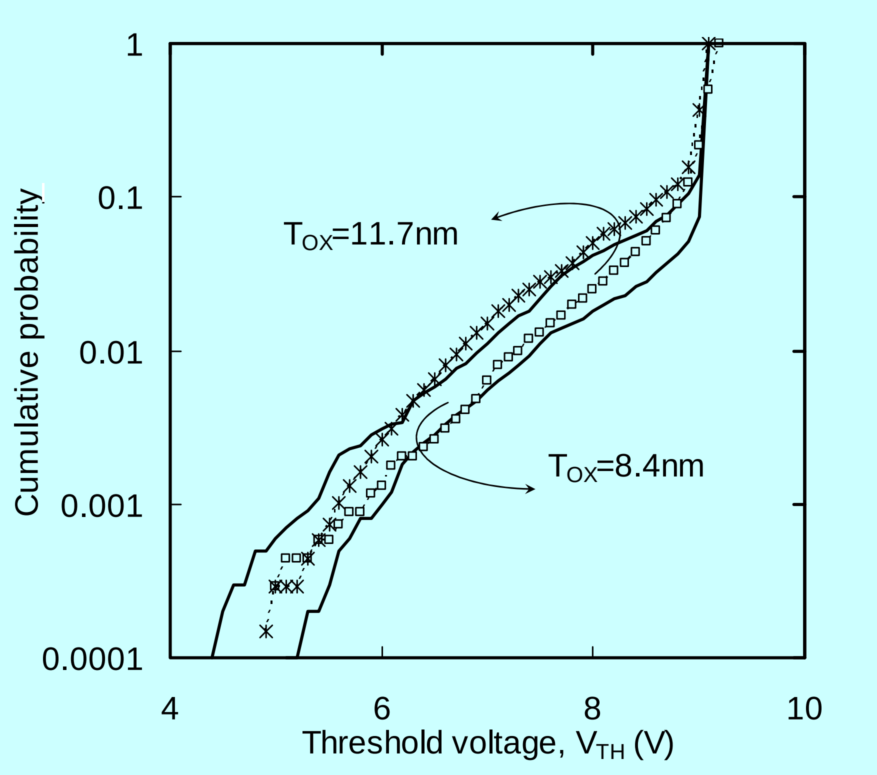
V_{TH} DISTRIBUTION /3

- **Excellent fitting** also with different ions!
- Interestingly, **defect number** (12 for I, 11 for Ag, 5 for Br) **depends** (as expected) to the **ion Linear Energy Transfer**



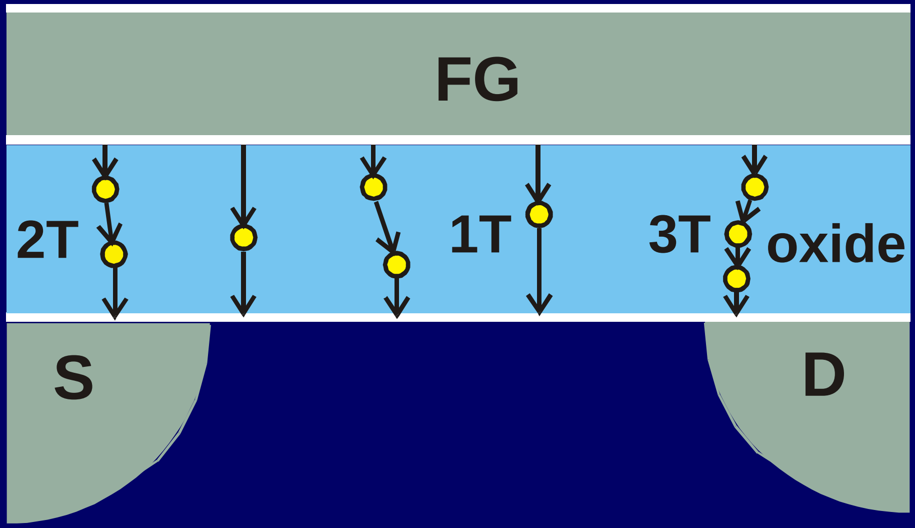
V_{TH} DISTRIBUTION /4

- **The model works well** also for Flash cells irradiated by Iodine **having different T_{OX}!**
- **Defect number** (~6 for T_{OX}=8.7nm and ~14 for T_{OX}=11.7nm) depends on the oxide thickness



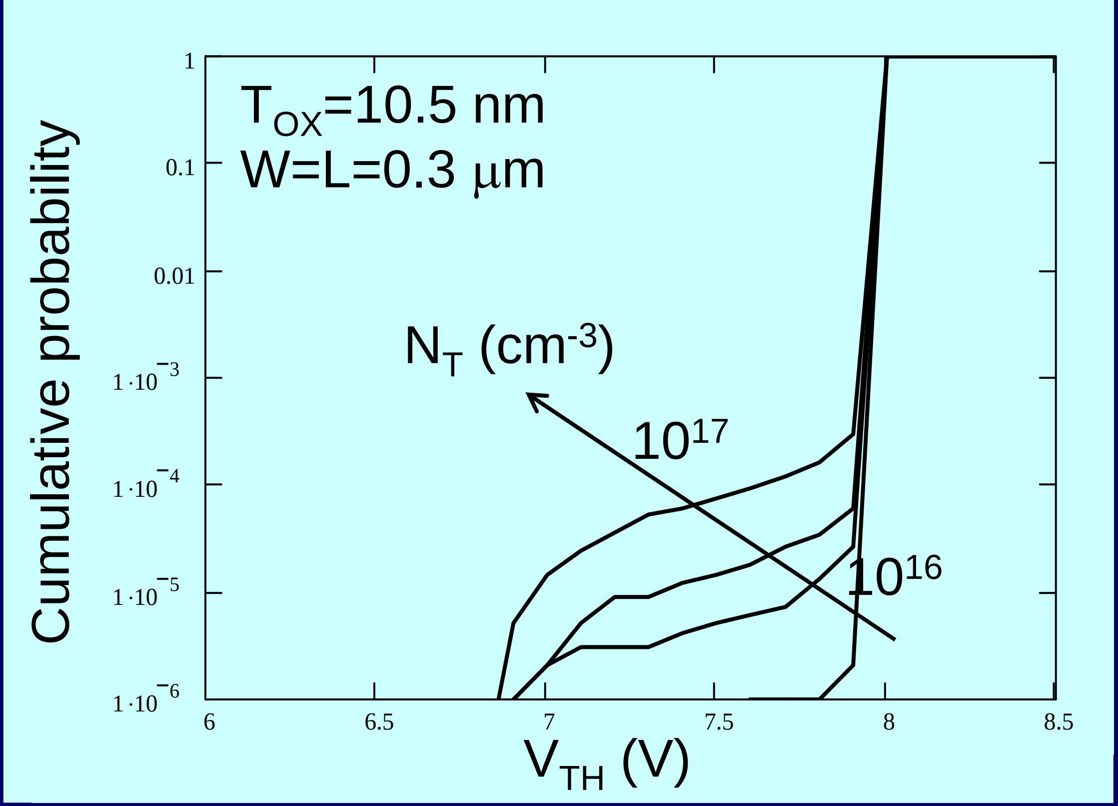
V_{TH} DISTRIBUTION /5

- This model allows to investigate reliability of Flash subjected to conventional P/E stresses
- Defects are uniformly generated in tunnel oxide to account for the P/E oxide degradation
- Largest V_{TH} reduction (fast/moving bits) could be correlated to defect features (N_T, σ_T, E_T, ..)



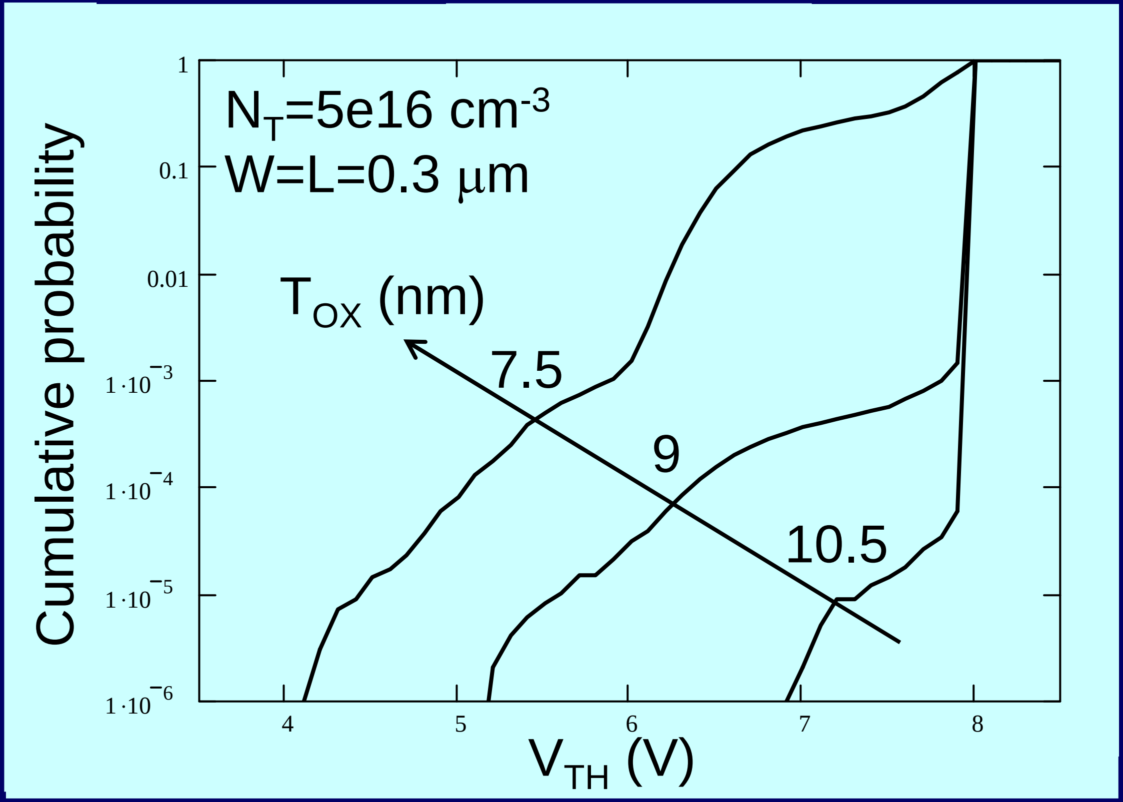
V_{TH} DISTRIBUTION /6

- V_{TH} distribution (10^6 simulation trials) of 0.18μm Flash cells left unbiased for 10 years
- Very few cells feature V_{TH}<8V, which is due to the large SILC driven by 3-trap percolation paths



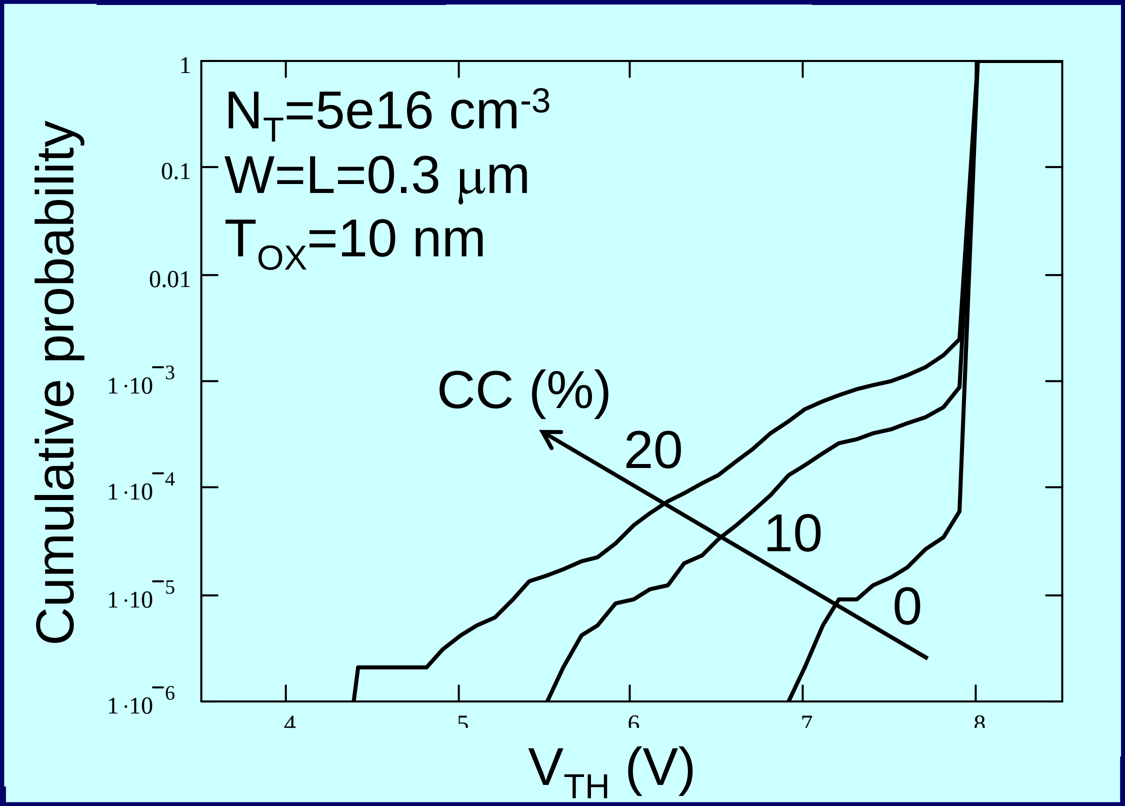
V_{TH} DISTRIBUTION /7

- **Strong V_{TH} degradation** on scaling T_{OX}, due to **exponential SILC** increase
- Statistical V_{TH} tail increase prediction helps to scale reliably Flash cells



V_{TH} DISTRIBUTION /8

- Defects can be generated also by a correlated process
- Tails at low V_{TH} strongly increases with the defect **Correlation Coefficient, CC**



CONCLUSIONS

- The model presented here is physical and statistical
- It reproduces very accurately SILC across gate-tunnel (T_{OX}=3.3–10.5nm) oxides and V_{TH} in Flash cells after various stresses (electrical, radiation)
- Simulation times are not critical: 2 hours on a Pentium 4 PC for 10^7 simulation trials
- It is an important tool for Flash technology improvement as it allows:
  - To correlate defect features to V_{TH} statistics
  - To identify physical mechanisms responsible of fast/moving bits
  - To predict oxide scaling effects