

Airgap and Line Slope Modeling for Aluminum/TEOS Interconnect

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Agenda

- **Motivation:** Why this work is done
- **Airgap formation:** Airgaps form between Aluminum lines
- **Airgap characterization:** How to characterize airgaps versus space
- **Airgap properties:** General trends observed about airgaps
- **Airgap modeling:** How airgaps are modeled using field solver
- **Impact of airgap on capacitance:** Airgaps reduce capacitance
- **Airgaps and 3D models:** How to simplify exact 2D model to simplified 3D
- **Line slope characterization:** How to characterize line slope versus space
- **Line slope modeling:** How to model line slope using field solver
- **Impact of line slope on capacitance:** Line slope increases capacitance
- **Conclusion**

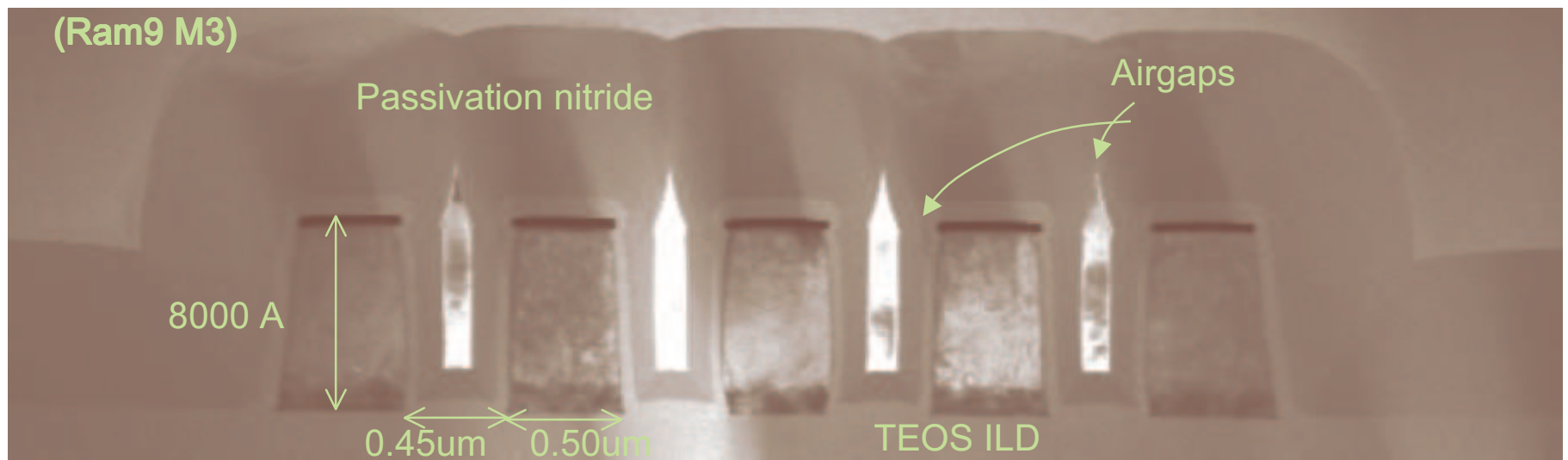
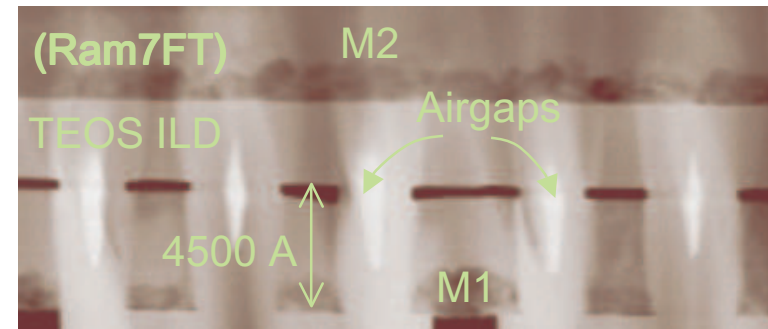
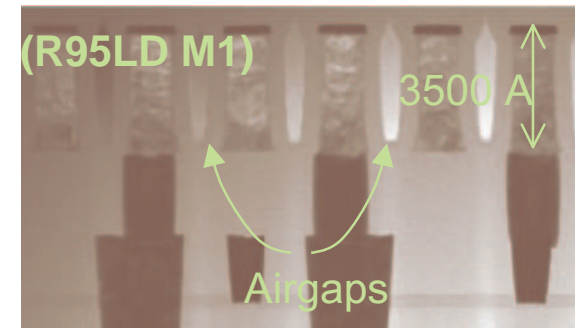
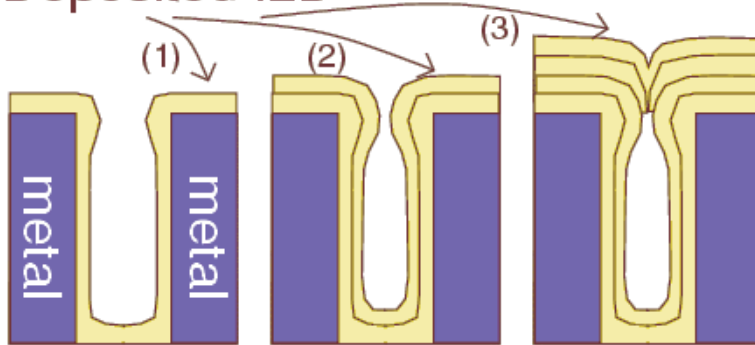
Motivation

- Interconnect **delay** (RC) is a significant component of total delay for logic and memory products
- Interconnect **power consumption** also significant component of total power
- Interconnect includes both **routing RC** (e.g., clock, data, decoder) and **3D connectivity** for memory cells (e.g., bitline or wordline for SRAM) and standard cells (e.g., in or out for AND, OR, ... gates)
- Interconnect impact is more **significant for recent and future technologies** since lines get closer and coupling capacitance increases
- To achieve certain technology node, many **process steps** are applied to metal, which result in byproducts such as **airgaps, line slope**, undercut, etc
- Process byproducts have significant **impact on line capacitance**
- Goal is to ***model impact of airgaps and line slope on capacitance***

Airgap Formation

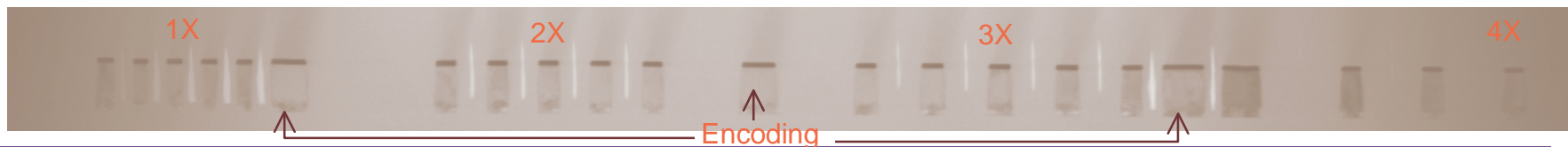
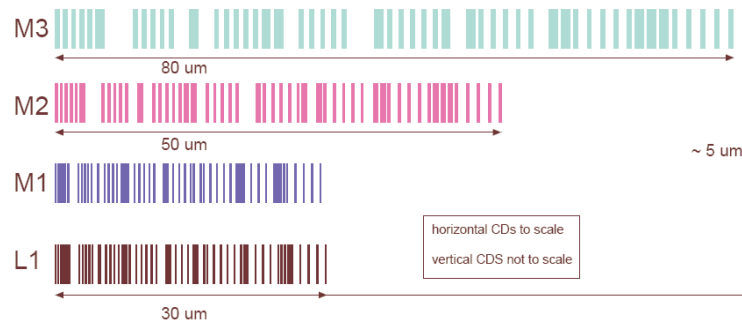
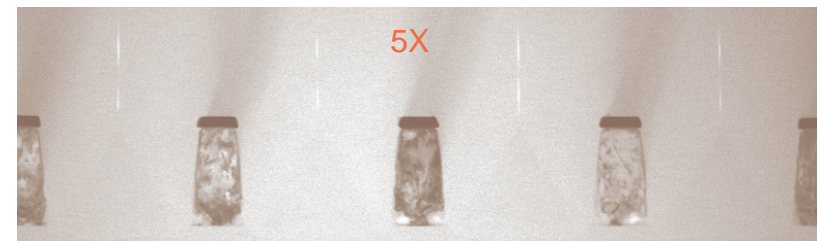
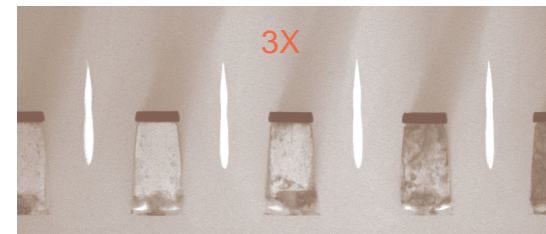
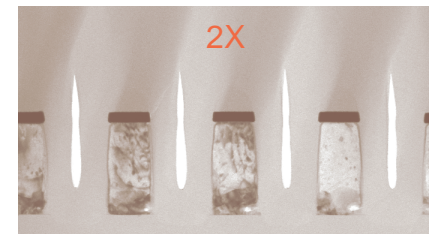
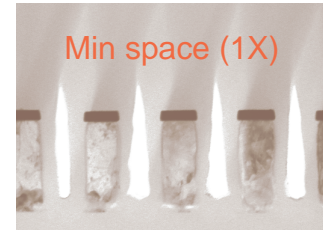
- Airgaps form between different metals
- Airgaps form in oxide as well as nitride

Deposited ILD



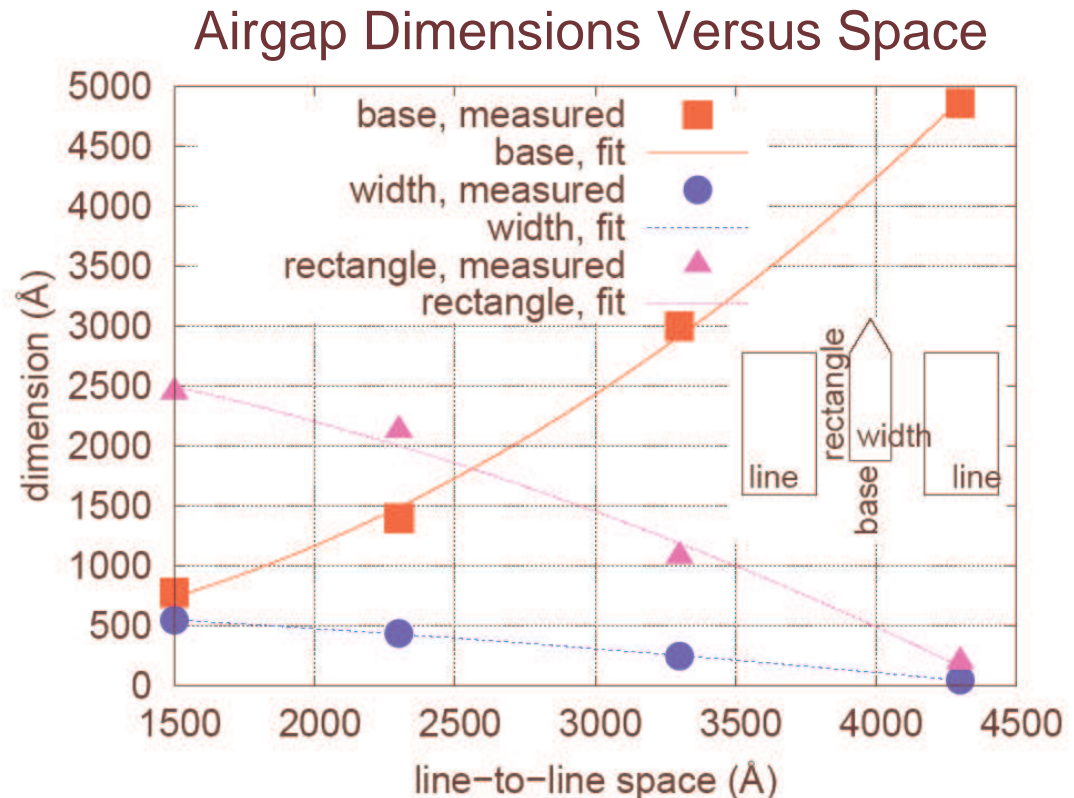
Airgap Characterization

- An **etest module** is designed with lines at different spaces
- Some **encoding** is added to be able to tell which space at hand
- **Single SEM** image taken of structure showing void dimensions at different spaces
- **Dimensions** and location of each metal void measured and **fit into a polynomial**



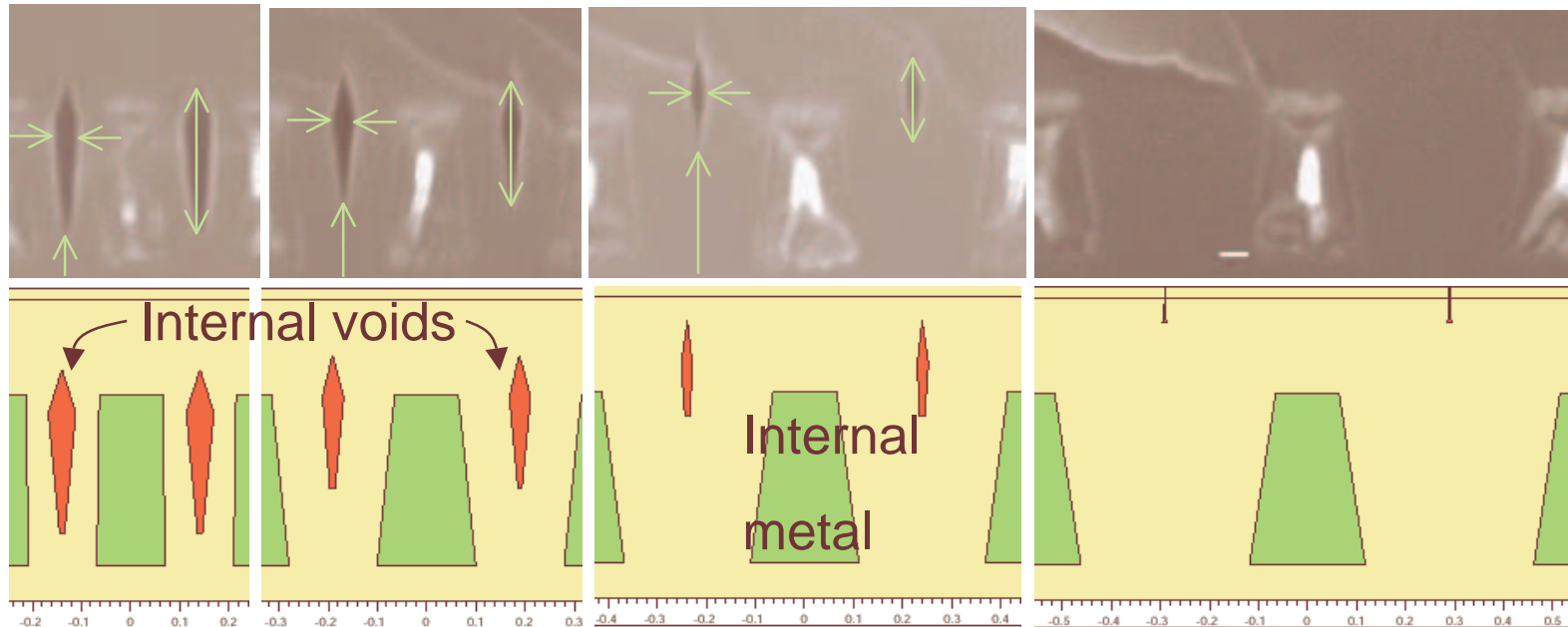
Airgap Properties

- Void **width** maximum at minimum space
- Void width decreases versus space
- Void **altitude** (base) moves up as a function of space
- **Rectangular** portion of void decreases versus space
- Higher **aspect ratio** (thicker metal) results in larger airgaps
- Void CDs **non linear** versus space – need at least quadratic fit

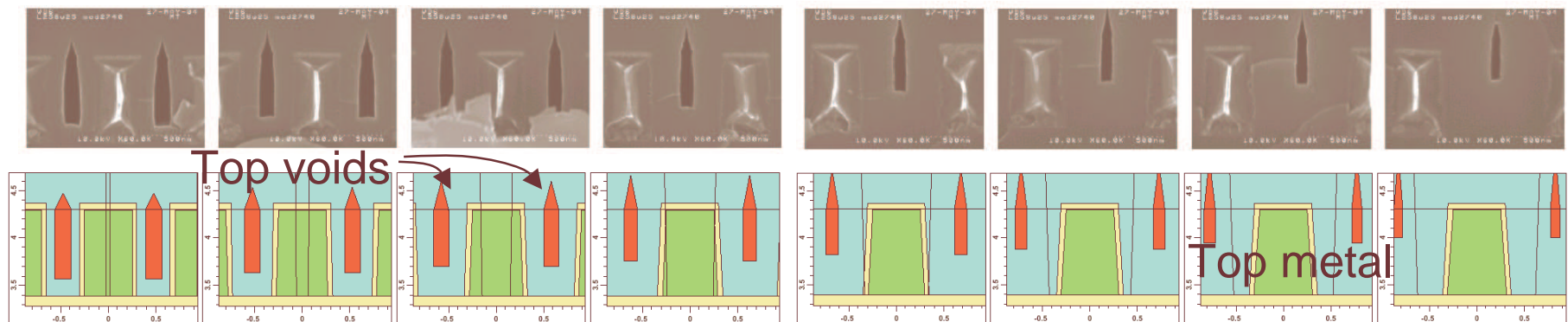


Airgap Modeling

- Internal metal airgap modeling compared to silicon (TEOS ILD)



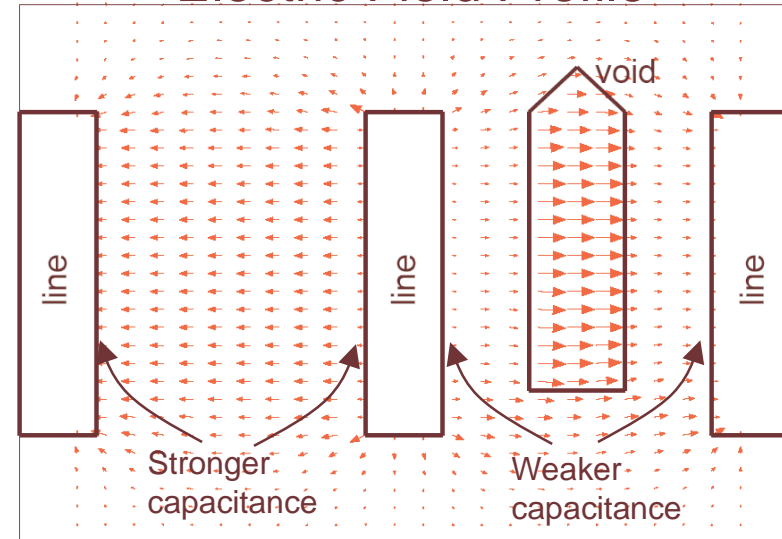
- Top metal airgap modeling compared to silicon (top passivation nitride)



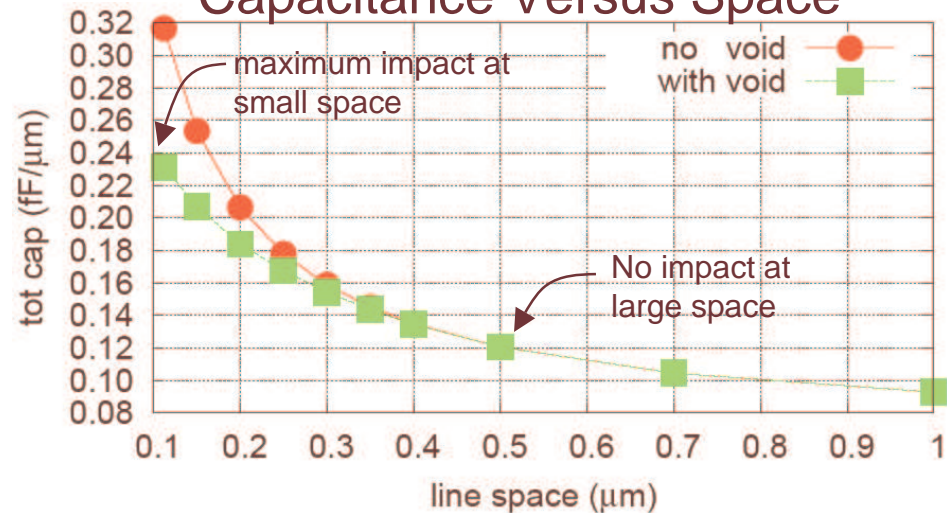
Impact of Airgap on Capacitance

- Airgap modeled with **dielectric constant of 1**
- Corresponding electric field and potential calculated
- Net result is **capacitance reduction** (~ 25% at small space)
- **At large space voids are gone** and no impact on capacitance
- Airgaps embedded in a high-k material (e.g., top passivation nitride, $k=7.5$) have larger impact than those embedded in oxide ($k=3.9$)

Electric Field Profile

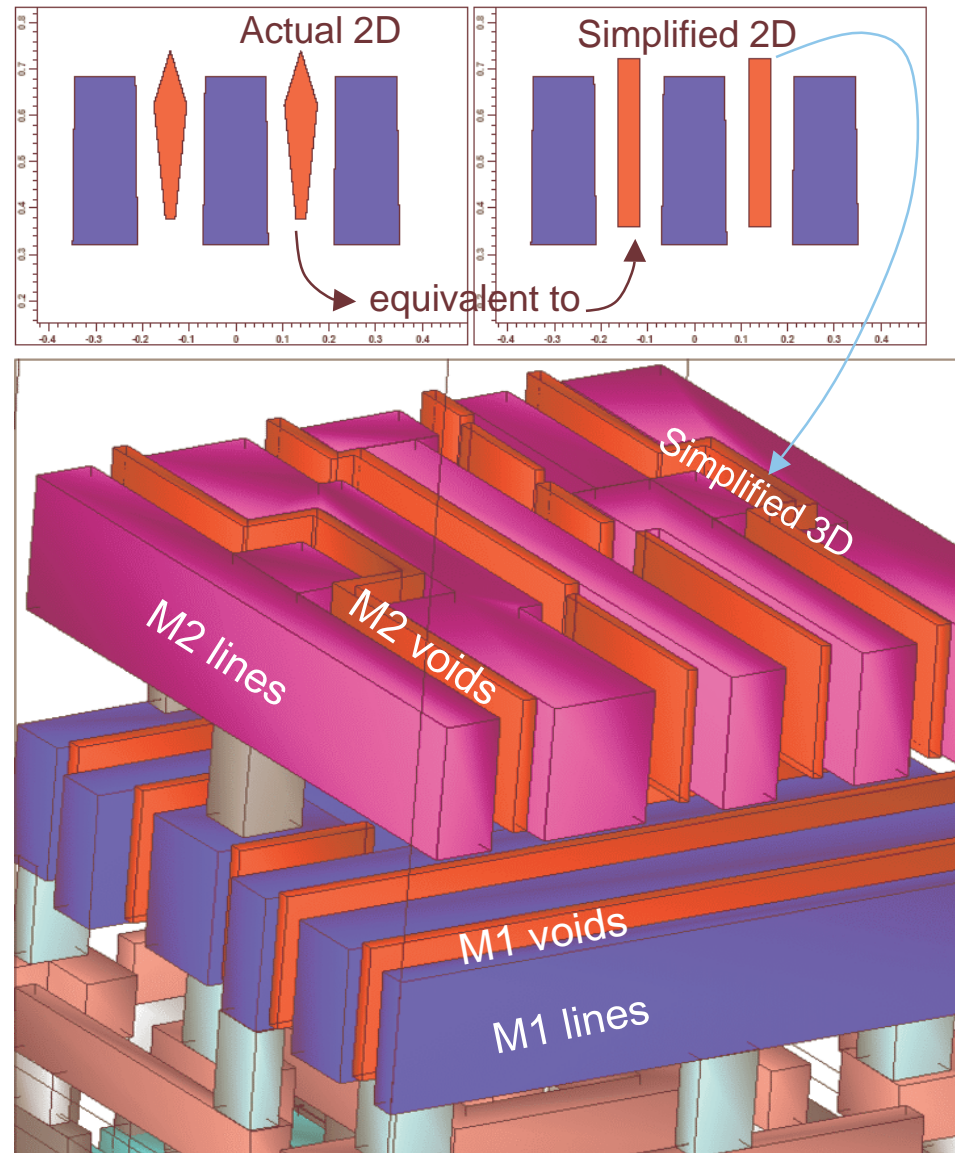


Capacitance Versus Space



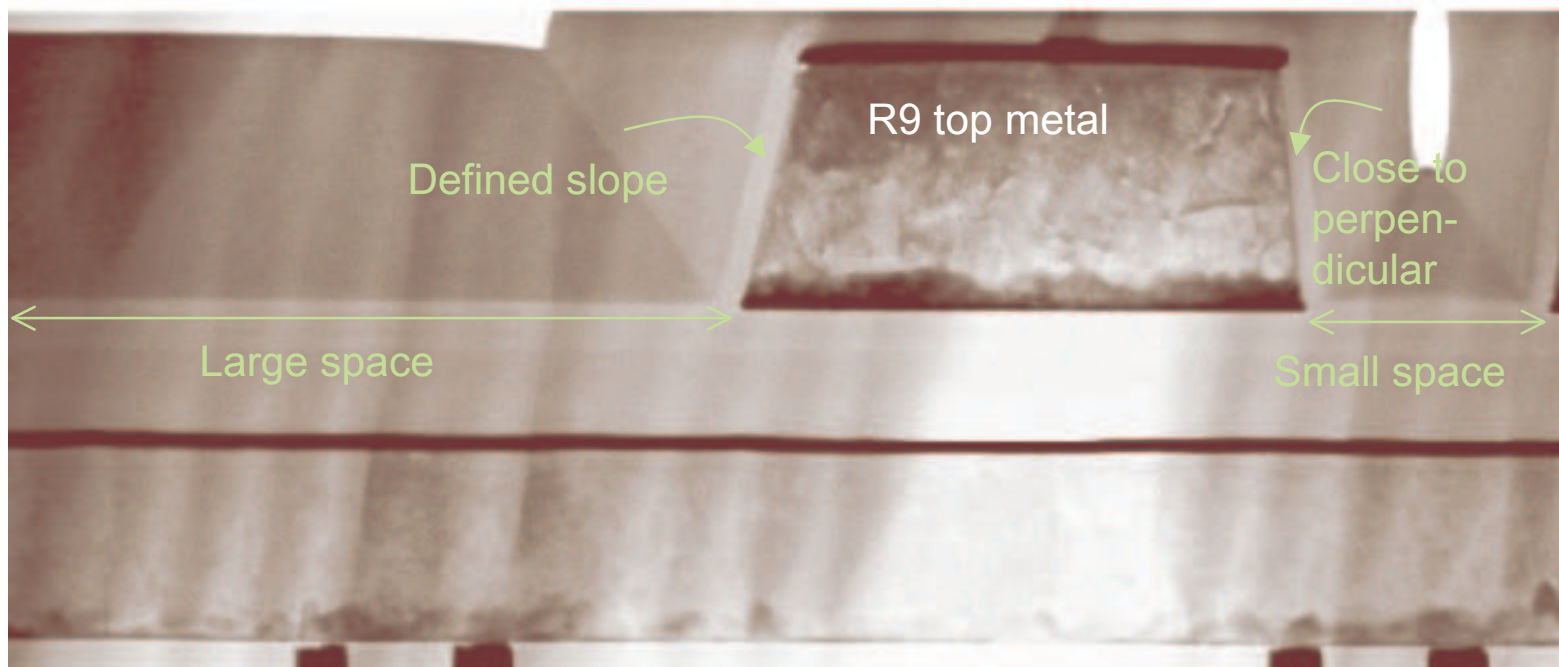
Simplified Airgap Models for 3D Simulations

- Because of 3D software limitations, 3D voids can be drawn only as rectangles
- A transformation is carried out to map 2D voids into 3D rectangular voids
- Figure on right shows sample 3D extraction with M1 and M2 airgaps
- Since cells are compact in space, airgaps exist in most metals



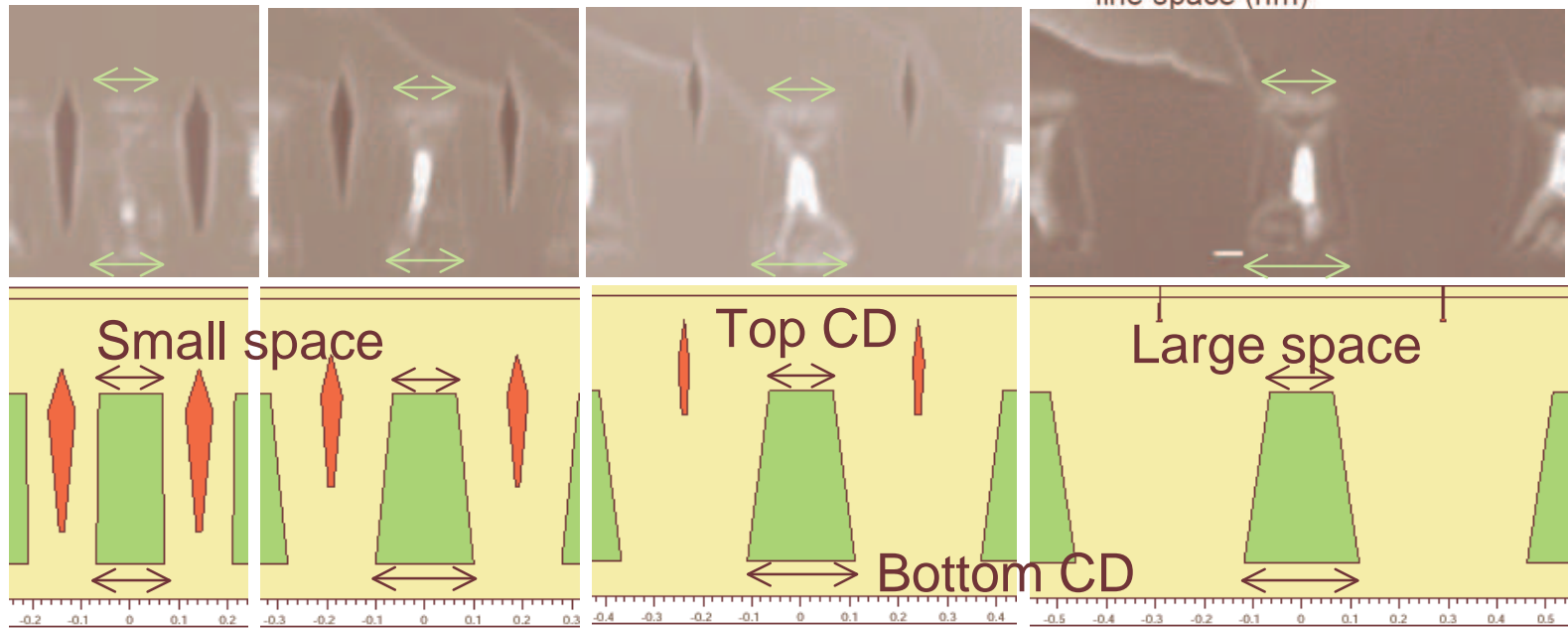
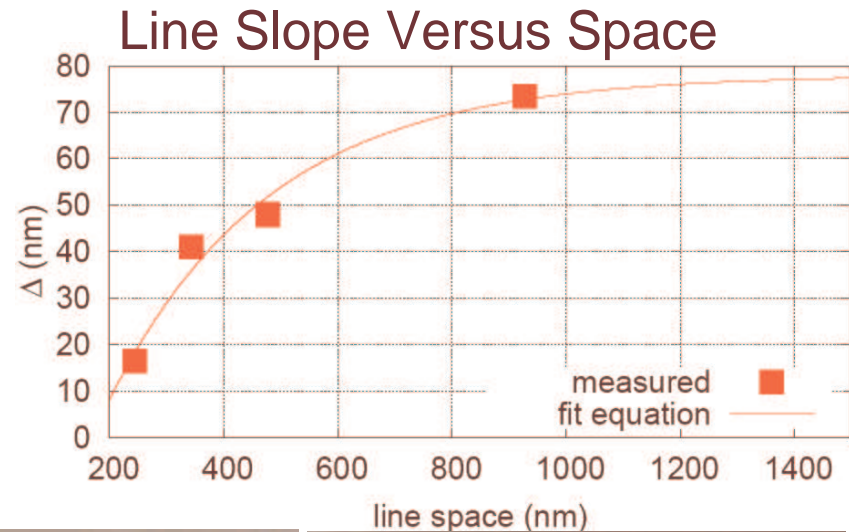
Line Slope Characterization

- **Aluminum** lines at small space come out close to perpendicular
- Lines at intermediate and large space have a **slope**
- At very large space line slope **saturates**



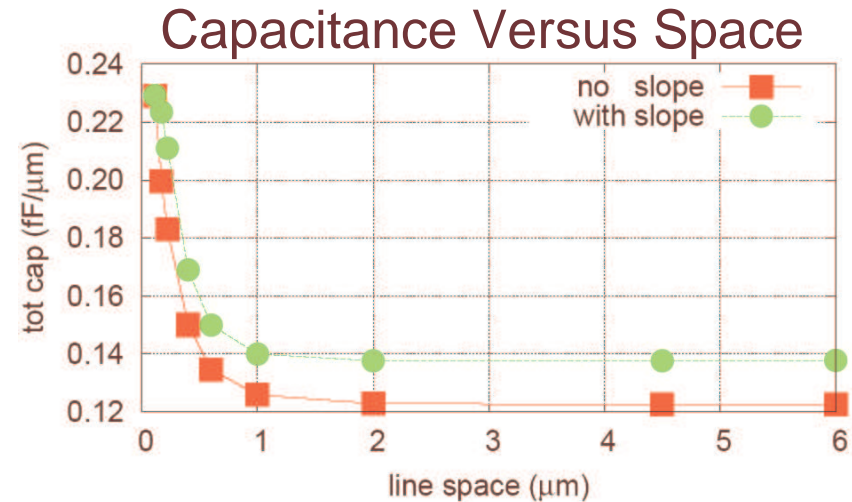
Line Slope Modeling

- Difference between bottom CD and top CD measured as a function of space (bottom CD = top CD + 2 Δ)
- Bottom CD fit into polynomial
- Polynomial fed in field solver
- Sample R9T M1 below



Impact of Line Slope on Capacitance

- At small space line is perpendicular, hence no impact on capacitance
- Line slope kicks in at large space
- Line slope **increases capacitance** (mainly bottom capacitance)



Conclusion

- Silicon-based method for **modeling capacitance impact of airgaps and line slope**, both as a function of space
- Principle relies on **measuring CDs and fitting into polynomial**
- Use **fit polynomial as input for capacitance simulation software**
- **Airgaps decrease capacitance**, especially at small space
- **Line slope increases capacitance**, especially at large space