A History of MOS Transistor Compact Modeling

Chih-Tang (Tom) Sah
University of Florida
Acknowledgement

• Xing Zhou
• Colin C. McAndrew
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• Mitiko Miura-Mattausch
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• Read stories in proceedings.
What is Compact Modeling?

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Comments on “A New Approach to the Theory and Modeling of IGFET’s”

J. R. BREWS

Abstract—The El-Mansy and Boothroyd MOSFET model is shown to be inconsistent. Therefore, MOSFET characteristics predicted by this model are not logical consequences of their assumed form for the minority carrier density \( Q_m \). Moreover, the derivation and heuristic arguments in favor of \( Q_m \) are faulty. These circumstances leave the physical origin of \( Q_m \) a mystery.

INTRODUCTION

The prospect of explaining MOSFET behavior at large gate voltages with a constant mobility model has been raised by El-Mansy and Boothroyd [1]. In particular, the observed slow drop in transconductance \( g_m \) at large gate voltages generally has been attributed to mobility degradation. El-Mansy and Boothroyd suggest inaccurate prediction of the gate voltage dependence of the minority carrier density \( Q_m \) as the root of the problem with the traditional models. With a correct \( Q_m \) they claim, \( g_m \) will drop without invoking mobility degradation.

The object of this comment is to cast severe doubt upon the El-Mansy and Boothroyd model. We point out that 1) their model is internally inconsistent, 2) their derivation of a new form for \( Q_m \) involves assumptions which are contradicted by experiment, and 3) their new form of \( Q_m \) departs from the usual form in a way which cannot be explained as a quantum-mechanical correction.

Internal Inconsistency

The El-Mansy and Boothroyd model employs a form for the total semiconductor charge \( Q_t \) which is not compatible with their form for the minority carrier charge \( Q_m \). Using their (11) and (15) we find that in their model

\[
Q_t = 2 \left( \frac{kT}{qL_m} \right) \epsilon_0 \left[ U_s - U_b + \exp \left( U_e - \frac{z}{2} - 2U_e \right) \right]^{1/2}
\]

(1)

Equation (1) is the Pao-Sah expression [2] for \( Q_t \) in the limit \( U_e \gg U_s + 1 \) [i.e. in depletion or inversion]. We know that (1) is derivable from the Pao-Sah expression for the minority carrier density, which we will label \( Q_{m,mc} \). Is \( Q_t \) also compatible with the El-Mansy and Boothroyd expression \( Q_m \)? In weak inversion a comparison is easily made. We expand (1) for small minority carrier densities (exponential small compared to \( U_s - U_b \)). The result agrees with \( Q_{mc} \), not \( Q_m \). Therefore, in weak inversion \( Q_m \)

Authors’ Reply to “Comments on ‘A New Approach to the Theory and Modeling of IGFET’s’”

Y. A. EL-MANSY AND A. R. BOOTHROYD

The points raised by Brews¹ on our approach [1] to the modeling of the IGFET appear to reflect a lack of sympathy with the objectives of the “device modeling engineer” working in the context of CAD, who is required to characterize the device accurately over a wide range of operating conditions, in a manner acceptable to the circuit designer and with the capability of efficient computer implementation of the model. In order to achieve these objectives, he commonly employs a combination of device physics, approximation techniques, and insight in regard to the route to his goal which is likely to be the most successful. In the interests of the best representation of first-order physical behavior of the device in the working context, he is prepared to sacrifice accuracy of representation of some he judges to be second-order effects. The first paragraph of our paper [1]

Manuscript received October 6, 1977; revised December 6, 1977.
Y. A. El-Mansy is with Bell-Northern Research, Ottawa, Canada.
A. R. Boothroyd is with the Department of Electronics, Carleton University, Ottawa, Canada.

where \( L_B \) is the extrinsic Debye length,

\[
L_B = \left[ \frac{kT \epsilon_0}{q^2 N_A} \right]^{1/2}
\]

(2)

The authors with Bell Laboratories, Murray Hill, NJ 07974.
What is Compact Modeling?

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What are computed to compare with and extract parameters from experimental data?

- DCIV: $I_D$-$V_{DS}$; $I_D$-$V_{GS}$
- YV: $g_d$, $g_m$, $C_{gd}$, $C_{gb}$, $C_{gs}$, others vs $V_{DS}$, $V_{GS}$
- AC small-signal harmonic distortions
- Switching transients, rise-fall-delay times
- See Narain Arora’s 1993 book for a superb review and tutorial on compact modeling.
Theoretical DCIV of nMOST

6604039
Review of Analysis Methods for the theoretical DCIV

- Geometry shows MOS Transistor is 3-D or at least 2-D.
MOS Transistor is 2-D and 3-D.
Macroscopic Large Microscopic Small

Large Geometry
– Many atoms, electrons, statistical average
– Differential Equation and Difference Equation

Small Geometry
– Few atoms, electrons, time average
– Ballistic solution and trajectory average
Macroscopic Large

Large Geometry

Differential and Difference Equations

• Differential Equation
  – Shockley Semiconductor Differential Equations
  – Analytical, fast, accurate
    • Faster by approximating formulas = compact modeling

• Difference Equation
  – Shockley Semicond. Finite Difference Equation
  – Numerical, slow, not accurate
Analytical Solution of Differential Equations

- 2-D(x,y) to two one-D: 1-D(x), 1-D(y)
- x-y coupling dropped in 0th order - long-channel
- 1-D(x) gives Voltage Equation via Poisson Eq
  - Electric Potential \( U \triangleq qV/kT \)
  - Electrochemical or Quasi-Fermi Potential
    or just plain “Voltage” \( U_N(x,y) \)
  - Implicit Voltage equation: \( V_{\text{Gate}} = f(U, U_N) \)
- 1-D(y) gives Current Equation (Drift+Diffusion)
1-D Analytical y-Solution

- nMOST on p-Body
- Electron Current between n+D and n+S

\[ \mathbf{J} = \mathbf{J}_N + \mathbf{J}_P \approx \mathbf{J}_N(x,y) \approx \mathbf{J}_{NY}(x,y) = \text{channel current} \]

\[ \mathbf{J}_{NY} = q \mu_n \mathbf{N} \mathbf{E}_Y + q \mathbf{D}_n \partial \mathbf{N} / \partial y = \uparrow 2\text{-term} \]

\[ = - q \mu_n \partial \mathbf{V}_N / \partial y \quad \text{(use } \mathbf{E}_Y = - \partial \mathbf{V} / \partial y) \quad \uparrow 1\text{-term} \]

\[ \mathbf{J}_{NX} = q \mu_n \mathbf{N} \mathbf{E}_X + q \mathbf{D}_n \partial \mathbf{N} / \partial x \quad \text{(use } \mathbf{E}_X = - \partial \mathbf{V} / \partial x) \]

\[ = - q \mu_n \partial \mathbf{V}_N / \partial x = 0 \quad \therefore \mathbf{V}_N(x,y) = \mathbf{V}_N(y) \quad \uparrow \]

1. Boltzmann Representation (exponential transform)

\[ \mathbf{N} = n_i \exp[q(\mathbf{V} - \mathbf{V}_N)/kT] \]

2. Einstein Relation \( \mathbf{D}_n / \mu_n = kT/q \)

\[ \mathbf{J}_P = - q \mu_n \nabla \mathbf{V}_P = 0 \quad \therefore \mathbf{V}_P(x,y) = \mathbf{V}_P = \text{constant} \quad \uparrow \]
1-D Analytical x-Solution

• **Poisson Equation** (nMOST=p-Base)
  \[ \varepsilon \nabla \cdot \mathbf{E} = \rho = q(P - N - P_{AA} + N_{DD}) \]
  \[ = \varepsilon \left( \frac{\partial E_X}{\partial x} + \frac{\partial E_Y}{\partial y} \right) \approx \varepsilon \left( \frac{\partial E_X}{\partial x} \right) \]
  \[ = - \frac{\partial^2 V}{\partial x^2} \]

• **Integrate 3 ways**: dx, dxdx, dV(x,y=k)
  Use: \( V_P = V_F \), \( V_N(x,y) = V_N(y) \), \( V(0,y) = V_S(y) \), \( V(\infty,y) = 0 \)

• **Give Voltage Equation**
  \[ C_0 (V_{GB} - V_{FB} - V_S) = Q_{AA} F_A^2 \]
  (Let \( U = qV/kT \))
  \[ F_A^2 = (e^{-U_S} + U_S - 1)e^{+U_F} \]
  40-years of bulk-charge work
  \[ + (e^{+U_S} - U_S - 1)e^{-U_F + U_{PN}} \]
  40-years of \( Q_{inv} \) trouble
History of MOS Transistor Compact Model Analysis

- You might not know it, do you?
- Half of the theoretical analyses of MOS Compact Modeling (Voltage-equation) was formulated in
  - 1953-Brown-Shockley for n/p/n electron channel and
  - 1955-Garrett-Brattain for MOS FE to determine $Q_{SS}$. 
History of MOS DC Analyses
Experimental Motivation == $Q_{SS}$

- 1926-1933 Linenfeld FET patents
- 1947 Meyerhof (U.Penn) and others: Schottky Barrier little dependence on metal workfunction
- 1947 Bardeen (BTL) surface-state on thin oxide between metal and semiconductor (MOS) pins $U_S$ at $\sim E_V + E_G/3$ from high density of U-shape $Q_{SS}$
- 1948 Shockley+Pearson (BTL) Thin-film air-gap FE conductivity modulation failed due to high $Q_{SS}$
Characteristics of the Metal-Oxide-Semiconductor Transistors

C. T. SAH, MEMBER, IEEE

March 7, 1933

J. E. LILIENTHAL

DECEASED ELECTRIC CURRENT

Filed March 28, 1933

3 Sheets-Sheet 1

Fig. 1—The field effect transistor structures. (a) The metal-oxide-semiconductor transistor proposed by Lilienthal. (b) The metal-oxide semiconductor thin film transistor proposed by Heil.

Fig. 2—The geometry of N-channel MOS transistors. (a) Top view. (b) Cross-sectional view. (c) The expanded channel region of the circular geometry. (d) The linear structure.
Contact Potential Difference in Silicon Crystal Rectifiers

WALTER E. MEYERHOF

University of Pennsylvania, Philadelphia, Pennsylvania

(Received, February 16, 1947)

The rectifying portion of a crystal rectifier is the contact between a small point made of metal such as tungsten, and a semiconductor such as silicon or germanium containing suitable impurities. The potential energy of a conduction electron near the contact determines the rectifying action of the crystal rectifier. The most important feature of this potential energy, as far as the present paper is concerned, is the height of the potential barrier, which the electrons have to overcome when they pass from the metal to the semiconductor or vice versa. The height of the barrier is called here contact potential difference (c.p.d.), because theoretically it is equal to the difference in the work functions of the substances in contact. The c.p.d. has been measured using both n- and p-type silicon and different metallic contacts. (The c.p.d. can be obtained from the variation of the contact resistance with temperature.) The work function differences (w.f.d.) between the same substances were obtained independently by a parallel plate condenser method (Kelvin method). The results showed no correlation between the c.p.d. and the w.f.d. The c.p.d. is practically independent of the kind of metal used and also of the structure of the silicon surface. These results are in contradiction to the present theoretical model of the silicon crystal rectifier.


** This work was done under Contracts OEmSr-388 and NObs-34144 between the Trustees of the University of Pennsylvania and the Office of Scientific Research and Development and the Navy Department, Bureau of Ships, respectively, which assume no responsibility for the accuracy of the statements contained herein.

*** Now at the University of Illinois.

ACKNOWLEDGMENTS

The author wishes to thank Dr. W. E. Stephens for his constant advice and guidance in this research and Dr. L. I. Schiff for his many valuable suggestions.
Contact Potential Difference in Silicon Crystal Rectifiers

WALTER E. MEYERHOF
University of Pennsylvania, Philadelphia, Pennsylvania
(Received, February 16, 1947)

Fig. 1. Energy level diagrams for metal and semiconductor in equilibrium.

Fig. 4a. Apparatus used to measure c.p.d.

Fig. 4b. Crystal rectifier assembly.
**Contact Potential Difference in Silicon Crystal Rectifiers**

*WALTER E. MEYERHOF***

*University of Pennsylvania, Philadelphia, Pennsylvania*

(Received, February 16, 1947)

### Table I. Contact potential differences of various metals with respect to p-type silicon.

<table>
<thead>
<tr>
<th>Metal</th>
<th>Observed ( \theta \varphi ) (volts)</th>
<th>Corrected ( \varphi ) (volts)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Al</td>
<td>0.00, 0.01, 0.09</td>
<td>0.00, 0.07, 0.21</td>
</tr>
<tr>
<td>Au</td>
<td>0.21, 0.23, 0.28</td>
<td>0.36, 0.39, 0.44</td>
</tr>
<tr>
<td>Cu</td>
<td>0.15, 0.22, 0.36</td>
<td>0.29, 0.38, 0.53</td>
</tr>
<tr>
<td>Fe</td>
<td>0.14, 0.17, 0.22</td>
<td>0.28, 0.32, 0.38</td>
</tr>
<tr>
<td>Mo</td>
<td>0.17, 0.26, 0.39</td>
<td>0.32, 0.42, 0.57</td>
</tr>
<tr>
<td>Ni</td>
<td>0.16, 0.31, 0.33</td>
<td>0.30, 0.48, 0.50</td>
</tr>
<tr>
<td>Ni-alloy(^{10})</td>
<td>0.21, 0.20, 0.41</td>
<td>0.36, 0.42, 0.59</td>
</tr>
<tr>
<td>Pt</td>
<td>0.10, 0.17, 0.20</td>
<td>0.22, 0.32, 0.35</td>
</tr>
<tr>
<td>Pt-alloy(^{11})</td>
<td>0.17, 0.19, 0.37</td>
<td>0.32, 0.34, 0.55</td>
</tr>
<tr>
<td>Ta</td>
<td>0.10, 0.18, 0.26</td>
<td>0.22, 0.33, 0.42</td>
</tr>
<tr>
<td>W</td>
<td>0.15, 0.23, 0.32</td>
<td>0.29, 0.39, 0.49</td>
</tr>
</tbody>
</table>
Localized states (Tamm levels), having energies distributed in the “forbidden” range between the filled band and the conduction band, may exist at the surface of a semiconductor. A condition of no net charge on the surface atoms may correspond to a partial filling of these states. If the density of surface levels is sufficiently high, there will be an appreciable double layer at the free surface of a semiconductor formed from a net charge from electrons in surface states and a space charge of opposite sign, similar to that at a rectifying junction, extending into the semiconductor. This double layer tends to make the work function independent of the height of the Fermi level in the interior (which in turn depends on impurity content). If contact is made with a metal, the difference in work function between metal and semiconductor is compensated by surface states charge, rather than by a space charge as is ordinarily assumed, so that the space charge layer is independent of the metal. Rectification characteristics are then independent of the metal. These ideas are used to explain results of Meyerhof and others on the relation between contact potential differences and rectification.

Fig. 1. Energy level diagram for metal-semiconductor contact illustrating notation used in text. The Fermi levels are $\mu_1$ and $\mu_2$ and the work functions $\phi_1$ and $\phi_2$. The lowest state of the conduction band is denoted by $C$ and the highest level of the filled band by $F$. If the surface states are filled to an energy $E_s$ below the conduction band there is no net charge on the surface atoms.

Fig. 4. Schematic diagram showing how the potential rise $\phi_s$ is determined from the density of surface levels and the contact potential difference (see text).
MOS Theory for Surface Field-Effect Experiments

• 1953 Walter L. Brown (Bell Labs via Harvard)
  – Under Shockley. MIT Physicist, easy to understand
  – N-Surface channel on n/p/n BJT.
  – Bipolar Junction Transistor physics.

• 1955 C.G.B. Garrett (Bell Labs via UK)
  – Under Brattain. UK Chemists, tough notation.
  – Surface FE conductivity modulation for $Q_{SS}$.
  – Thorough analyses of many cases.
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n-Type Surface Conductivity on p-Type Germanium

W. L. Brown
Bell Telephone Laboratories, Murray Hill, New Jersey
(Received March 17, 1953)

A positive charge on the surface of a p-type germanium crystal induces a net negative space charge within the crystal adjacent to the surface. This space charge is composed of ionized acceptor atoms and also of electrons under certain conditions. When electrons occur they provide a layer of n-type conductivity immediately under the p-type germanium surface. Such a layer has been found on the p-type region of some n-p-n transistors. In the n-p-n structure the layer of electrons appears as an extra conducting path—"a channel"—across the p-type material between the two n-type ends. The conductance of a channel and the capacity between the channel and the p-type material have been measured and compared with the theoretical predictions based on a simple model.

The author is particularly indebted to W. Shockley for his part in this work. His suggestions during its progress and his assistance with the manuscript have contributed materially to the appearance of this paper. I am also much indebted to M. Sparks and K. D. Smith who provided most of the transistors used in this study.
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**n-Type Surface Conductivity on p-Type Ge**
n-Type Surface Conductivity on p-Type Germanium

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W. L. Brown

Fig. 2. (a) Experimental floating potential curve. (b) Connections for measurement of channel capacity. (c) Circuit for channel conductance measurement.
n-Type Surface Conductivity on p-Type Germanium

W. L. Brown
Bell Telephone Laboratories, Murray Hill, New Jersey
(Received March 17, 1953)

\[ \rho = n_s \exp\left(\frac{q\psi}{kT}\right), \quad n = n_i \exp\left(\frac{q\phi_s}{kT}\right). \]

In a nonequilibrium case it will be convenient to define two quasi-Fermi potentials \( \psi_a \) and \( \psi_p \) such that
\[ \rho = n_s \exp\left(\frac{q\psi_a}{kT}\right), \quad n = n_i \exp\left(\frac{q\psi_p}{kT}\right). \]

when \( \psi = \psi_a \) the hole and electron concentrations are equal to the intrinsic concentration \( n_i \). For the equilibrium case:

\[ \frac{d\psi}{dz} = -\frac{4\pi \rho}{z}, \quad \frac{d\phi_p}{dz} = \frac{4\pi q N_i}{x} \]

and using (5):
\[ 4\pi q N_i = \left(\lambda (V_a - 2\psi_p)\right)^4 \left(\lambda (V_a - 2\psi_p)\right)^4. \]

In the equilibrium case, \( \rho(\psi) \) has the form
\[ \rho = 2\rho_i \sinh(\frac{q\psi}{kT}) + \rho_n \]

where \( \rho_i = 2q\rho_i \) and \( \rho_n = -qN_i \). \( N_i \) is the density of acceptors. Figure 6(a) shows \( \rho(\psi) \). The dashed line is given in (3) by:
\[ \rho = \rho_i \sinh(\frac{q\psi}{kT}) = \frac{q\psi}{kT} \quad \text{for} \quad \psi > \psi_p, \]
\[ \rho = -\rho_n \sinh(\frac{q\psi}{kT}) = -\frac{q\psi}{kT} \quad \text{for} \quad \psi < \psi_p. \]

From (9)
\[ g = \frac{\mu (w/L)}{2\pi} \left(\lambda (V_a - 2\psi_p)\right)^4 - \left(\lambda (V_a - 2\psi_p)\right)^4. \]

Where \( w \) is the width of the channel, so that
\[ g = \frac{qN_i w}{L}. \]

Fig. 6. Theoretical charge densities.
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  - Surface FE conductivity modulation for $Q_{SS}$.
  - Thorough analyses of many cases.
Physical Theory of Semiconductor Surfaces

C. G. B. Garrett and W. H. Brattain
Bell Telephone Laboratories, Inc., Murray Hill, New Jersey
(Received December 20, 1954)

The properties associated with the space-charge region and with surface states at a semiconductor surface are discussed. A theory of the space-charge region that takes into account charge-densities arising from immobile impurities and from both signs of mobile carrier is presented. The properties of the space-charge are discussed in terms of the surface potential and of the electrochemical potentials of holes and electrons, and related to the transport of added carriers in a homogeneous semiconductor. The change in surface conductivity arising from nonvanishing surface excesses of holes and electrons is treated. The space-charge systems at a free surface and at a p-n junction are compared, and the range of validity of the Mott-Schottky space-charge theory evaluated. The arrangement of surface states is discussed with reference to the Brattain-Bardeen model. Theories for the surface photoeffect and field-effect experiments are given, with and without surface states: it is concluded that the existence of surface states is without gross effect on the former, while relevant quantitative evidence from the latter is not yet available. The question of the relation between surface potential and contact potential is discussed. The properties of “channels” are discussed in terms of the theory. The paper concludes with a short section on long-time effects.
A History of MOS Transistor Modeling by Chih-Tang Sah
Stable Oxide

• 1959 Atalla, Tannenbaum Scheibner (BTL)
  – Thermally Grown Oxide on p/n and p/n/p/n.
  – Low reverse leakage at 10V for BV=40V
    • Body 53nA/cm²
    • Perimeter surface 3.5nA/cm²
    • Low corner-frequency 1/f noise
  – Same issue of Claude Shannon (BTL)
    • Probability of Error for Optimal Codes in a Gaussian Channel
Stabilization of Silicon Surfaces by Thermally Grown Oxides*

By M. M. ATALLA, E. TANNENBAUM and E. J. SCHEIBNER

(Manuscript received January 7, 1959)

A study has been carried out of the stability of silicon surfaces when they are provided with a chemically bound solid-solid interface. Stable surfaces have been obtained with the system silicon-silicon dioxide when the oxide is thermally grown. This latter system has been studied in some detail. In this paper the following phases of our investigation are presented: (i) some aspects of the thermal oxidation process and properties of the oxide; (ii) the electronic properties of the resulting silicon-silicon dioxide interface; (iii) the application of the process to devices and resulting device characteristics.
Stabilization of Silicon Surfaces by Thermally Grown Oxides

By M. M. ATALLA, E. TANNENBAUM and E. J. SCHEIBNER

Fig. 21 — Typical characteristics of oxidized p⁺-n graded junction silicon diodes.

At 10V
1(Body) = 53 nA/cm²
1(Surf) = 3.5 nA/cm²
Stabilization of Silicon Surfaces by Thermally Grown Oxides*

By M. M. Atalla, E. Tannenbaum and E. J. Scheibner

(Manuscript received January 7, 1959)
Probability of Error for Optimal Codes in a Gaussian Channel

By CLAUDE E. SHANNON

(Manuscript received October 17, 1958)

A study is made of coding and decoding systems for a continuous channel with an additive gaussian noise and subject to an average power limitation at the transmitter. Upper and lower bounds are found for the error probability in decoding with optimal codes and decoding systems. These bounds are close together for signaling rates near channel capacity and also for signaling rates near zero, but diverge between. Curves exhibiting these bounds are given.
MOSCV Experiments - Theory

- 1959 Atalla Stable Thermal Oxide
- 1962 Terman MOSC $N_{IT}$, $dN_{IT}/dE_{IT}$
- 1962 Lindner Varactor, $C_{LF}$, $C_{HF}$
- 1964 Grove, Deal, Snow, Sah $C_{HF}$
Silicon MOS CV

• 1962 Lewis Terman (Stanford PhD under John Moll)
  – MOS C-V-f extraction of $Q_{SS}$, $N_{IT}$ and $dN_{IT}/dE_{IT}$
  – High-frequency C-V to give $Q_{SS}$, $N_{IT}$, $dN_{IT}/dE_{IT}$
  – U-shaped Density of States $dN_{IT}/dE_{IT}$

• 1961 Moll proposed MOS C-V Variactor at Wescon in San Francisco.
AN INVESTIGATION OF SURFACE STATES AT A SILICON/SILICON OXIDE INTERFACE EMPLOYING METAL–OXIDE–SILICON DIODES*†

L. M. TERMAN
I. B. M. Yorktown Heights, New York
(Received 16 October 1961; in revised form 8 February 1962)

Abstract—A new solid-state device, the M–O–S diode, of which an oxidized silicon surface is an integral part, is introduced, and a theory for its operation in the absence of surface states is obtained. The capacitance of this device may be considerably more voltage sensitive than that of a p–n junction. The existence of surface states with non-zero relaxation times is introduced into the theoretical model. It is shown that the states may increase the capacitance of the device, as well as affect the proportion of applied voltage which appears across the silicon. A small-signal equivalent circuit is derived which includes the effect of the surface states. It is also shown that a comparison of the theoretical capacitance vs. voltage curve without states and a measured high-frequency capacitance vs. voltage curve may be used to obtain the distribution of all states, regardless of their time constants.

Results are given of measurements and calculations on two M–O–S diodes having different surface treatments before oxidation. Both surfaces have a total density of about $3 \times 10^{12}$ states/cm². In both cases, the distribution of states is continuous and has its highest peak about 100 mV above $E_F(0)$, the position of the Fermi level at the silicon surface if there is no voltage drop across the silicon. The time constants of the states extend from $10^{-8}$ sec to longer than $10^{-2}$ sec. There is a tendency for states located at deeper energy levels to have longer time constants, but some of the states in the high density of states above $E_F(0)$ have long time constants. The distribution of time constants with energy level is somewhat different for the two surfaces.

A comparison is made between the distribution of states obtained here with the distribution reported by others working in the field. The results are similar in density and location of the peaks of the distribution reported here, but differ in that some other sources report a discrete distribution.
AN INVESTIGATION OF SURFACE STATES AT A SILICON/SILICON OXIDE INTERFACE EMPLOYING METAL–OXIDE–SILICON DIODES*†

L. M. Terman
I. B. M. Yorktown Heights, New York
(Received 16 October 1961; in revised form 8 February 1962)

Fig. 7(a). Circuit to plot \( Q \) vs. \( V \) for M–O–S diode on oscilloscope.

Fig. 7(b). Typical plot of \( Q \) vs. \( V \) for M–O–S diode on oscilloscope.
Interface State Capacitance $C_{IT}$
U-Shaped Interface States
Semiconductor Surface Varactor

By R. LINDNER

(Manuscript received October 19, 1961)

The semiconductor varactor using surface space charge is analyzed and measurements made on several experimental units are described. The chief characteristics of this device are its capacity-voltage dependence and its negligible dc conduction.

The particular system used in this work is a thermally grown oxide on silicon. A theory developed from the surface charge relation is shown to agree with the experimental data over a wide range of silicon resistivity.

The theory for optimum operation for both dc and ac biasing is derived and used to compare the performance of this device with that of the p-n junction varactor. The result of this comparison shows that with careful design the semiconductor surface varactor will be able to compete favorably with the junction varactor for many possible applications, including those of ultra high frequency.
Semiconductor Surface Varactor

By R. LINDNER
(Manuscript received October 19, 1961)

Fig. 5 — Solid lines are experimental plots of the capacity measured over a range of bias voltage. The results of four units made from 15 ohm-cm n-type silicon are shown on the left and two units of 15 ohm-cm n-type silicon are...
Simple Physical Model for the Space-Charge Capacitance of Metal-Oxide-Semiconductor Structures


Fairchild Semiconductor Research & Development Laboratory, Division of Fairchild Camera & Instrument Corporation, Palo Alto, California

(Received 9 March 1964)

A simple physical model is presented which gives the capacitance-voltage characteristics of a metal-oxide-semiconductor structure at high measurement frequencies in excellent agreement with the experimental observations. The model is based on the concept that at high frequencies the minority carriers within the inversion region act as 'fixed charges' and so do not contribute to the ac variation of charge within the semiconductor. However, their presence determines the size of the depletion region under the given dc bias and hence the space-charge capacitance.

Fig. 1. (a) The metal-oxide-semiconductor structure, (b) energy band at large positive bias, (c) idealized charge distribution within the semiconductor for large positive bias, (d) electric field for charge distribution given in (c), (e) potential distribution for charge distribution given in (c).

Fig. 2. The number of electrons in the inversion region and the width of the depletion region as a function of the total charge induced in the semiconductor.

Fig. 3. Comparison between the theoretical high- and low-frequency capacitance-voltage characteristics and the experimental measurements. (The voltage scale for the experimental curves was shifted by 3 V to line them up with the theoretical calculations. This shift represents the effect of surface states on the characteristics.)
Modern Silicon MOS Transistor

- 1961 Kahng (BTL)
  - Forward and Reverse bias drain/base junction
  - Voltage-dependent bulk-charge theory
  - Constant bulk-charge used in data analyses
- 1963 Wanlass, Sah, Moore CMOS circuit
- 1964 Sah constant bulk-charge theory
- 1964 Ihantola and Moll bulk-charge theory
- 1965 Sah 3-layer bulk-charge theory
- 1966 Pao-Sah Drift-Diffusion double-integral
Modern Silicon MOS Transistor

- 1972 Barron (Stanford March-1971)
  - Subthreshold Theory and Experiment.
- 1972 Stuart+Eccleston (Liverpool March 1972)
  - Experimental subthreshold data $I_D \sim \exp(qV_G/\alpha kT)$
- 1972-1978 Many on Subthreshold, slope, threshold-voltage
- 1978 Brews (BTL May 1977)
  - Charge sheet theory subthreshold, inversion, saturation.
- 1978 Baccarani, Ruidan, Spadini (Bologna Oct.1977)
- 1979 Van de Wiele (Louvian April 1979)
  - Systematic successive approximation theories.
    - Derived threshold voltage and surface potential formulas for inversion.
    - Subthreshold required separate formula.
- 1978-1980 Many on 2-D effects and subthreshold
  - 1978 Taylor, 1979 Toyabe, 1979 Troutman DIBL, 1980 Klaassen-De Groot,
    1981 Nguyen-Plummer DIBL, 1983 Guebels-Van de Wiele,
    1983 Pierret-Shields
Dawon Kahng

• 1960-May Kahng patent granted 1963
  – pMOST reverse and forward drain/base junction
• 1960-August Atalla patent granted 1962
  – n/i/n space-charge-limited or intrinsic MOST
• 1960-June Kahng-Atalla SSDRC-Pittsburg
  – Kahng presented enhancement MOSTs in:
• 1961-BTL Memorandum for File MH-2821-DK-pg
  – Used 1953-Brown voltage equation analysis
  – But attributed to 1960-1961-Atalla.
1961 Dawon Kahng BTL Memo

INTRODUCTION
The effect of an electric field normal to a semiconductor surface on the surface properties has been the subject of intensive studies for many years.\(^{(1)}\) In particular,

ACKNOWLEDGMENTS
The author wishes to express his appreciation to M. M. Atalla for his contribution to some of the theoretical analysis, Miss J. D. Goeltz for her help in connection with the digital computation, E. E. LaBate and E. I. Povilonis for device fabrication, and H. K. Gummel and R. Lindner for helpful discussions on some aspects of the device characterization.
Silicon-Silicon Dioxide Surface Device
MEMORANDUM FOR FILE
MH-2821-DK-pg

January 16, 1961
D. Kahng

FIG. 1  P-INVERSION LAYER
AT THE SURFACE OF A
N-TYPE MATERIAL,
VOLTAGE V_d APPLIED
ACROSS THE SURFACE.

FIG. 2  METAL FILM
OXIDE
DIFFUSED LAYERS
(P-TYPE)
N-TYPE
Silicon-Silicon Dioxide Surface Device –
MEMORANDUM FOR FILE
MH-2821-DK-pg

January 16, 1961
D. Kahng

FIG. 3

FIG. 7
DESIGN THEORY OF A SURFACE FIELD-EFFECT TRANSISTOR*

H. K. J. IHNANTOLA
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and

J. L. MOLL
Stanford Electronics Laboratories, Stanford University, Stanford, California

(Received 23 September 1963; in revised form 16 December 1963)

Abstract—The design theory of insulated gate, surface field-effect transistors is presented. It is shown that for similar dimensions the surface field-effect transistor has frequency response comparable to other field-effect transistors. It is found to be quite simple to trade capacitance and transconductance in the surface field-effect transistor. The static imput resistance of the surface field-effect transistor is just the leakage of the insulator, so that this device may be used in electrometers and similar equipment. In addition, the construction on the surface of a semiconductor crystal offers interesting possibilities as an element of an integrated circuit.

Résumé—On présente la théorie de la construction des transistors à déclencheur isolé et à effet de champ de surface. On démontre que pour des dimensions similaires, le transistor à effet de champ de surface a une réponse de fréquence comparable aux autres transistors ayant des effets de champ. On découvre qu’il est très simple d’échanger la capacité et la transconductance dans ce transistor. La résistance statique d’entrée du transistor à effet de champ de surface n’est que la fuite de l’isolant telle que le dispositif pourrait être employé dans les électromètres et autres équipements similaires. Aussi la construction sur la surface d’un cristal semi-conducteur offre d’intéressantes possibilités en tant qu’élément d’un circuit intégré.

DESIGN THEORY OF A SURFACE FIELD-EFFECT TRANSISTOR

H. K. J. IHANTOLA and J. L. MOLL

Fig. 1. Principle of a surface field effect transistor. Gate voltage controls conductance between source and drain.

REFERENCES
DESIGN THEORY OF A SURFACE FIELD-EFFECT TRANSISTOR*

H. K. J. IHANTOLA and J. L. MOLL

![Graph showing the relationship between ID and VD.]

Fig. 3. Theoretical ID–VD characteristics. The current is saturated beyond the saturation point, the locus of which is indicated by dashed line.

3. MATHEMATICAL ANALYSIS OF THE SFET

\[ I_D = \frac{\mu_n \varepsilon_d B}{LW_d} \left( V_G - \frac{1}{2} V_D^2 - \frac{1}{8} K [(V_D + 2\phi_F)^{3/2} - (2\phi_F)^{3/2}] \right) \]

where \( K = W_d \sqrt{(2\varepsilon q N_A)/\varepsilon_d} \)

The slope near zero drain volts is:

\[ G_0 = \left( \frac{\partial I_D}{\partial V_D} \right) = \mu_n \varepsilon_d B \left( V_G - K(2\phi_F)^{1/2} \right)/W_dL. \]

Actually the conductance does not become zero at \( V_G = K(2\phi_F)^{1/2} \) (threshold)

\[ g_m = \mu_n \varepsilon_d B V_D/W_dL. \]

\[ V_{D0} = V_G + \frac{K^2}{2} - \sqrt{\left( V_G K^2 + \frac{K^4}{4} + 2K^2\phi_F \right)} \approx V_G - K \sqrt{(V_G)}. \]
CMOS Inverter Circuit

• 1963 Wanlass and Sah
  – ISSCC Philadelphia

• 1963 Moore Sah Wanlass
  – European Low Power Circuit Conference
Complementary N and P type field effect Metal-Oxide-Semiconductor-Field-Effect-Transistor (N莫斯) have been fabricated from silicon by a planar diffusion process. These devices have gate input resistance of about 10^12 ohms and input capacitance of 10 picofarads. Fig. 1 shows the cross section of both types of NMos which will be referred to as N and P elements. If an N element is biased with a positive gate-source voltage as shown in Fig. 2a, and if its gate is tied to its source, then drain-source current, I_{DS}, will be of the order of that flowing in a reverse biased silicon diode. But, I_{DS} can be increased considerably by using the gate-source voltage V_{GS} to 10 volts by a change of 20 volts in V_{DS}. The P element is described the same way as the N element except that all voltages need to be reversed. Thus, if a P element is connected as in Fig. 2b, I_{DS} can become very large if the gate is biased negatively with respect to its source. Fig. 3 shows characteristic I_{DS} vs. V_{DS} curves for both types of NMos when connected as in Fig. 2.

Consider the inverter circuit of Fig. 4 as an example of low power logic that uses only N and P elements without the need for resistors or any other components. Here the N element, acting as an active load for the P element, is turned on when the P element is off, and off when the P element is on. This combination will only dissipate appreciable power during switching. The leakage current is so low for a NMos in the off state that 10^3 circuits like that of Fig. 4 would use less than one watt of steady power.

Even though the steady power of the inverter of Fig. 4 is extremely low, it can still switch very fast. In an effort to measure the signal propagation delay of the inverter the three stage ring oscillation of Fig. 5 was set up. Fig. 6 is a plot of the output of one of the stages and it is seen that the propagation delay is less than 100 nsec. Part of the observed delay is due to oscilloscope input capacitance across the input.

Other useful logic circuits using only complementary N and P elements can be readily designed. For example, Fig. 7 shows a NCM circuit and Fig. 8 a set-reset flip-flop. In these circuits appreciable energy is dissipated only at a rate proportional to the information processing rate.

The output of a logic circuit composed of complementary NMos can fan out to a large number of other inputs by direct coupling; the only consideration is limiting the number being that of switching speed. It should be possible to drive approximately 50 inputs from one output and have less than 10 nsec signal propagation delay.

Since NMos are switched in the voltage mode and no resistor-coupled active edge in the 8-6 switching consideration, high temperature differentials between different parts of N and P element circuitry can be tolerated well. This means that a volume of N and P elements that are dissipating power can be cooled efficiently using a small amount of heat exchange area. Thus, because both standby power density will be extremely low and switching power density can be high, it should be possible to construct NCM logic circuits with a very high packing density.
INSULATED-GATE FIELD EFFECT DEVICES FOR MICRO POWER LOGIC CIRCUITRY

G. E. Moore, C. T. Sah and F. M. Wanlass

Silicon field effect devices with gate electrodes insulated from the semiconductor by a silicon dioxide layer can be made so that with no applied gate voltage the source-to-drain characteristics are those of a planar silicon diode. By the application of a proper polarity gate signal the source-to-drain current can be varied from \(10^{-10}\) amps to \(10^{-6}\) ma. The gate electrode is a capacitive input having a d.c. impedance of \(10^{15}\) ohms.

Recent improvements in manufacturing technology allow such structures to be made in both polarities — where the underlying silicon is \(n\)-type as well as \(p\)-type. The existence of such complementary devices permits circuit performance not previously available.

An inverter circuit can be made by connecting the source electrodes of two complementary structures together, with the drain of the device employing \(p\)-type carriers connected to a negative power supply and the drain of the \(n\)-type device to a positive supply. The gates of the devices are connected in parallel for the input and the common source connection is the output. Logic configurations made from such inverter stages dissipate the order of \(10^{-9}\) watts per inverter except during switching, when power to charge the circuit capacitances is required. Switching propagation delays of 10 ns appear practical.

This paper will describe the device's structure and characteristics, its use in low stand-by power circuitry, and how integrated functions employing insulated-gate field effect devices might be made.
Dr. Gordon Moore
Director, Research and Development
Fairchild Semiconductor
4001 Junipero Serra Boulevard
Palo Alto, California

Dear Gordon:

I noticed that you men, F. M. Vanlase and C. T. Sah, will give a paper ("Haworth Logic") at the 1963 ISSCC in Philadelphia, Pa. You know my specific interest in this field, and I am wondering if this paper could not be presented at the June 1963 European Micropower Symposium. The program for that Symposium already has been completed but there is always room for a good paper.

As I have mentioned to you previously, there is a good probability that the overseas transportation cost of the speakers may be absorbed by the sponsor of the symposium.

I am looking forward to hearing from you soon.

Sincerely,

Edward Klosnjian

PKirk

P. S. 1. Chapter 8 ("Functional Devices") is already in. It is a brief but extremely well written piece, dealing chiefly with the broad philosophy of the concept, illustrated with some concrete examples.

2. I am still waiting for a decent photograph for T. I.'s package!

Ed

Dr. Gordon Moore
Fairchild Semiconductor
4001 Junipero Serra Blvd.
Palo Alto, California

Dear Gordon:

I was glad to hear that you endorse the presentation of the paper of Vanlase and Shah at the Micropower Symposium. I believe also that it would be a worthwhile contribution to the program. I shall see what can be done to include this paper in the program. For your information, I am enclosing a copy of my letter to the participants of the symposium. Please note that presentations are of university type lectures, with approximately one hour duration (or more). Subsequently, the lectures should be a very comprehensive treatment of the subject in which the idea of microcircuit should stand up very prominently. We have excellent speakers already lined up for the Lecture Series (one of them, incidentally, is from Stanford University).

As you noticed from the attached, we do not have yet a facility offer from Italy. This is due to the fact that our men in Torino, Dr. Giovanni Villa of FMI, Torino, is rather far from the semiconductor world and therefore he probably has difficulty to contact right people in this field (Olivetti, Teletrora or S.C.S.). Could someone from your company's subsidiary in Torino contact Dr. Villa in this connection?

The dates scheduled for our presentation in Torino are:

June 28 and 29 (or June 29 and July 1)

If you decide to present the paper yourself, then we would already have two authors of our book on the program. I would love if you could make it.

Sincerely,

Edward Klosnjian

P. S. The TI photo and the rest of the material have just arrived. Thanks.
Fixed Bulk Charge
40+Years of Approximations

Abstract—The theory of the characteristics of the MOS transistors is developed based on a model in which both the bulk charge due to the ionized impurity in the semiconductor substrate and the difference between the electrostatic potential and the voltage drop in the channel are included. A detailed comparison of the theory is made with experimental data of gate capacitance, drain current voltage characteristics, and transconductance characteristics on both $N$-channel and $P$-channel silicon devices with thin (2000 A) and thick (6200 and 8400 A) oxides under the gate electrode. The correlation is good using the surface mobility as the adjustable parameter. Mobility reduction in the saturation transconductance characteristics is predicted in the theory and demonstrated in the experimental data. It arises entirely from the bulk charge, which modifies the device characteristics, and is not associated with some basic surface scattering phenomena, which further reduce the mobility. It is also demonstrated experimentally that to evaluate a physically meaningful surface mobility from the conductance of the channel, the interface surface state charge $Q_{SS}$ cannot be assumed constant in the devices used in this study.

I. Introduction

This model were made on silicon devices [4], which showed that the general shape of the experimental characteristics follows well the predicted characteristics of the constant bulk charge model. However, a considerable amount of fine structures observed experimentally could not be accounted for by the simple model. These discrepancies were attributed to the spatially dependent and applied voltage dependent bulk charge of the extrinsic substrate of the silicon device used.

In this paper, detailed quantitative comparison between an improved theory and experimental results are made. In the improved theory, not only the nonconstancy of the bulk charge is taken into account, but also a differentiation between the surface potential and the quasi-Fermi potential or voltage drop along the channel is made.

II. Analysis of the Bulk Charge Term

When a large positive gate voltage is applied to the device, which is shown in Fig. 1, a negatively charged layer is formed at the surface of the semiconductor. This layer consists of a deep layer of electrons...
The Effects of Fixed Bulk Charge on the Characteristics of Metal-Oxide-Semiconductor Transistors

C. T. SAH, MEMBER, IEEE, AND H. C. PAO

\[ Q_B = -\sqrt{2qN_AK_S\varepsilon_0 \left[(2\phi_F + V - 3kT/q)^{1/2}
+ 2(kT/q)(2\phi_F + V - kT/q)^{-1/2}
+ e^{-1}(kT/q)(2\phi_F + V + kT/q)^{-1/2}\right]}. \]

Here, the major contribution comes from the first term in (3), which is due to the uncompensated and ionized impurities in the depletion layer near the surface. Thus, neglecting the two small terms, which is implicitly made by Ihantola [1], the bulk charge may then be approximated by

\[ Q_B = -C_0 V_B \sqrt{1 + V/2\phi_F} \]

where the effective bulk charge voltage is

\[ V_B = \sqrt{4qN_AK_S\varepsilon_0\phi_F/C_0}. \]

An effective width of the transition region may be defined from the bulk charge using

\[ Q_B = -qN_A W. \]

This width is the equivalent width of the semiconductor surface layer, which would provide the desired amount of net charge if it is entirely depleted of carriers. Thus, from (4) and (5), this effective width may be written as

\[ W = \sqrt{2K_S\varepsilon_0(V + 2\phi_F - 3kT/q)/qN_A}. \]
The Effects of Fixed Bulk Charge on the Characteristics of Metal-Oxide-Semiconductor Transistors

C. T. SAH, MEMBER, IEEE, AND H. C. PAO

Fig. 10. The drain current-voltage characteristics with theory (dots) and experiments (solid lines).
The Effects of Fixed Bulk Charge on the Characteristics of Metal-Oxide-Semiconductor Transistors

C. T. Sah, Member, IEEE, and H. C. Pao

Fig. 2. The saturation drain to source voltage as a function of gate voltage. (a) $I_D = 2000\alpha$ and $N_A$ as parameter, (b) $N_A = 10^8/cm^2$ and $\alpha$ as parameter.

Fig. 3. The effect of bulk charge on the saturation drain current vs. gate voltage, $x_0 = 2000\alpha$ and $N_A$ as parameter. (a) $I_D$, (b) $\sqrt{I_D}$, and (c) the threshold gate voltage, all for silicon at 25°C. $K_s = 4$, $K_a = 12$. 

2005 Workshop on Compact Modeling
A History of MOS Transistor Modeling by Chih-Tang Sah

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EFFECTS OF DIFFUSION CURRENT ON CHARACTERISTICS OF METAL–OXIDE (INSULATOR)–SEMICONDUCTOR TRANSISTORS*

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Department of Electrical Engineering and Material Research Laboratory, University of Illinois Urbana, Illinois, U.S.A.

(Received 4 April 1966; in revised form 10 May 1966)

Abstract—A qualitative discussion of the device operation is first given using three-dimensional energy band diagrams to show the significance of the diffusion current. The theoretical static I–V characteristics are then computed including both the diffusion and the drift currents, based on the one-dimensional and gradual channel model. Drain current saturation phenomena are evident in these exact solutions which are in good agreement with the calculations based on the bulk charge approximation and with the experimental data for the entire non-saturating and saturated ranges. The relative importance of the two current components along the length of the channel is illustrated. The effects of the diffusion current on the three more important low-frequency dynamic characteristics (the short-circuit gate capacitance, the transconductance, and the drain conductance) are discussed. The surface potential, the quasi-Fermi potential, the surface electric field and the surface carrier concentration along the channel are examined. The complete one-dimensional gradual channel model is inadequate to account for the large drain conductance observed in the saturation range, and it is shown that the electric field longitudinal to the channel current flow must be taken into account near the drain junction where it is larger than the transverse field due to the voltage applied to the gate electrode.

Résumé—Une discussion qualitative de l'opération du dispositif est donnée tout d'abord en employant les schémas d'énergie de bande à trois dimensions. Les caractéristiques théoriques...
EFFECTS OF DIFFUSION CURRENT ON METAL-OXIDE-SEMICONDUCTOR TRANSISTORS

H. C. PAO and C. T. SAH

3. DRAIN CURRENT

\[ I_D = \int_{0}^{x_i} J(x, y) dx \]

where \( \xi \) is the electron quasi-Fermi level measured from the bulk Fermi level and normalized to \( kT/q \). The total drain current is then

\[ I_D = \frac{1}{L} \int_{0}^{L} D_n q Z \left( \frac{d\xi}{dy} \right) \int_{0}^{x_i} n(x, y) dx dy \]

\[ = \left( \frac{kT}{q} \right)^3 \left( \frac{C_0 Z}{2L} \right) \gamma_{\mu_n} \int_{0}^{U_v} \int_{0}^{U_s} \frac{e^{U_v - U_s - \xi}}{F(U, \xi, U_F)} dU d\xi \]

\[ U_G' = \left( q/kT \right) \left( V_G - \phi_{MS} + Q_{z1}/C_0 \right) \]

For a particular device, equation (4) may be calculated numerically. The input data are: the bulk impurity concentration \( N_A \), the physical dimensions of the device and the constant effective carrier
EFFECTS OF DIFFUSION CURRENT ON METAL-OXIDE-SEMICONDUCTOR TRANSISTORS

H. C. PAO and C. T. SAH

PHYSICAL REVIEW VOLUME 91.
NUMBER 3 AUGUST 1, 1953

n-Type Surface Conductivity on p-Type Germanium
W. L. BROWN
Bell Telephone Laboratories, Murray Hill, New Jersey
(Received March 17, 1953)

Fig. 1(a). A sketch of the physical structure of an N-channel MOS transistor. (b–d)
Three-dimensional energy band diagrams depicting (b) the flat-band zero-bias equilibrium
condition, (c) the equilibrium condition under a gate bias and (d) the equilibrium condition
under both drain and gate biases.

Fig. 2. (a) Experimental floating potential curve.
(b) Connections for measurement of channel capacity.
(c) Circuit for channel conductance measurement.
EFFECTS OF DIFFUSION CURRENT ON METAL-OXIDE-SEMICONDUCTOR TRANSISTORS
H. C. PAO and C. T. SAH

3. DRAIN CURRENT

\[ I_D = \int_0^L D_{nq} Z \left( \frac{d\xi}{dy} \right) n(x, y) \, dx \, dy \]

where \( \xi \) is the electron quasi-Fermi level measured from the bulk Fermi level and normalized to \( kT/q \). The total drain current is then

\[ I_D = \frac{1}{L} \int_0^L D_{nq} Z \left( \frac{d\xi}{dy} \right) n(x, y) \, dx \, dy \]

\[ = \left( \frac{kT}{q} \right)^{2} \left( \frac{C_0 Z}{2L} \right) \frac{U_p}{U_{eq}} \int_0^{U_p} \int_0^{U_F} \frac{e^{U-u} - e^{-U-u}}{F(U, \xi, U_F)} \, dU \, d\xi \]

\[ Q_0 = C_D \int_0^{U_p} F(U, \xi, U_F) \, dU \]

\[ \frac{C_{Dx}}{C_0} = 1 - \frac{1}{I_D} \int_0^{U_p} \frac{e^{U-u} - e^{-U-u}}{F(U, \xi, U_F)} \, dU \]

\[ = \frac{1}{I_D} \int_0^{U_p} \frac{e^{U-u} - e^{-U-u}}{F(U, \xi, U_F)} \, dU \]

\[ \int_0^{U_p} \frac{e^{U-u} - e^{-U-u}}{F(U, \xi, U_F)} \, dU \]

For a particular device, equation (4) may be calculated numerically. The input data are: the bulk.

4. OTHER DEVICE PARAMETERS

Several important device parameters are computed in this section. In our previous paper, \textsuperscript{16}
EFFECTS OF DIFFUSION CURRENT ON METAL-OXIDE-SEMICONDUCTOR TRANSISTORS

H. C. PAO and C. T. SAH

3. DRAIN CURRENT

\[ I_D = \int_{0}^{L} J(x, y) \, dx \]

\[ J(x, y) = J_n + J_p \approx J_n = q \mu_n nE_y + q D_n n \xi \]

\[ = -q D_n n \xi \]

where \( \xi \) is the electron quasi-Fermi level measured from the bulk Fermi level and normalized to \( kT/q \). The total drain current is then

\[ I_D = \frac{1}{L} \int_{0}^{L} D_n q Z \left( \frac{d \xi}{dy} \right) \int_{0}^{x} n(x, y) \, dx \, dy \]

\[ = \left( \frac{kT}{q} \right)^2 \left( \frac{C_0 Z}{2L} \right) \mu_n \int_{0}^{u_t} \int_{0}^{u_r} \frac{e^{u-t-u_r}}{F(U, \xi, U_r)} \, dU \, d\xi \]

\[ U_{G'} = (g'kT)(V_G - \phi_{MS} + Q_{ss}/C_0) \]

\[ = U_s + \gamma F(U_s, \xi, U_r) \]

For a particular device, equation (4) may be calculated numerically. The input data are: the bulk impurity concentration \( N_A \), the physical dimensions of the device and the constant effective carrier

Fig. 3. Comparison of the drain current calculated from the bulk charge method and the present method.

\[ I_D = \mu_c Z (dV/dy) \int_{0}^{Q_n} \, \, dz = -\mu_c Z (dV/dy) Q_n \]

\[ = (\mu_c Z/L) \int_{0}^{\phi_n \xi} \, \, -Q_n \, dV \]

\[ = \mu_c Z (dV/dy)(V_0 - \psi_{ss} - \phi_{MS}) \]

\[ + (Q_n + Q_{ss}/C_0) \]

\[ I_D = \mu_c Z (L/V_0 - \psi_{ss} - \phi_{MS} + Q_{ss}/C_0) V_0 \]

\[ - V_l/2 - (4\phi_s V_s/3) ((1 + V_o/2\phi_s)^{2/3} - 1) \].
Fig. 10. The (a) transverse and (b) longitudinal electric field at the surface along the channel with the MOS transistor operating just in saturation.

Fig. 11. The ratio of electric fields along the channel with the MOS transistor operating just in saturation for different impurity concentrations.
5. SOME ELECTROSTATIC PROPERTIES

There are several electrostatic properties of the channel whose variation along the channel is of considerable interest. These are the surface potential, $U_s$, the quasi Fermi potential, $\xi$, the surface electric field, $F(U_s, \xi, U_D)$, and the surface carrier concentration $n_s$. By integrating equation (I) with respect to $\xi$ and setting an arbitrary limit to $\xi$, the normalized distance along the channel measured from the source, $y/L$, may be related to $\xi$.

$$\frac{y}{L} = \frac{1}{I_D'} \int_0^{\xi} \int_0^{U_s} \frac{e^{-u - \xi - U_D}}{F(U, \xi, U_D)} dU d\xi = \frac{I_D'(\xi)}{I_D'(U_D)}$$

(11)

Note that $y/L$ is the dependent variable and it is also the ratio of the total current components up to the point $\xi$ over the total current components in the entire open channel. Thus, this relationship is not valid in the pinch-off region. In Fig. 7, the normalized surface potential $U_s$ is plotted for fixed gate voltages while the drain is maintained saturated in all the cases. The drain voltage is
APPENDIX A

The Poisson equation for the channel may be written as:

\[ \frac{d^2 \psi}{dx^2} = -\rho \]

\[ = -\frac{q}{K_s \varepsilon_0} \left[ p - n + N_D - N_A \right] \quad (A-1) \]

where

\[ p = n_i e^{U - U_s} - n_i e^{U_s - U} \quad (A-2) \]

\[ n = n_i e^{U - U_s} = e^{U - U_s} \quad (A-3) \]

\[ N_A - N_D = n_i (e^{U_s - U} - e^{-U_s}) \quad (A-4) \]

\[ \text{Wrong} \]

The boundary conditions are:

\[ \psi(x) \to 0 \quad \text{as} \quad x \to \infty \quad (A-5) \]

\[ \frac{d\psi(x)}{dx} \to 0 \quad \text{as} \quad x \to \infty \quad (A-6) \]

In units of electrostatic potential

\[ \frac{d^2 U}{dx^2} = \frac{q^2}{kT K_s \varepsilon_0} \]

\[ \times \left[ e^{-U - U_s} - e^{U_s - U} + e^{U_s - U_s} - e^{-U_s} \right] \]

\[ = \frac{1}{L_D^2} \left[ e^{-(\xi/2)} \sinh(U - (\xi/2) - U_s) \right] + \sinh U_s \] \quad (A-7)

\[ \int_0^U \left( \frac{dU}{dx} \right) d \left( \frac{dU}{dx} \right) = \frac{1}{2L_D^2} \int_0^U \left[ e^{U - U_s} - e^{U_s - U} + e^{U_s - U_s} - e^{-U_s} \right] dU \]

\[ \left( \frac{dU}{dx} \right)^2 = \frac{1}{L_D^2} \left[ e^{U - U_s} + e^{U_s - U} + (U - 1)e^{U_s} - (U + e^{-U_s})e^{-U_s} \right] \quad (A-8) \]

\[ \left( \frac{dU}{dx} \right) \frac{U}{L_D} = \frac{1}{L_D} \frac{U}{|U|} F(U, \xi, U_s) \quad (A-9) \]

\[ F(U, \xi, U_s) = \sqrt{[e^{U - U_s} + e^{U_s - U} + (U - 1)e^{U_s} - (U + e^{-U_s})e^{-U_s}]} \quad (A-10) \]

At the surface, \( x = 0, U = U_s \)

\[ E_s = \left( \frac{kT}{q} \right) \left( \frac{dU}{dx} \right) = \frac{U_s}{|U_s|} \left( \frac{kT}{q} \right) F(U_s, \xi, U_s) \]

\[ \left( \frac{dU}{dx} \right) \frac{U}{L_D} = \frac{1}{L_D} \frac{U}{|U|} F(U_s, \xi, U_s) \quad (A-11) \]
Modern Silicon MOS Transistor

- 1972 Barron (Stanford March 1971)
  - Subthreshold Theory and Experiment.
- 1972 Stuart+Eccleston (Liverpool March 1972)
  - Experimental subthreshold data $I_D \sim \exp(qV_G/\alpha kT)$
- 1972-1978 Many on Subthreshold, slope, threshold-voltage
- 1978 Brews (BTL May 1977)
  - Charge sheet theory subthreshold, inversion, saturation.
- 1978 Baccarani, Ruidan, Spadini (Bologna Oct.1977)
- 1979 Van de Wiele (Louvian April 1979)
  - Systematic successive approximation theories.
    - Derived threshold voltage and surface potential formulas for inversion.
    - Subthreshold required separate formula.
- 1978-1980 Many on 2-D effects and subthreshold
  - 1978 Taylor, 1979 Toyabe, 1979 Troutman DIBL, 1980 Klaassen-De Groot,
    1981 Nguyen-Plummer DIBL, 1983 Guebels-Van de Wiele,
    1983 Pierret-Shields
LOW LEVEL CURRENTS IN INSULATED GATE
FIELD EFFECT TRANSISTORS

M. B. BARRON†
General Electric Corporate Research and Development, Schenectady, New York, U.S.A.
(Received 24 March 1971; in revised form 11 August 1971)

Abstract — A theory for low-level current operation in Insulated Gate Field Effect Transistors is
developed. Using the depletion approximation for the semiconductor surface potential, an analytical
expression is obtained which is accurate for gate voltages corresponding to surface operation from
depletion to the onset of strong inversion. Numerical calculations that avoid the limitations on gate
voltage have shown the theory to hold as well for surface potentials corresponding to strong inversion.

NOTATION

\( \begin{array}{ll}
C_D & \text{depletion capacitance per unit area} \\
C_{ox} & \text{oxide capacitance per unit area} \\
D_a & \text{electron diffusion coefficient} \\
D_p & \text{hole diffusion coefficient} \\
\phi & \text{electric field} \\
I_D & \text{drain saturation current} \\
I_S & \text{source current} \\
I(x,y) & \text{total current density} \\
kT/q & \text{thermal voltage (approximately 0.026V at room temperature)} \\
L & \text{transistor channel length} \\
L_D & \text{intrinsic Debye length (2.4 \times 10^{-3} \text{ cm for silicon})} \\
L_{De} & \text{extrinsic Debye length} \\
n & \text{electron density} \\
n_i & \text{intrinsic carrier density} \\
N_A & \text{acceptor density} \\
N_D & \text{donor density} \\
N_s & \text{‘fast’ surface state density per unit area} \\
p & \text{hole density} \\
p_0 & \text{equilibrium minority hole density in } n \text{ region} \\
q & \text{electron charge} \\
Q_{ss} & \text{fast surface-state charge density per unit area} \\
Q_{ox} & \text{immobile oxide charge density per unit area} \\
\end{array} \)

\( \begin{array}{ll}
w & \text{normalized potential} = \frac{q\phi}{kT} \\
w_f & \text{equilibrium Fermi potential (normalized to units of } kT/q) \\
w_c & \text{normalized gate voltage} \\
w_e & \text{normalized electron quasi-Fermi potential} \\
w_h & \text{normalized hole quasi-Fermi potential} \\
V_D & \text{drain voltage} \\
V_g & \text{gate voltage} \\
V_{ef} & \text{effective gate voltage} \left( V_g + Q_{ss}/C_{ox} - \phi_{ss} \right) \\
V_{th} & \text{threshold voltage} \\
W & \text{width of IGFET gate} \\
x, \ y & \text{distance into substrate from } \text{Si–SiO}_2 \text{ interface} \\
x_0, \ y_0 & \text{point in substrate where } \rho = n_i^2/N_D \\
\epsilon & \text{permittivity of } \text{Si} \\
\mu_{ef} & \text{effective mobility of holes at surface} \\
\phi & \text{hole quasi-Fermi potential} = q(\phi_h - \phi_f)/kT \\
\phi_{hs} & \text{equilibrium Fermi potential} \\
\phi_{ss} & \text{metal–semiconductor work function} \\
\phi_p & \text{hole quasi-Fermi potential} \\
\phi & \text{potential} \\
\phi_s & \text{surface potential} \\
\eta & \text{distribution function of surface state density through band gap} \\
\end{array} \)
LOW LEVEL CURRENTS IN INSULATED GATE FIELD EFFECT TRANSISTORS

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(Received 24 March 1971; in revised form 11 August 1971)

Fig. 1. Schematic of p-channel IGFET.

2. THEORETICAL CONSIDERATIONS

A theoretical expression for the source current can be obtained by considering the basic semiconductor current and field relationships. Reconstructing the derivations of Pao and Sah[9] the current density in a semiconductor is given by

\[ J(x, y) = q \left( \mu_a n_0 \frac{\partial \phi}{\partial x} + D_n \frac{\partial N_n}{\partial x} + \mu_p n_0 \frac{\partial \phi}{\partial y} + D_p \frac{\partial N_p}{\partial y} \right) \]  

(3)

If the gradual channel approximation[8] is assumed, and generation currents are ignored, then for a p-channel IGFET equation (3) reduces to

\[ J(y) = q \left( \mu_p n_0 \frac{\partial \phi}{\partial y} - D_p \frac{\partial \phi}{\partial y} \right) \]  

(4)

A hole quasi-Fermi level, \( \phi_h \), can now be defined as

\[ \phi_h = \frac{q}{kT} \log \frac{p}{n_0} + \phi \]  

(5)

and, for convenience, normalized variables can be

Fig. 2. Comparison of experimental and theoretical IGFET characteristics.

\[ u = q \frac{\phi_e}{kT} \]  

\[ v = q \frac{\phi_e}{kT} \ln \frac{N_d}{n_i} \]  

(6)

\[ \xi = q \left( \phi_e - \phi_h \right) / kT \]  

\[ J_s = -q D_n \int_0^{\delta_y} \frac{\partial \phi}{\partial y} \, dz \]  

(8)

where \( \phi_e \) is the equilibrium Fermi level in the substrate, which is assumed to be equal to the electron quasi-Fermi level in the channel[3]. By combining equations (5) and (6) with equation (4) and making use of the Einstein relation, \( D_e = \frac{kT}{n_i} \), the hole current density in the surface

Fig. 3. Source current and drain current vs. gate voltage.

\[ J_f = -q D_p \int_0^{\delta_y} \frac{\partial \phi}{\partial y} \, dz \]  

(9)

The corresponding source current is found by integrating over the active cross-section area of the channel. Performing the integration yields.

\[ I_s = -q D_n \int_0^{\delta_y} \frac{\partial \phi}{\partial y} \, dz \]  

where \( \delta_y \) is defined as the point in the substrate where \( p = n_0 / N_0 \). Equation (8) may be integrated over \( y \) from \( y = 0 \) to \( y = L \), giving

\[ I_s = -q D_n \int_0^{\delta_y} \frac{\partial \phi}{\partial y} \, dz \]  

(10)

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A History of MOS Transistor Modeling by Chih-Tang Sah
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3. APPROXIMATE LOW-LEVEL CURRENT SOLUTION

Attention will be focused first on operation corresponding to surface potentials (near the source) in the range

$$2u < u < -2,$$

which covers the surface modes from depletion through mild inversion (but short of the classical inversion point). For these values of $u$, the ionized donors dominate the semiconductor space charge, and the field function equation (12) can be approximated by

$$F(u, \xi, u_0) = \sqrt{1-(u+1)e^{-\xi}}, \quad 2u < u < -2.$$  

Under these conditions, the equation for the source current is

$$I_s = \frac{qWD_mL_e}{L} \int_0^{u_0} \frac{e^{-\xi}}{F(u, \xi, u_0)} du,$$

with the surface potential, $u_s$, being related to the gate voltage, $V_g$, by

$$V_g = \frac{q}{Q} \phi_n - (Q_0 + Q_n(u_0))C_{ox}.$$  

Although it is possible to numerically integrate equation (14), an approximate analytic solution is desirable. One such solution is described below.
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4. COMPARISON OF THEORY WITH EXPERIMENTAL DATA

In Fig. 7 source current as calculated from equation (25) is compared with actual device characteristics for an IGFET with \( W/L = 12 \), \( N_0 = 2.5 \times 10^{13} \text{ cm}^{-2} \), \( x_0 = 1400 \text{ Å} \) and \( V_D = 1 \text{ V} \). The calculations were done assuming a uniform fast surface state density of \( N_{ss} = 8 \times 10^{14} \text{ cm}^{-2} \) and a diffusion constant of \( D_D = 5 \text{ cm}^2/\text{sec} \).

Since \( Q_m \) was not known for this device, the voltages were arbitrarily matched at \( I_s = 1 \text{ pA} \) when plotting the curves. The mobility, \( \mu = (q/kT)D_p \), has been assumed to be constant over the range of

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Acknowledgement—The author would like to thank Dr. R. L. Pritchard for his valuable discussions during the course of this research and for his helpful comments on this paper.

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Subthreshold $I_D \propto \exp(qV_G/\alpha kT)$

1972 Stuart & Eccleston (Liverpool)
Analytical i.g.f.e.t. model including drift and diffusion currents

G. Baccarani, M. Rudan and G. Spadini

Indexing terms: Insulated-gate field-effect transistors, Semiconductor device models

Abstract: An analytical i.g.f.e.t. model including drift and diffusion currents along the channel is developed. The theory, which is based on a gradual-channel approximation, is essentially equivalent to the double-integral formula by Pao and Sah, which provides correct results both in weak and in strong inversion. I.G.F.E.T. characteristics such as drain current, transconductance and output conductance are analytically expressed against the surface potential at the source and drain edges of the channel, which can be numerically evaluated in a few iterative steps. The model therefore seems suitable for c.a.d. applications.
Analytical i.g.f.e.t. model including drift and diffusion currents

G. Baccarani, M.-Rudan and G. Spadini

Table 1: Normalising factors

<table>
<thead>
<tr>
<th>Physical quantities</th>
<th>Normalising factors</th>
</tr>
</thead>
<tbody>
<tr>
<td>x, y, L, W</td>
<td></td>
</tr>
<tr>
<td>U, U_s, U_sc, U_D, U_G, U_T, U_FB, U_F, U_F, U</td>
<td>kT/q</td>
</tr>
<tr>
<td>Q_s, Q_o, Q_l</td>
<td>q n_L_i</td>
</tr>
<tr>
<td>C_ox</td>
<td>e_s/L_i</td>
</tr>
<tr>
<td>I_D</td>
<td>k T / \mu n_L_i</td>
</tr>
<tr>
<td>\eta_m, \eta_D</td>
<td>q u^2 n_L_i</td>
</tr>
</tbody>
</table>

2. Inversion-layer and bulk fixed charges

\[ U_s = 2 U_F + \xi \]

\[ I_D = - \frac{W}{L} \int_{U_S}^{U_D} Q_l(U_G, \xi) d\xi \]

\[ Q_l = Q_s - Q_o \]

\[ Q_s = -\sqrt{2} \left( e^{U_F}(e^{-U_s} + U_s - 1) \right) \]

\[ + \left( e^{U_s} - e^{-U_s} - e^{-U_F} \right) (U_s - U_F) \]

\[ \approx -\sqrt{2} \left( e^{U_F}(U_s - 1) + e^{U_s} - e^{-U_F} \right) \]

\[ Q_o = -\sqrt{2} \left( e^{U_F}(U_F - 1) \right) \]

\[ Q_s = e^{-U_F - \xi} \int_{0}^{U_s} (e^U - 1) \left( \frac{dU}{dx} \right)^{-1} dU \]

\[ Q_o = e^{U_F} \int_{0}^{U_s} (1 - e^{-U}) \left( \frac{dU}{dx} \right) dU \]

\[ Q_s = Q_l + Q_o \]

\[ \frac{dU}{dx} = -\sqrt{2} \left( e^{U_F}(e^{-U} + U - 1) \right) \]

\[ + e^{-U_F}(e^{U_F} - U - e^{-U}) \]
Analytical i.g.f.e.t. model including drift and diffusion currents

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\[
\begin{align*}
I_D &= \frac{W}{L} C_{ox} \left( \frac{U_G - U_{FB} + 2U_F}{3} + \frac{2(U_s - 1)^{3/2}}{\sqrt{3}} + \frac{4(U_s - 1)^{1/2}}{\sqrt{3}} \right. \\
&\left. - 2(U_s - 1)^{1/2} \ln \left( \sqrt{U_s} - 1 + \sqrt{U_s} - 1 \right) \right) \\
&\left. + 2(U_s - 1)^{1/2} \ln \left( \sqrt{U_s} - 1 - \sqrt{U_s} - 1 \right) \right) \\
&\left. \left( \frac{U_s}{U_s} \right)^{1/2} \\
U_e &= U_G - U_{FB} + 1/(2\delta) \\
&\left. - \frac{[(U_G - U_{FB} - 1 + 1/(4\delta)]/\delta} \right)^{1/2} \\
U_e &= U_G - U_{FB} + 1/(2\delta) \\
&\left. + \frac{[(U_G - U_{FB} - 1 + 1/(4\delta)]/\delta} \right)^{1/2} \\
U_s &= 2U_F + \xi \\
dU_s &= d\xi \\
\end{align*}
\]

I.G.F.E.T. drain current

Eqn. 8a does not allow derivation of an explicit \( U_s = U_s \) (\( U_G, \xi \)) function. To evaluate the integral in eqn. 1, it is therefore necessary to change the integration variable. We have

\[
\begin{align*}
I_D &= \frac{W}{L} \int \frac{U_s}{U_s(1)} dU_s \\
&= \frac{W}{L} \int \frac{U_s}{U_s(1)} \left[ C_{ox}(U_G - U_{FB} - U_s) - \sqrt{2e^U F^m} (U_s - 1)^{1/2} \right] dU_s \\
&= -\frac{2}{3} \left( \frac{U_D + 2U_F - 1}{\sqrt{2}} \right) \left( U_s + 2U_F - 1 \right)^{1/2} \\
&= \frac{W}{L} C_{ox} \left[ (U_G - U_{FB} - 2U_F) (U_D - U_S) - \frac{1}{4}(U_F - U_S) \right] \\
&\left. - \frac{2}{3} \left( \frac{(U_D + 2U_F - 1)}{(U_s + 2U_F - 1)^{1/2}} \right) \right) \\
&= \frac{W}{L} C_{ox} \left[ \left( U_D - U_S - 2U_F \right) (U_D - U_S) - \frac{1}{4}(U_F - U_S) \right] \\
&\left. - \frac{2}{3} \left( \frac{(U_D + 2U_F - 1)}{(U_s + 2U_F - 1)^{1/2}} \right) \right) \\
&= \frac{W}{L} e^{-U_F} \int_{U_S}^{U_D} e^{-\xi} d\xi \\
&= \frac{W}{L} e^{-U_F} \int_{U_S}^{U_D} e^{-\xi} \left( \frac{dU}{dx} \right)^{1/2} dU \\
&= \frac{W}{L} e^{-U_S} \left( \frac{dU}{dx} \right)^{1/2} \left( e^{-U_S} - e^{-U_D} \right) \\
&\left. \right) \\
\end{align*}
\]
Analytical i.g.f.e.t. model including drift and diffusion currents

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Fig. 5 Drain current $I_D$ against drain voltage $U_D$ for various gate voltages: comparison of eqns. 14, 17 and 18

Fig. 6 I.G.F.E.T. transfer characteristic, with current ranging from subthreshold to high level: comparison of eqns. 14, 18 and 19
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    1981 Nguyen-Plummer DIBL, 1983 Guebels-Van de Wiele,
    1983 Pierret-Shields
A LONG-CHANNEL MOSFET MODEL

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Abstract—A MOSFET model valid for long-channel devices is derived. The model describes correctly the drain current and the small signal parameters in all regions of operation, including the subthreshold regime and the saturation regime. The model contains as an approximation the charge-sheet model proposed by Brews [1]. Mobility variations along the channel, resulting from the normal and lateral electric fields, can be taken into account.

CONCLUSION

A MOSFET model valid for long-channel devices has been derived, which contains as an approximation the charge-sheet model proposed by Brews [1]. Both models describe correctly the drain current and the small signal parameters in the subthreshold, the non-saturation and the saturation regions. The fact that the charge-sheet model is accurate to within 1.5% implies that the shape of the finite inversion layer and its variation along the channel is indeed unimportant [1] for the current characteristics of long-channel MOSFETS.

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$p = N_A \exp \left( -\beta (\phi - V_B) \right)$

(1)

$n = (n_e^2/N_A) \exp \left( \beta (\phi - V(y)) \right)$

(2)

$Q_{sc}(y) = -\lambda C_{ox} \left[ \phi_s - V_B + \frac{1}{\beta} \exp \left( -\beta (\phi_s - V_B) \right) - 1 \right]$

+ $\exp \left( \beta (\phi_s - 2\phi_F - V) \right) - \exp \left( \beta (V_B - 2\phi_F - V) \right) \right)^{1/2}$

(3)

$\lambda = (2e_oxN_A)^{1/2}C_{ox}$

(4)

$\phi_F = \frac{1}{\beta} \ln \left( \frac{N_A}{n_i} \right)$

(5)

and assuming that $\exp \left( -2\beta \phi_F \right) < 1$.

Gauss' law: $Q_{sc} = -C_{ox}(V_G - V_{FB} - \phi_s)$

(6)

$Q_{sc} = -\lambda C_{ox} \left[ \frac{1}{\beta} \exp \left( \beta (\phi_s - 2\phi_F - V) \right) \right]^{1/2}$

(7)

$\phi_s = 2\phi_F + V(y) + \frac{1}{\beta} \ln \left( \beta \lambda^2 \right) + \frac{2}{\beta} \ln \left( V_G - V_{FB} - \phi_s \right)$

(8)

$\phi_s' = 2\phi_F + V(y) + \frac{1}{\beta} \ln \left( \beta \lambda^2 \right) + \frac{2}{\beta} \ln \left( V_G - V_{FB} - \phi_s \right)$

(9)

$\phi_s = 2\phi_F + V(y)$

(10)

$Q_D = -\lambda C_{ox} \left( \phi_s - V_B - \frac{1}{\beta} \right)^{1/2}$

(11)

$\phi_s = V_G - V_{FB} + (\lambda^2/2) - \lambda [(\lambda/2)^2 + V_s]^{1/2}$

(12)

$V_o = V_G - V_{FB} - V_B - \frac{1}{\beta}$

(13)

The previous approximations for $\phi_s$ are illustrated in Fig. 1.
A LONG-CHANNEL MOSFET MODEL

F. VAN DE WIELE

\[ V_I = V_G - V_{FB} - 2\phi_F + (\lambda/2) - \lambda[(\lambda/2)^2 + V_o]^{1/2} \]
\[ - \frac{1}{2} \ln \beta - \frac{2}{\beta} \ln \{(\lambda/2) + (\lambda/2)^2 + V_o\}^{1/2}. \]

What is the physical significance of \( V_I \)? The free
\[ Q_N = Q_{sc} - Q_D \]
to the definition of \( V_I \): \( Q_N(V_I) = 0 \).
i.e. \( V_I \) can be considered as the drain saturation poten-
\[ V_T = V_S + V_{FB} + 2\phi_F - (\lambda/2) \]
\[ + \lambda \left[ (\lambda/2)^2 + V_T - V_{FB} - V_B - \frac{1}{\beta} \right]^{1/2} + \frac{1}{\beta} \ln \beta \]
\[ + \frac{2}{\beta} \ln \left\{ (\lambda/2)^2 + V_T - V_{FB} - V_B - \frac{1}{\beta} \right\}^{1/2}. \]

The Gauss' law: \( Q_{sc} = -C_{ox}(V_O - V_{FB} - \phi_s) \)
\[ \phi_s = 2\phi_F + V(y) + \frac{1}{\beta} \ln (\beta/\lambda^2) + \frac{2}{\beta} \ln (V_O - V_{FB} - \phi_s). \]
\[ \phi_s^{\phi_s} = 2\phi_F + V(y) + \frac{1}{\beta} \ln (\beta/\lambda^2) + \frac{2}{\beta} \ln (V_O - V_{FB} - \phi_s'). \]
\[ Q_D = -\lambda C_{ox} \left( \phi_s - V_B - \frac{1}{\beta} \right)^{1/2}. \]
\[ \phi_s = V_O - V_{FB} + (\lambda/2) - \lambda[(\lambda/2)^2 + V_o]^{1/2} \]
\[ V_o = V_O - V_{FB} - V_B - \frac{1}{\beta}. \]

\[ \frac{dV}{d\phi_s} = 1 + \frac{2}{\beta} \frac{V_O - V_{FB} - \phi_s + (\lambda/2)}{(V_O - V_{FB} - \phi_s)^2 - \lambda^2 (\phi_s - V_B) + (\lambda/2)(1 - \beta)}. \]

\[ \frac{dV}{d\phi_s} = 1 + \frac{\lambda^2 C_{ox} - 2Q_{sc}}{Q_N(Q_{sc} + Q_D)}. \]
\[ \phi_s(L) = \phi_s(0) + (V_D - V_S). \]
\[ J_s(y) = \mu_n \left[ -\sigma (d\phi_s/dy) + \frac{1}{\beta} (\sigma n/dy) \right]. \]
\[ J_s(y) = -\mu_n (dV/dy). \]
\[ I_D = W \mu_n Q_N (dV/dy). \]
\[ \frac{W}{L} \int_0^L \frac{dV}{d\mu_n} = \int_{V_S}^{V_D} Q_N dV. \]
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According to (20) one obtains, since $Q_{sc} = Q_N + Q_D$,}

$$I_D = \frac{W}{L} \mu_* \int_{\phi_s(0)}^{\phi_s(L)} \left( Q_N - \frac{C_{ox}}{\beta} \left[ 1 + \frac{Q_N}{Q_N + 2Q_D} - \frac{\lambda^2 C_{ox}}{2Q_D} \right] \right) d\phi_s.$$  \hfill (31)

$$Q_N - \frac{C_{ox}}{\beta} \left[ 1 + \frac{Q_N}{Q_N + 2Q_D} - \frac{\lambda^2 C_{ox}}{2Q_D} \right] = Q_N - \frac{C_{ox}}{\beta} \left[ 1 - \frac{\lambda^2 C_{ox}}{2Q_D} \right].$$  \hfill (32)

$$- I_D^{(1)} \frac{L}{W \mu_* C_{ox}} = \left( V_G - V_{FB} - 2\phi_F \right) \left( V_D - V_S \right)$$

$$\frac{1}{2} \left( V_D^2 - V_S^2 \right) - \frac{2}{3} \left( \frac{V_D + 2\phi_F - V_B - 1}{\beta} \right)^{3/2}$$

$$- \left( V_S + 2\phi_F - V_B - 1 \right)^{3/2}. \hfill (27)$$

A better result is obtained if the surface potential is approximated by:

$$\phi_s = \phi_{so} + V \hfill (28)$$

$$- I_D^{(1)} \frac{L}{W \mu_* C_{ox}} = \left( V_G - V_{FB} - \phi_{so} \right) \left( V_D - V_S \right)$$

$$\frac{1}{2} \left( V_D^2 - V_S^2 \right) - \frac{2}{3} \left( \frac{V_D + \phi_{so} - V_B - 1}{\beta} \right)^{3/2}$$

$$- \left( V_S + \phi_{so} - V_B - 1 \right)^{3/2}. \hfill (29)$$

$$I_D = \frac{W}{L} \mu_* \int_{\phi_s(0)}^{\phi_s(L)} Q_N \frac{dV}{d\phi_s} d\phi_s. \hfill (30)$$

$$I_D = \frac{W}{L} \mu_* \int_{V_1}^{V_2} Q_N \frac{dV}{d\phi_s} d\phi_s.$$  \hfill (36)}

$$Q_N = - \frac{1}{2\beta} \lambda C_{ox} \left( \phi_s - V_B - \frac{1}{\beta} \right) \left( \phi_s - \frac{1}{\beta} \right). \hfill (38)$$

$$- I_D^{(3)} \frac{L}{W \mu_* C_{ox}} = \frac{\lambda}{2} \left( C_{ox}^{1/2} - \frac{\lambda}{2} \right)$$

$$\times \exp \left( \beta \left( \phi_s - 2\phi_F - V \right) \right) \hfill (39)$$
A History of MOS Transistor Modeling by Chih-Tang Sah
Compare Models with 66XT0139
Early History Review Finished
For Recent Developments on
Surface Potential Model
vs
Inversion Charge Model
Please Attend
the 10-author Invited Paper
Thank You