

**Workshop on Compact Modeling**  
***The 8th International Conference on Modeling and Simulation of Microsystems***

(Anaheim, California, USA. May 10–12, 2005)

**Overview**

Compact Models (CMs) for circuit simulation have been at the heart of CAD tools for circuit design over the past decades, and are playing an ever increasingly important role in the nanometer system-on-chip (SOC) era. Although not highly “visible” to circuit designers and technology developers, a compact model plays the key role in accuracy and efficiency of the circuit simulator being used by designers as well as a bridge to the technology to which the design is to be fabricated. Like the role CM is played in circuit simulation, CM developers play the similar role in bridging the circuit designers and technology developers. As the mainstream MOS technology is scaled into the nanometer regime, development of a truly physical and predictive compact model for circuit simulation that covers geometry, bias, temperature, DC, AC, RF, and noise characteristics becomes a major challenge. This demands that CM developers work more closely with the technology people and the design community.

**Objective**

***Workshop on Compact Modeling (WCM)*** is one of the first of its kind in bringing people in the CM field together. The *objective* of WCM is to create a truly open forum for discussion among experts in the field as well as feedback from technology developers, circuit designers, and CAD tool vendors. The creation of WCM is a natural response of the CM community to the increasing demand in the field, and it will position itself as a premier forum for CM developers in information exchange and promotion of modeling diversity. Ultimately, the result of such a forum will benefit not only the model developers, but also as a service to the entire technology, modeling, and design communities.

**Scope**

The *scope* of WCM covers compact models for circuit simulation, which is centered at the mainstream MOS intrinsic models and extended to SOI, bipolar, interconnect, extrinsic, statistical, numerical-based, and reliability models. The key application is for circuit simulation and, hence, numerical simulation and pure theoretical and experimental work will not be within the scope of WCM.

**Topics**

The *topics* for WCM are largely categorized into the following areas:

- Bulk MOS intrinsic models
- SOI/double-gate/multiple-gate/floating-gate MOS models
- Bipolar/HBT/SiGe/GaN/JFET models
- RF/noise/scalable capacitance/NQS models
- Statistical/predictive/process-based models
- Interconnection/passive device models

- Extrinsic/parasitic element models
- Reliability/hot carrier/tunneling/ESD models
- Atomic-level/quantum-mechanical compact models
- Numerical/TCAD/behavioral/table-based models
- Model parameter extraction and optimization
- Model–simulator interface and standardization

### WCM-MSM2005

The fourth *Workshop on Compact Modeling* (WCM-MSM2005) will be held in association with *the 8th International Conference on Modeling and Simulation of Microsystems* at **Nanotech 2005** in Anaheim, California, USA on May 10–12, 2004. It is planned to have an *Invited-Speaker Session*, a *Forum* and an *Evening Panel Discussion*, as well as a contributed *Poster Session*. Highlights of WCM2005 include a Keynote paper by Prof. Chih-Tang Sah and a special joint-authored review paper by invited key contributors to be presented at the Forum.

### Invited Speakers

Invited speakers from all over the world are listed below:

- Narain Arora, *Cadence Design Systems, USA*
- Matthias Bucher, *Technical University of Crete, Greece*
- Yuhua Cheng, *Siliconlinx, USA*
- Jamal Deen, *McMaster University, Canada*
- Robert Dutton, *Stanford University, USA*
- Carlos Galup-Montoro, *Universidade Federal de Santa Catarina, Brazil*
- Gennady Gildenblat, *Pennsylvania State University, USA*
- Keith Green, *Texas Instruments, USA*
- Chenming Hu, *University of California at Berkeley, USA*
- Benjamín Iñíguez, *Universitat Rovira i Virgili, Spain*
- Dirk Klaassen, *Philips Research Laboratories, The Netherlands*
- Ronald van Langevelde, *Philips Research Laboratories, The Netherlands*
- Luca Larcher, *Università di Modena e Reggio Emilia, Italy*
- Shiuh-Wuu Lee, *Intel, USA*
- Juin Liou, *University of Central Florida, USA*
- Colin McAndrew, *Freescale Semiconductor, USA*
- Mitiko Miura-Mattausch, *Hiroshima University, Japan*
- Ali Niknejad, *University of California at Berkeley, USA*
- Guofu Niu, *Auburn University, USA*
- Adelmo Ortiz-Conde, *Universidad Simón Bolívar, Venezuela*
- Rafael Rios, *Intel, USA*
- Chih-Tang Sah, *University of Florida, USA*
- Samar Saha, *Silicon Storage Technology, USA*
- Michael Schröter, *University of Technology Dresden, Germany*
- Yuan Taur, *University of California at San Diego, USA*
- Josef Watts, *IBM, USA*
- Xing Zhou, *Nanyang Technological University, Singapore*

## **Workshop Program**

### **Keynote:**

- Chih-Tang Sah, *University of Florida, US*  
“A History of MOS Transistor Compact Modeling”

There are 21 invited papers, which are categorized in the following topic areas:

### ***Bulk MOS intrinsic models:***

- Advances in Charge-Based Compact MOSFET Modelling  
*Matthias Bucher, Technical University of Crete, GR*
- Comparison of Surface Potential and Charge-based MOSFET Core Models  
*Carlos Galup-Montoro, Universidade Federal de Santa Catarina, BR*
- Introduction to PSP MOSFET Model  
*Gennady Gildenblat, Pennsylvania State University, US*
- Unified Regional Charge-based Versus Surface-potential-based Compact Modeling Approaches  
*Xing Zhou, Nanyang Technological University, SG*

### ***RF modeling:***

- RF-MOSFET Model Parameter Extraction with HiSIM  
*Mitiko Miura-Mattausch, Hiroshima University, JP*
- Challenges in Compact Modeling for RF and Microwave Applications  
*Ali Niknejad, University of California at Berkeley, US*
- A Study of Figures of Merit for the High Frequency Behavior of MOSFETs in RF IC Applications  
*Yuhua Cheng, Siliconlinx, US*

### ***Double/multiple-gate MOS models:***

- Compact Modeling of Multiple-gate SOI MOSFETs  
*Benjamín Iñíguez, Universitat Rovira i Virgili, ES*
- Analytic Solution for the Drain Current of Undoped Symmetric Dual-Gate MOSFET  
*Adelmo Ortiz-Conde, Universidad Simón Bolívar, VE*
- Physics-Based, Non-Charge-Sheet Compact Modeling of Double-Gate MOSFETs  
*Yuan Taur, University of California at San Diego, US*

### ***High-K:***

- Mobility Extraction and Compact Modeling for FETs Using High-K Gate Materials  
*Robert Dutton, Stanford University, US*

### ***Noise modeling:***

- The Effects of the Gate Tunneling Current on the High Frequency Noise Parameters of MOSFETs  
*Jamal Deen, McMaster University, CA*
- Correlated Noise Modeling and Simulation

*Colin McAndrew, Freescale Semiconductor, US*

***Interconnect models:***

- Modeling and Characterization of High Frequency Effects in ULSI Interconnects  
*Narain Arora, Cadence Design Systems, US*

***Modeling for design:***

- Modeling for Pre-Silicon Design Verification  
*Shiuh-Wuu Lee, Intel, US*
- Modeling FET Variation Within a Chip as a Function of Circuit Design and Layout Choices  
*Josef Watts, IBM, US*

***High-voltage LDMOD models:***

- Compact Modelling of High-Voltage LDMOD Devices  
*Dirk Klaassen, Philips Research Laboratories, NE*

***Bipolar/HBT models:***

- Two-/Three-Dimensional GICCR for Si/SiGe Bipolar Transistors  
*Michael Schröter, University of Technology Dresden, DE*
- Physics and Modeling of Noise in SiGe HBT Devices and Circuits  
*Guofu Niu, Auburn University, US*

***JFET models:***

- Compact Modeling of Four-Terminal Junction Field-Effect Transistors  
*Juin Liou, University of Central Florida, US*

***Floating-gate models:***

- Statistical Simulations of Oxide Leakage Current in MOS Transistor and Floating Gate Memories  
*Luca Larcher, Università di Modena e Reggio Emilia, IT*

**Forum**

A special 2-hour **Forum** is organized to focus on MOSFET *Compact Model Utopia*, with the topic on:

***Surface-potential versus charge based approaches to MOSFET compact modeling.***

A special *joint-authored review paper* is planned with invited key contributors in the field, to be edited by *Josef Watts* (IBM) and presented by *Colin McAndrew* (Freescale) on behalf of all the co-authors, followed by invited Forum presenters from representative model developers of surface-potential and charge-based approaches. This Forum represents an important event and milestone for WCM in bringing people together in the CM field.

**Forum chair:**

Colin McAndrew, *Freescale Semiconductor, USA*

**Joint paper co-authors:**

- Josef Watts, *IBM, USA*
- Colin McAndrew, *Freescale Semiconductor, USA*
- Christian Enz, *Swiss Center for Electronics and Microtechnology, Switzerland*
- Carlos Galup-Montoro, *Universidade Federal de Santa Catarina, Brazil*
- Gennady Gildenblat, *Pennsylvania State University, USA*
- Chenming Hu, *University of California at Berkeley, USA*
- Ronald van Langenvelde, *Philips Research Laboratories, The Netherlands*
- Mitiko Miura-Mattausch, *Hiroshima University, Japan*
- Rafael Rios, *Intel, USA*
- Chih-Tang Sah, *University of Florida, USA*

**Forum presenters:**

- Colin McAndrew, *Freescale Semiconductor, USA*
- Matthias Bucher, *Technical University of Crete, Greece*
- Carlos Galup-Montoro, *Universidade Federal de Santa Catarina, Brazil*
- Gennady Gildenblat, *Pennsylvania State University, USA*
- Chenming Hu, *University of California at Berkeley, USA*
- Ronald van Langevelde, *Philips Research Laboratories, The Netherlands*
- Mitiko Miura-Mattausch, *Hiroshima University, Japan*
- Rafael Rios, *Intel, USA*
- Yuan Taur, *University of California at San Diego, USA*

**Evening Panel Discussion**

An evening **Panel** discussion is planned, continuing the debate on different modeling approaches in the Forum as well as on MOSFET *Compact Model Development Utopia*, with the question:

***How to engage a diversified model developer community towards the same ultimate goal?***

Some of the proposed questions include:

- *Can a “best model” be built out of “best pieces” from various sources?*
- *How many MOSFET models do we need?*
- *What does it take to move a model from academia to industry?*
- *Do we need standard models or model standards?*

**Panel chair:**

Narain Arora, *Cadence Design Systems, USA*

**Moderator:**

Josef Watts, *IBM, USA*

**Panelists:**

- Matthias Bucher, *Technical University of Crete, Greece*
- Gennady Gildenblat, *Pennsylvania State University, USA*
- Keith Green, *Texas Instruments, USA*
- Chenming Hu, *University of California at Berkeley, USA*
- Shiuh-Wuu Lee, *Intel, USA*

- Mitiko Miura-Mattausch, *Hiroshima University, Japan*
- Samar Saha, *Silicon Storage Technology, USA*

### Poster Session

Poster presentations in the scope of “compact models for circuit simulation” are solicited. A **10-minute oral briefing** for each poster paper is planned. Contributed poster papers are listed below.

- Optimized Compact MOS Transistor Model from the Exact 4-component Theory  
*Bin B. Jie, University of Florida, US*
- All-Region MOS Model of Mismatch due to Random Dopant Placement  
*C. Galup-Montoro, Universidade Federal de Santa Catarina, BR*
- Analog Design Tool Based on the ACM Model  
*C. Galup-Montoro, Universidade Federal de Santa Catarina, BR*
- Extraction of MOSFET Effective Channel Length and Width Based on the Transconductance-to-Current Ratio  
*A. I. A. Cunha, Federal University of Bahia, BR*
- Unambiguous Extraction of Threshold Voltage Based on the Transconductance-to-Current Ratio  
*A. I. A. Cunha, Federal University of Bahia, BR*
- One-Iteration Parameter Extraction for Length/Width-Dependent Threshold Voltage and Unified Drain Current Model  
*Siau Ben Chiah, Nanyang Technological University, SG*
- Unified Regional Charge-Based MOSFET Model Calibration  
*Siau Ben Chiah, Nanyang Technological University, SG*
- RF Modeling for FDSOI MOSFET and Self Heating Effect on RF Parameter Extraction  
*Hui Wan, University of California at Berkeley, US*
- The Surface-Potential-Based Model HiSIM-SOI and Its Application to 1/f Noise in Fully-Depleted SOI-MOSFETs  
*N. Sadachika, Hiroshima University, JP*
- An *A Priori* Hysteresis Modeling Methodology for Improved Efficiency and Model Accuracy in Advanced PD SOI Technologies  
*Qiang Chen, AMD, US*
- SPICE Modeling of Multiple Correlated Electrical Effects of Dopant Fluctuations  
*Yoo-Mi Lee, IBM, US*
- A Compact Physical Model for Critical Quantum Mechanical Effects on MOSFET  
*Lihui Wang, Georgia Institute of Technology, US*
- A Compact model to Predict Quantized Sub-Band Energy Levels and Inversion Layer Centroid of MOSFET with Parabolic Potential Well Approximation  
*Jin He, University of California at Berkeley, US*
- A Compact Model for the Threshold Voltage of Silicon Nanowire MOS Transistors Including 2D-Quantum Confinement Effects  
*K. Nehari, Laboratoire Matériaux et Microélectronique de Provence, FR*
- Compact Modeling of Threshold Voltage in Double-Gate MOSFET Including Quantum Mechanical and Short Channel Effects  
*K. Nehari, Laboratory for Materials and Microelectronics of Provence, FR*
- Compact Model for Ultra-Short Channel Four-Terminal DG MOSFETs for Exploring Circuit Characteristics  
*T. Nakagawa, National Institute of Advanced Industrial Science and Technology, JP*

## WCM-MSM2005

- Device Parameter Extraction from Fabricated Double-Gate MOSFETs  
*Toshiyuki Tsutsumi, National Institute of Advanced Industrial Science and Technology, JP*
- A Compact I-V Model for FinFETs Comprising Multi-Dimensional Electrostatics and Quantum Mechanical Effects  
*Zhiping Yu, Tsinghua University, CN*
- How to Design for Analog Yield Using Monte Carlo Mismatch SPICE Models  
*Philip Beow Yew Tan, Silterra Malaysia, MY*
- Modeling Snapback and Rise-time Effects in TLP Testing for ESD MOS Devices Using BSIM3 and VBIC Models  
*Yuanzhong Zhou, Fairchild Semiconductor, US*
- Airgap and Line Slope Modeling for Interconnect  
*F. Badrieh, Cypress Semiconductor, US*
- HiSIM-1.2: The Effective Gate Length Validation with the Capacitance Data  
*Yoshihisa Iino, Silvaco Japan, JP*
- An Optimization Method of Deep Submicron SOI Compact Model Parameter Extraction  
*Y. Mahotin, Synopsys, US*

### **Call for Participation**

Workshop on Compact Modeling is initiated as a forum for model developers as well as interaction with the technology/design communities. It is mainly in the form of invited presentations for the specific topics in the compact modeling area. The topics cover all important aspects of compact model development and deployment, within the main theme – *compact models for circuit simulation*. Please visit the following website for updates:

<http://www.nsti.org/Nanotech2005/WCM2005/>

<http://www.ntu.edu.sg/home/exzhou/WCM/WCM2005/wcm05.htm>

For WCM-related enquiries, please contact *Dr. Xing Zhou* ([exzhou@ntu.edu.sg](mailto:exzhou@ntu.edu.sg)). For general MSM-related enquiries, please contact *Ms. Sarah Wenning* ([wenning@nsti.org](mailto:wenning@nsti.org)).

WCM-MSM2005, being the fourth one, will prove to be interesting and useful for people in a broad spectrum of fields: compact model developers, process engineers, device physicists, and circuit designers, in a variety of disciplines: universities, research institutions, chip manufacturers, wafer fabs, fabless companies, consulting firms, parameter-extraction tool and circuit-simulator vendors.

All are invited to participate in this exciting event!

#### WCM websites:

<http://www.nsti.org/Nanotech2005/WCM2005/>

<http://www.ntu.edu.sg/home/exzhou/WCM/>

**(Updated: April 21, 2005)**