Technology Limits and Compact Model for SiGe Scaled FETs


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Outline

• Stress relaxation effects by Shallow-Trench Isolations (STI)

• High current operations of strained-Si MOS for Electro-Static Discharge (ESD)

• Compact junction capacitance model for circuit simulation
STI Effects on Strained-Si/SiGe

- Tensile stress in strained-Si increases electron mobility
- Impact of STI-induced compressive stress?

STI

strained Si
(thickness=20nm)

Lg

gate

Si$_{0.8}$Ge$_{0.2}$

strained Si NMOS

L$_{active}$

2D tensile stress contours

STI

1033MPa

-200MPa

L$_{active}$=0.4µm

STI

350MPa

-400MPa

L$_{active}$=0.1µm

L$_{active}$=0.1µm (L$_g$=25nm)

L$_{active}$=0.4µm (L$_g$=0.1µm)
Stress Relaxation for Active Lengths

- Enhanced stress relaxation in strained-Si layers for shorter active lengths ($L_{\text{active}}$): strain is reduced by $\sim 2/3$ from $L_{\text{active}} = 0.4 \mu m$ to $0.1 \mu m$
3D Stress Simulation

- 3D (bi-axial) stress simulation with STI process
  \( L_{\text{active}} = 0.3 \mu m, \ W/L = 0.7 \mu m/0.1 \mu m \)

Initial stress (lattice mismatch strain)

After STI

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3D Stress Simulation (Cont.)

- Stress contours ($S_{xx}$) for $W/L=0.7\mu m/0.1\mu m$
Mobility Degradation

- STI thermal process-dependent stress relaxation and mobility degradation: enhanced stress relaxation for high temperature thermal conditions

![Diagram showing stress relaxation and mobility enhancement](image)
Mobility Degradation

- Enhanced mobility degradation for high temperature thermal condition from the stress-induced mobility model (Egley model) based on anisotropic band shift

![Graph of ID-VG and gm-VG for 1s,800°C and 10s,850°C]
**STI Effects to Narrow Width Devices**

- Severe stress relaxation for narrow width devices with small active width/length (i.e. SRAM cell transistor)

![Diagrams showing stress relaxation comparison between narrow and wide devices](image)
Stress Relaxation of Width Effects

- Less mobility enhancement for narrow width devices—a possible limitation of S-Si device for beyond 25nm node
High-Current Operation in S-Si

• x15 lower thermal conductivity of Si$_{0.8}$Ge$_{0.2}$ compared to bulk-Si: self-heating diminishes current enhancement

• Strained-Si material parameters for bandgap ($E_g$) and permittivity ($\varepsilon_r$) - reduced $E_g$ in S-Si and SiGe layers
Material Parameters in S-Si

- Bandgap ($E_g$) and permittivity ($\varepsilon_r$) parameters reduce $E_g$ in S-Si and SiGe layers
- Impact ionization characteristics of S-Si for high-current applications

\[
E_{g,SSi} = 1.08 - 0.4x \\
\varepsilon_{r,SSi} = 11.8
\]

\[
E_{g,SiGe} = 1.08 - 0.73x \\
\varepsilon_{r,SiGe} = 11.8 + 4.2x
\]
Impact Ionization

- Phonon mean-free path ($\lambda_n$) of S-Si is determined by energy relaxation time ($\tau_w$) based on Full-Band Monte Carlo (FBMC) device simulation.

\[ \alpha_{n,ii} = \alpha_{n,ii0} \exp\left[-\frac{E_g}{q\lambda_n E}\right] \]

- $E_{g,ssi} < E_{g,\text{Si}}$
- $\lambda_{n,ssi} > \lambda_{n,\text{Si}}$
- $\alpha_{n,ii}$ for S-Si $> \alpha_{n,ii}$ for bulk-Si
Electro-Thermal Simulation for S-Si

- Important for reliability problems - ESD and latchup
- Second-breakdown can be observed with thermal model and temperature dependent mobility

![Graph showing ID vs VD with and without thermal model.](Image)
High Current Operations

- Device simulation shows lower hold voltage ($V_h$) and higher 2nd breakdown current ($I_{t2}$) for strained-Si device due to its higher current gain and impact ionization rate.
Lattice Temperature

- Higher bipolar current gain ($\beta$) and uniform current conduction in high current operation for S-Si - ESD protection device.
Junction Capacitance in S-Si

- Drain-to-bulk junction capacitance ($C_{DB}$) in S-Si is larger than bulk-Si’s due to the increased $\varepsilon_{r,ssi}$ and $\varepsilon_{r,sige}$
- $\sim$10% increased junction capacitance and (K. Rim, ISSCC’01) in S-Si than bulk-Si
Junc. Capacitances for S- and bulk-Si

- Comparisons of MEDICI simulated junction capacitances between S-Si and bulk-Si
- 16% greater junction capacitance for S-Si at zero-bias

![Graph showing comparison of junction capacitances between strained-Si and bulk-Si](image)
Compact Junc. Capacitance Model

- Area capacitance ($C_{JA}$) with the built-in potential of SiGe
- Sidewall capacitance ($C_{JSW}$) considers both $C_{jsw,ssi}$ and $C_{jsw,sige}$ from two different materials

\[
C_{JA} = C_{JA0}(1+V_{DB}/\phi_{b,sige})^{-MJ}
\]

\[
C_{JSW} = C_{JSW,ssi}+C_{JSW,sige}
\]

\[
C_{JSW0} = \frac{C_{JSW0}}{t_{ssi}\varepsilon_{r,ssi}+t_{sige}\varepsilon_{r,sige}} \times \left[ t_{ssi}\varepsilon_{r,ssi}(1+V_{DB}/\phi_{b,ssi})^{-MJSW} + t_{sige}\varepsilon_{r,sige}(1+V_{DB}/\phi_{b,sige})^{-MJSW} \right]
\]

where $C_{JSW0}$ is zero-bias junction sidewall capacitance (F/cm)
Results of the Compact Junc. Cap. Model

• Comparisons between numerical (MEDICI) and compact junction capacitance model for different Ge-mole fractions

![Graph showing comparisons between numerical and compact models for Si$_{1-x}$Ge$_x$ with x=0.35]
Junction Leakage Current (Future Plan)

- ~X10 higher junction leakage current in S-Si than bulk-Si devices due to the narrower bandgap and defect density: enhanced band-to-band tunneling
- Compact junction leakage current model is necessary
Summary

- Stress relaxation effects due to STI can reduce the tensile stress and degrade device performance in small strained-Si device: **bad news!**

- S-Si can be a reliable ESD protection device due to its high bipolar current gain and uniform conduction: **good news!**

- Compact junction capacitance model for circuit simulation

- Compact junction leakage current model is also necessary