Technology Limits and Compact Model for SiGe Scaled FETs

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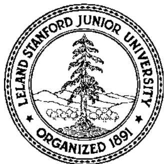
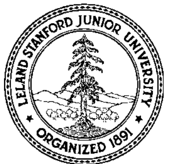


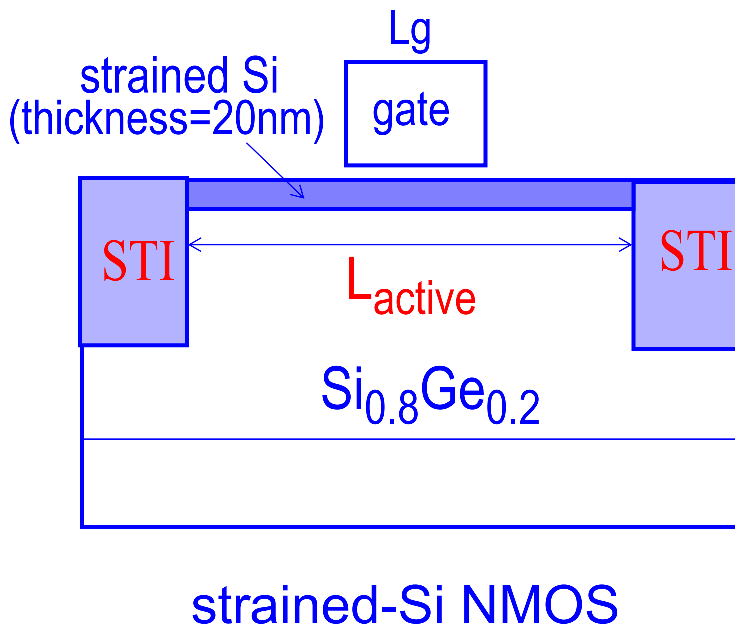
Outline

- Stress relaxation effects by Shallow-Trench Isolations (STI)
- High current operations of strained-Si MOS for Electro-Static Discharge (ESD)
- Compact junction capacitance model for circuit simulation

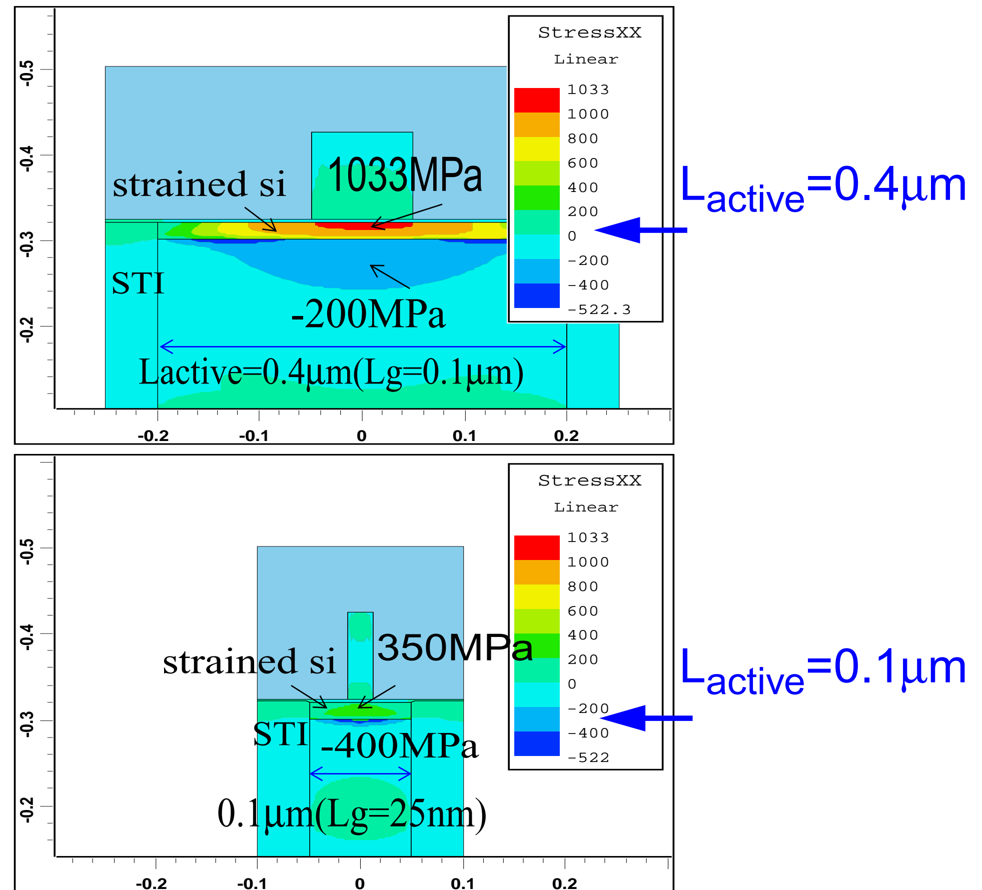


STI Effects on Strained-Si/SiGe

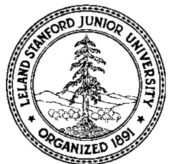
- Tensile stress in strained-Si increases electron mobility
- Impact of STI-induced compressive stress?



strained-Si NMOS

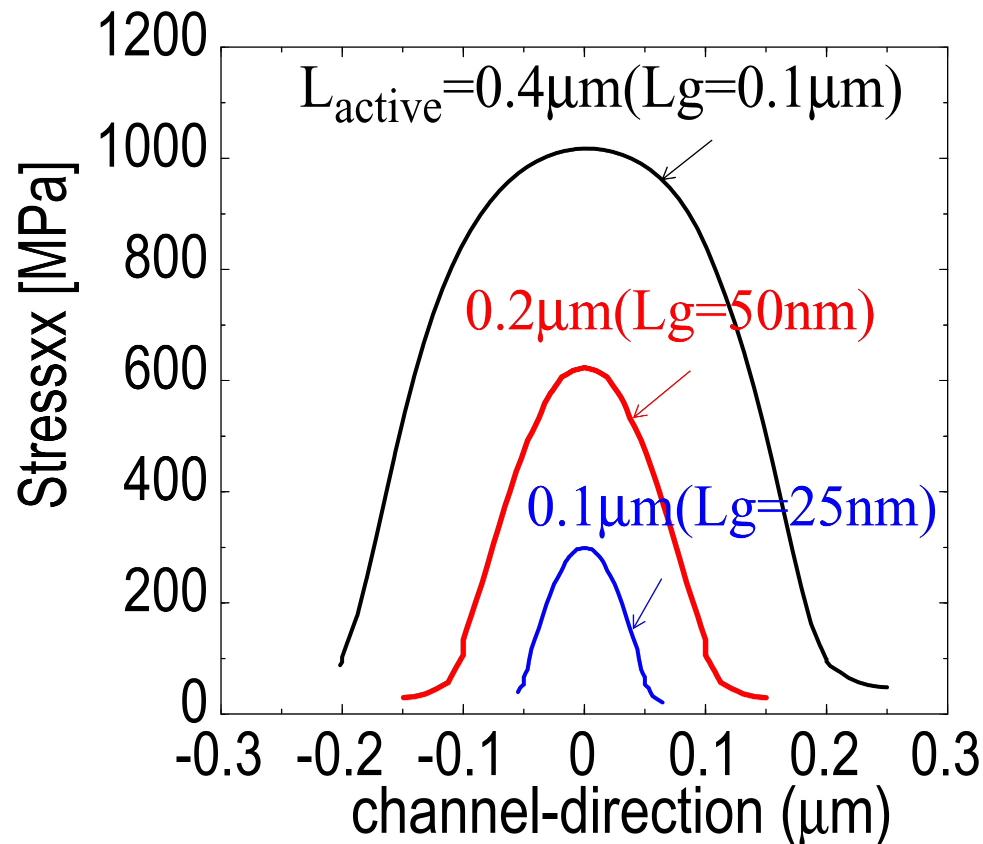


2D tensile stress contours



Stress Relaxation for Active Lengths

- Enhanced stress relaxation in strained-Si layers for shorter active lengths (L_{active}): strain is reduced by ~2/3 from L_{active}=0.4μm to 0.1μm

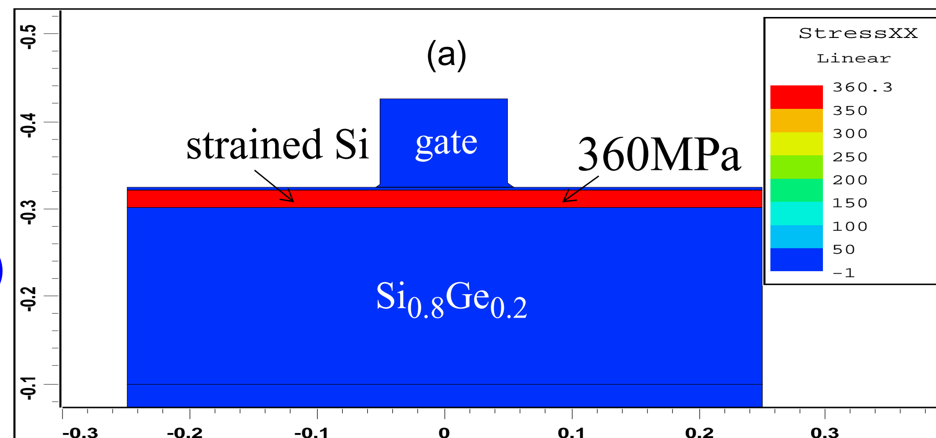


3D Stress Simulation

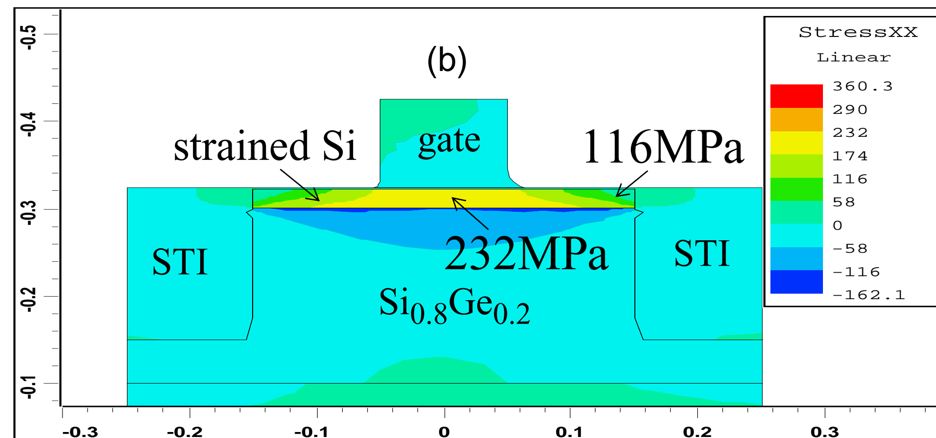
- 3D (bi-axial) stress simulation with STI process (L_{active}=0.3μm, W/L=0.7μm/0.1μm)

initial stress

(lattice mismatch strain)



after STI



3D Stress Simulation (Cont.)

- Stress contours (S_{xx}) for W/L=0.7μm/0.1μm

(a) poly-gate

(b) strained active, gate, STI, $Si_{0.8}Ge_{0.2}$

channel(x) direction

(c) gate, STI, $Si_{0.8}Ge_{0.2}$

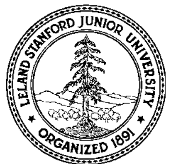
width (z) direction

(d) active, STI, W, Lg=0.1μm

top view

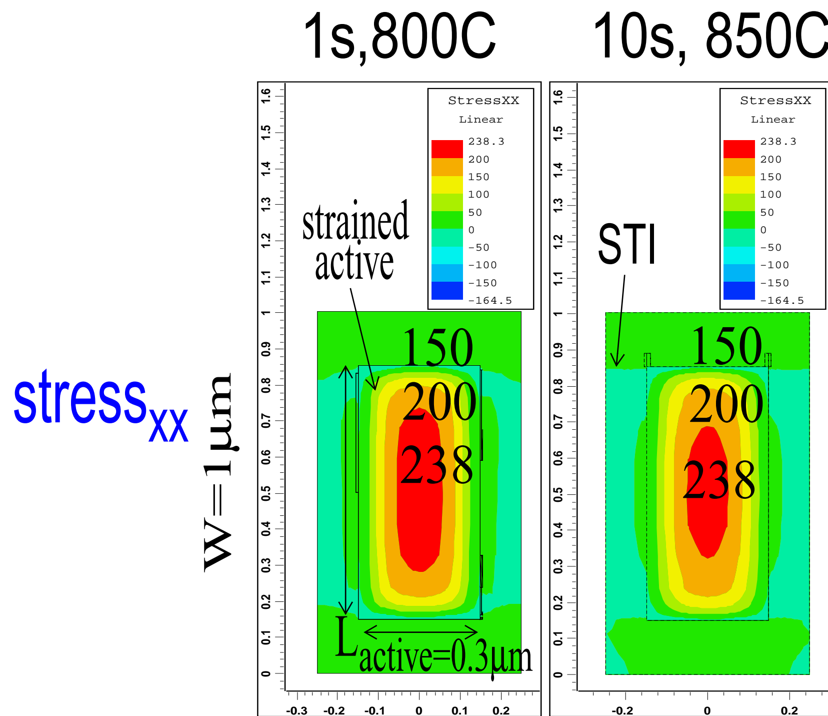
L_{active}=0.3μm

StressXX Linear: 239.4, 200, 150, 100, 50, 0, -50, -100, -150, -176.5

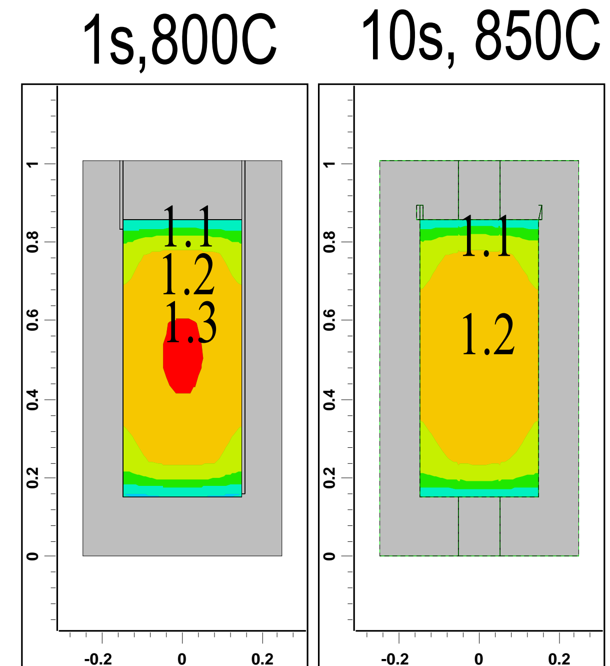


Mobility Degradation

- STI thermal process-dependent stress relaxation and mobility degradation: enhanced stress relaxation for high temperature thermal conditions



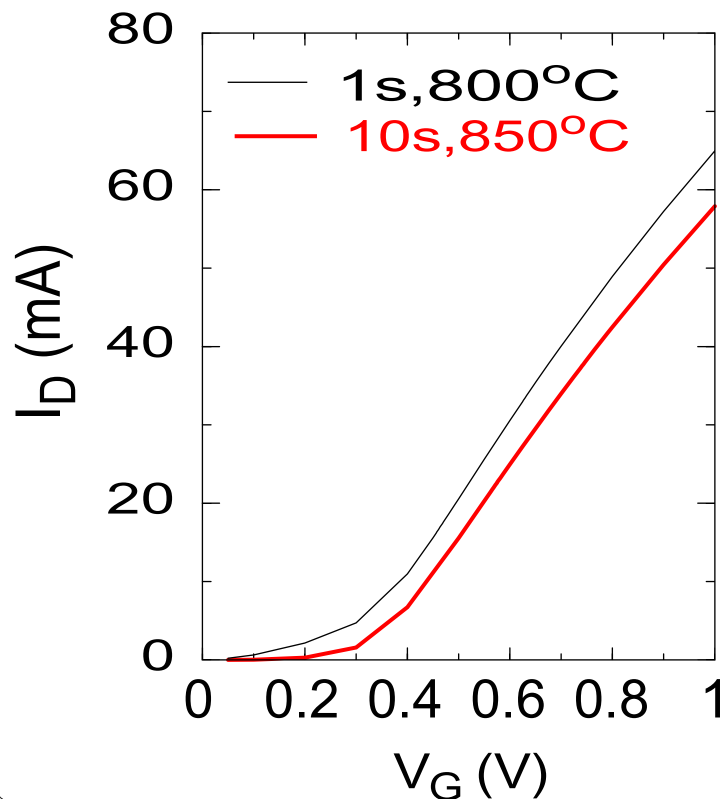
(a)

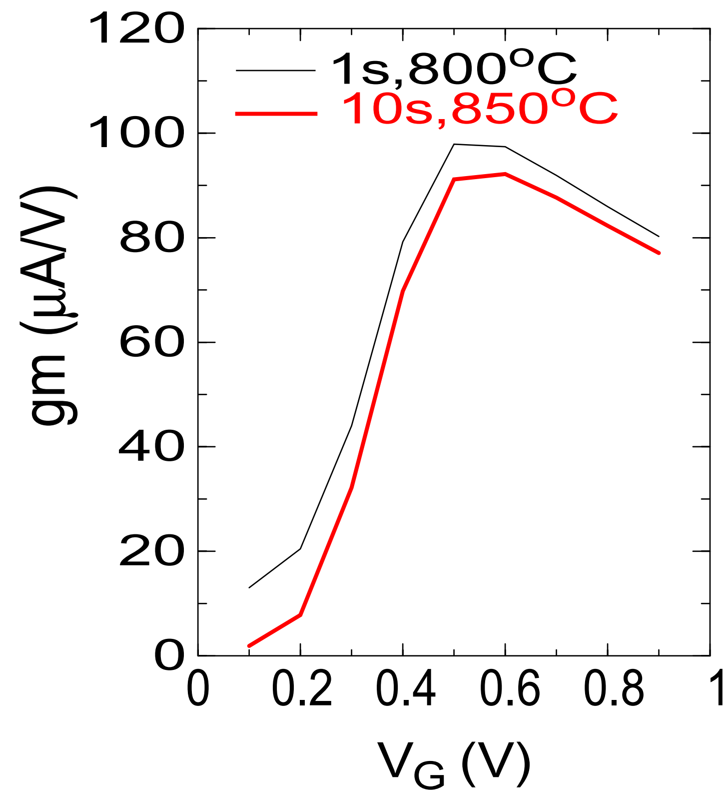


(b)

Mobility Degradation

- Enhanced mobility degradation for high temperature thermal condition from the stress-induced mobility model (Egley model) based on anisotropic band shift





STI Effects to Narrow Width Devices

- Severe stress relaxation for narrow width devices with small active width/length (i.e. SRAM cell transistor)

Sxx

W=0.2µm W=1.7µm

active STI

144

L_{active}=0.3um

W

230

200

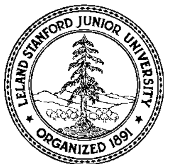
Szz

W=0.2µm W=1.7µm

750

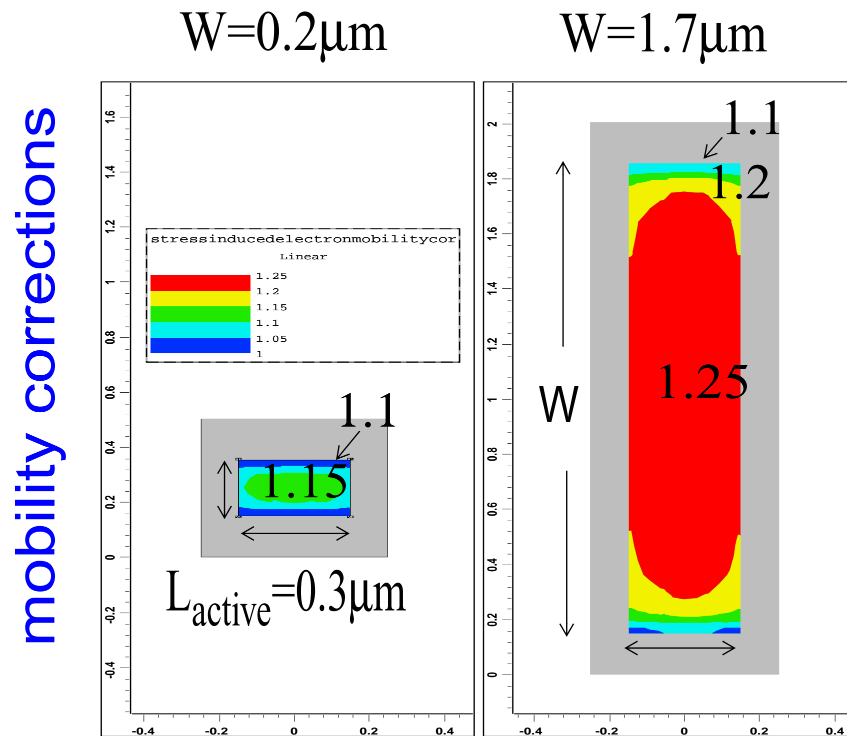
1250

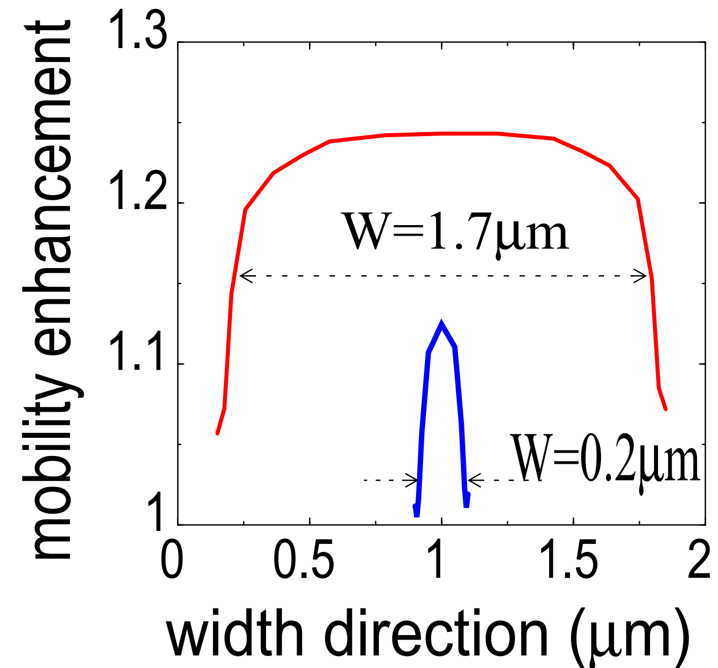
750



Stress Relaxation of Width Effects

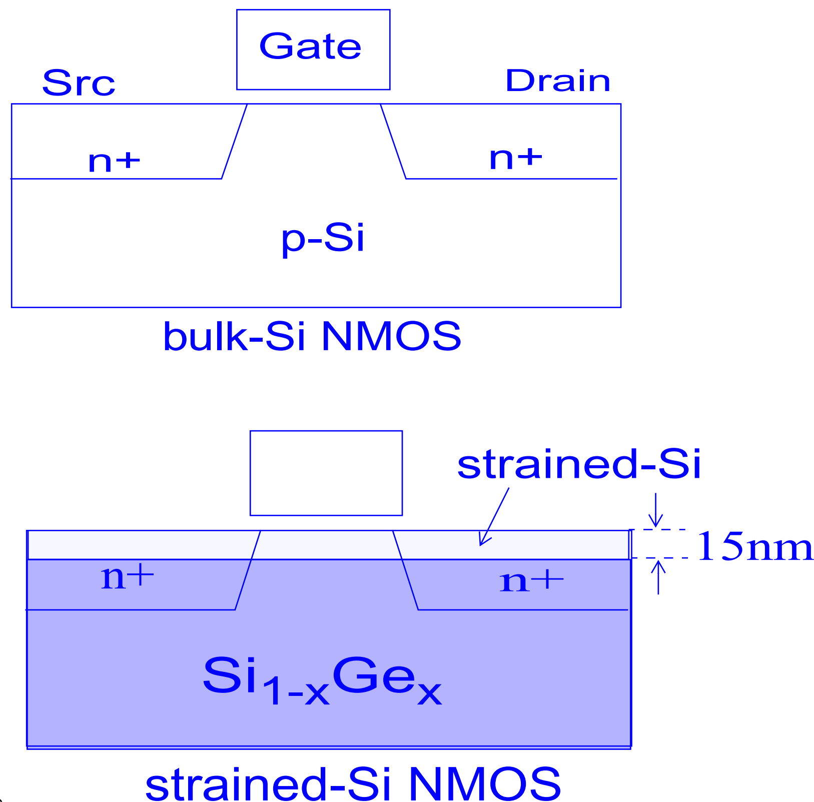
- Less mobility enhancement for narrow width devices- a possible limitation of S-Si device for beyond 25nm node

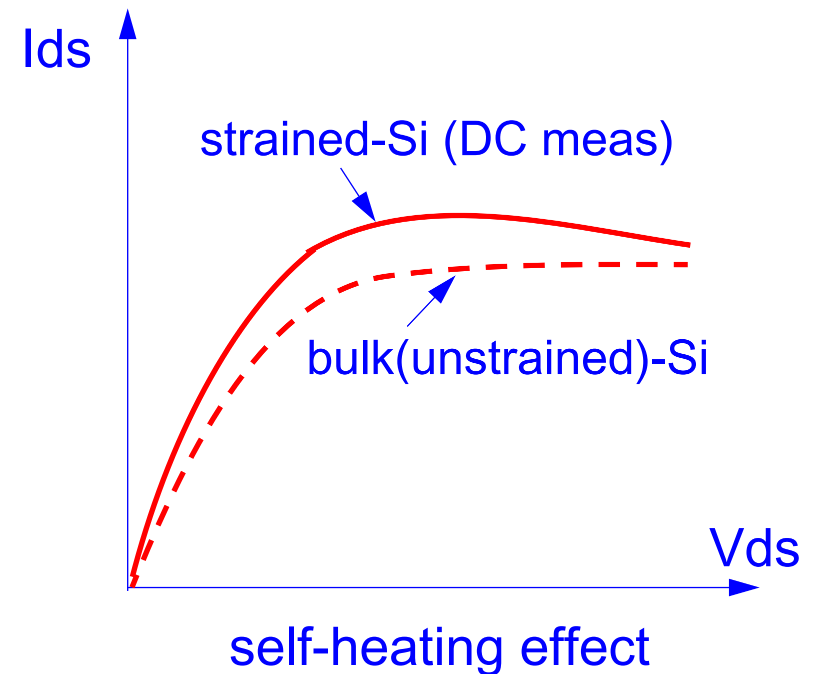




High-Current Operation in S-Si

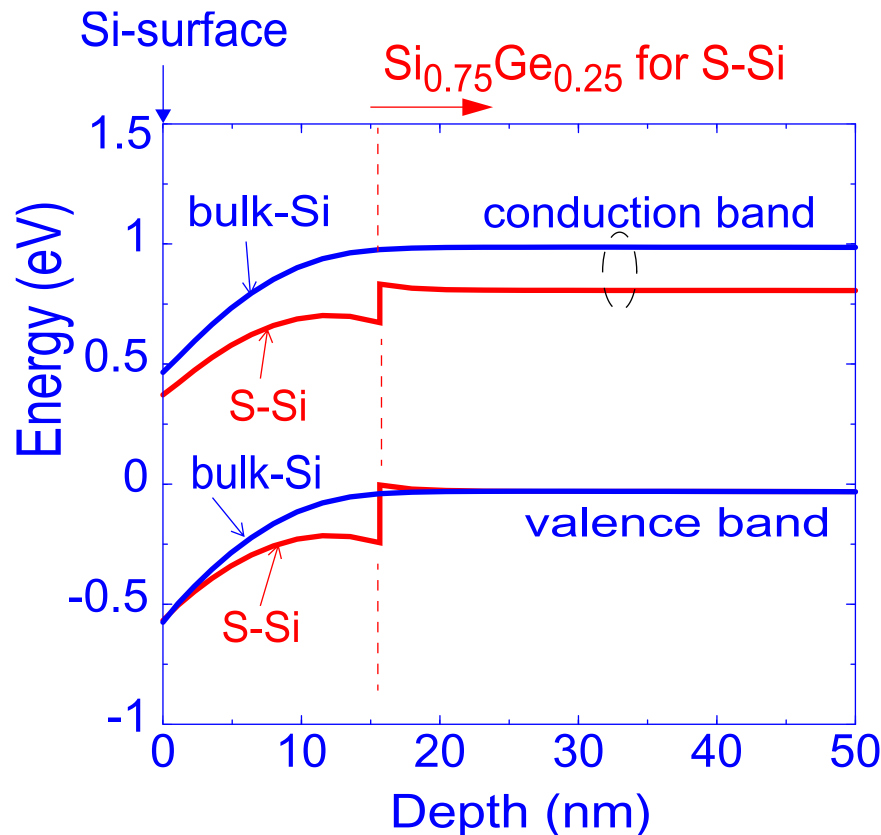
- x15 lower thermal conductivity of $Si_{0.8}Ge_{0.2}$ compared to bulk-Si : self-heating diminishes current enhancement
- Strained-Si material parameters for bandgap (E_g) and permittivity (ε_r) - reduced E_g in S-Si and SiGe layers





Material Parametersin S-Si

- Bandgap (E_g) and permittivity (ε_r) parameters reduce E_g in S-Si and SiGe layers
- Impact ionization characterisitcs of S-Si for high-current

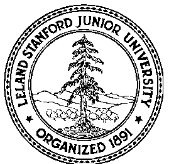


$E_{g,SSi}$=1.08-0.4x

$\varepsilon_{r,SSi}$=11.8

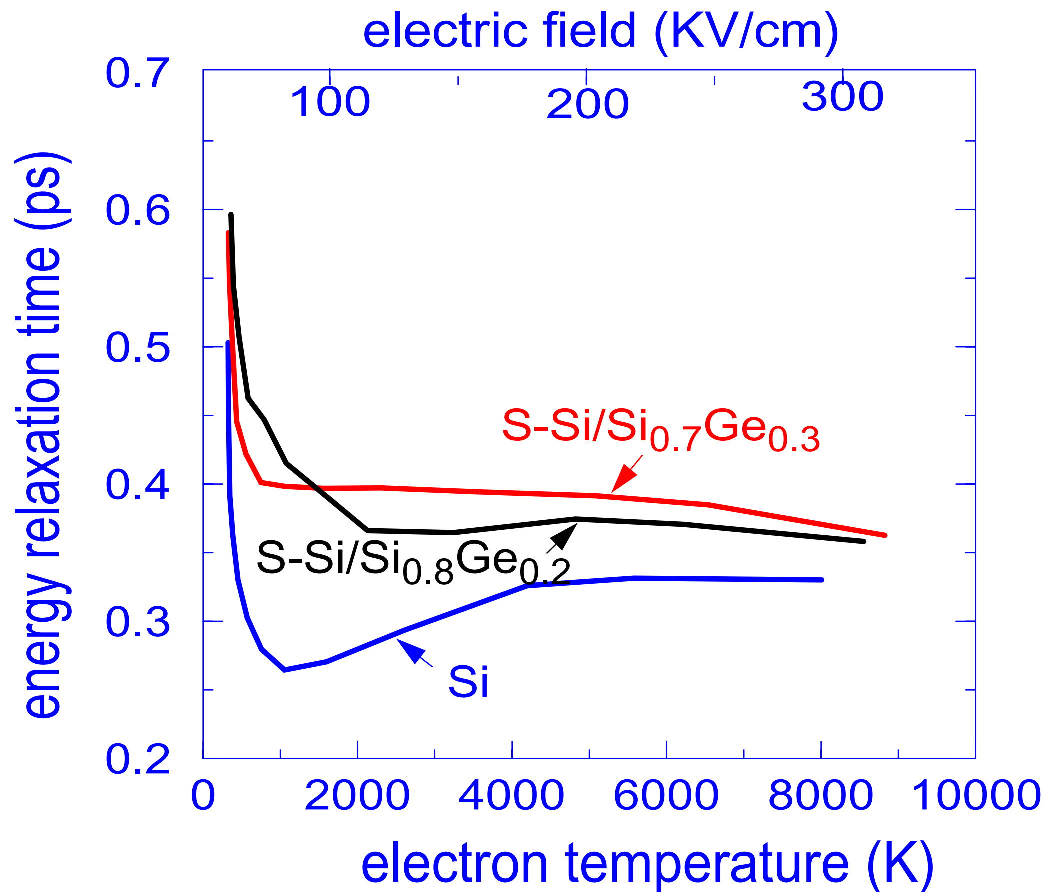
$E_{g,SiGe}$=1.08-0.73x

$\varepsilon_{r,SiGe}$=11.8+4.2x



Impact Ionization

- Phonon mean-free path (λ_n) of S-Si is determined by energy relaxation time (τ_w) based on Full-Band Monte Carlo (FBMC) device simulation



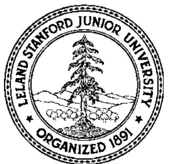
impact ionization rate

$\alpha_{n,ii}=\alpha_{n,ii0} \exp[-E_g/q\lambda_n E]$

$E_{g,ssi} < E_{g,Si}$

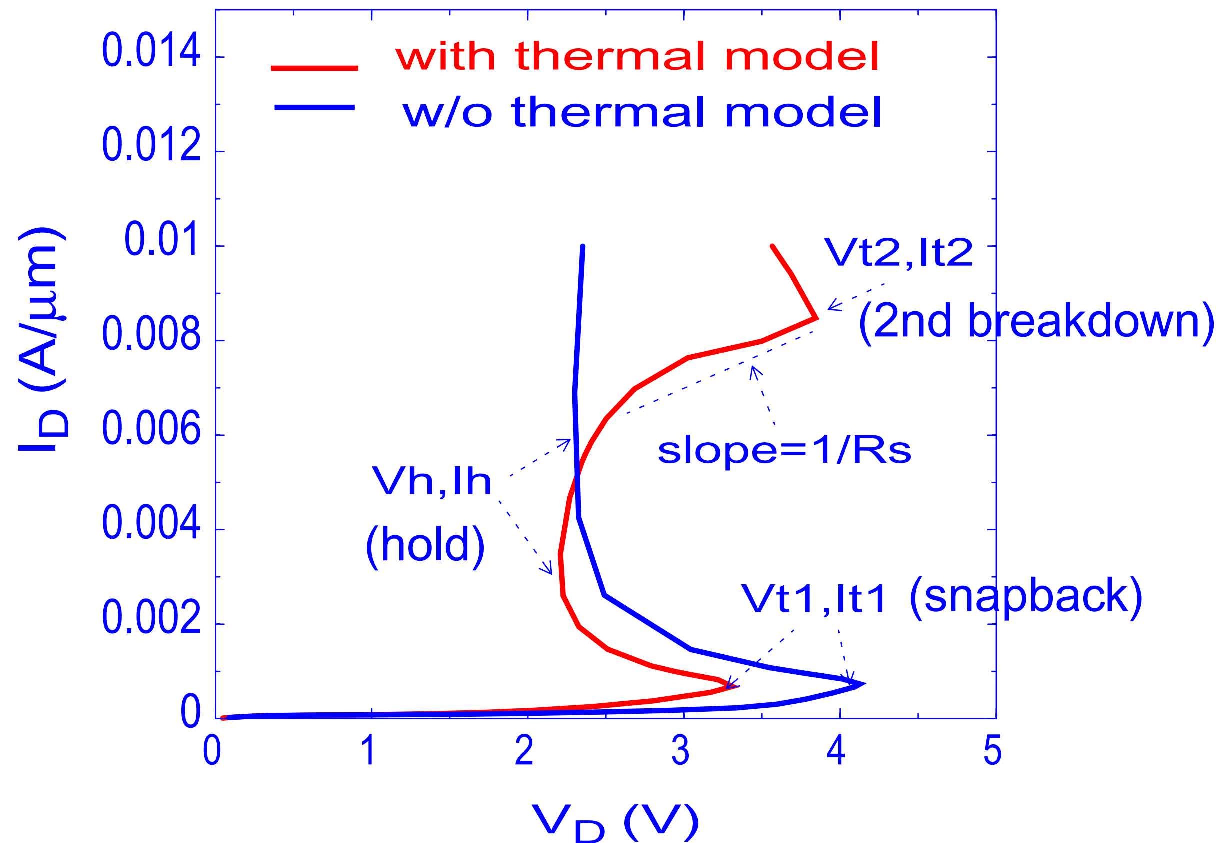
$\lambda_{n,ssi} > \lambda_{n,Si}$

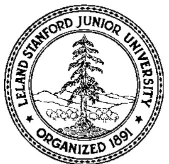
$\alpha_{n,ii}$ for S-Si > $\alpha_{n,ii}$ for bulk-Si



Electro-Thermal Simulation for S-Si

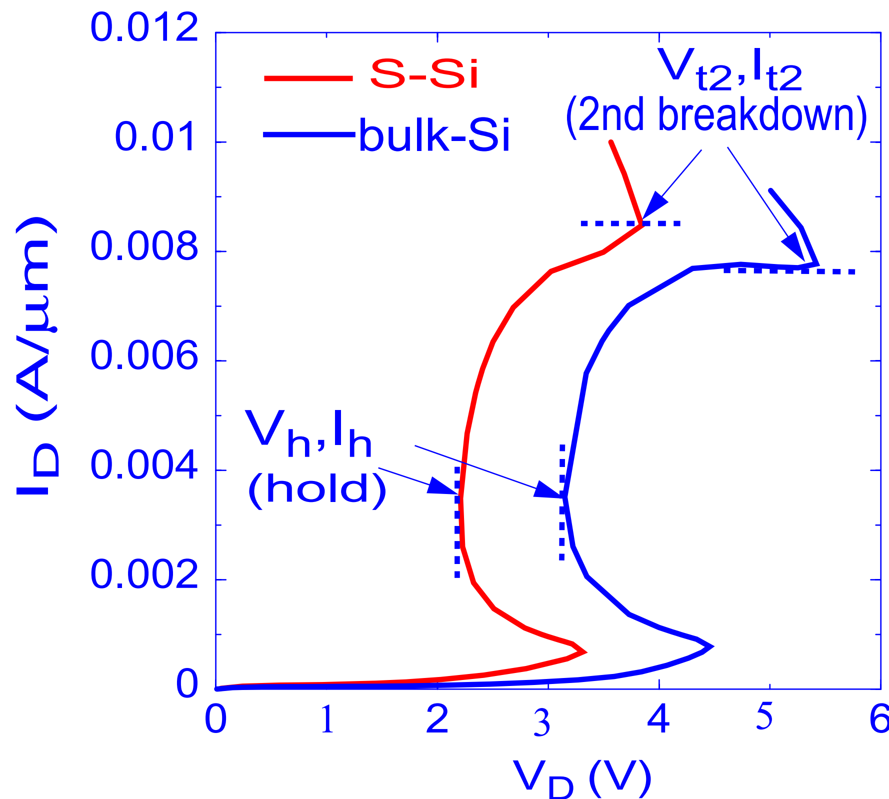
- Important for reliability problems- ESD and latchup
- Second-breakdown can be observed with thermal model and temperature dependent mobility

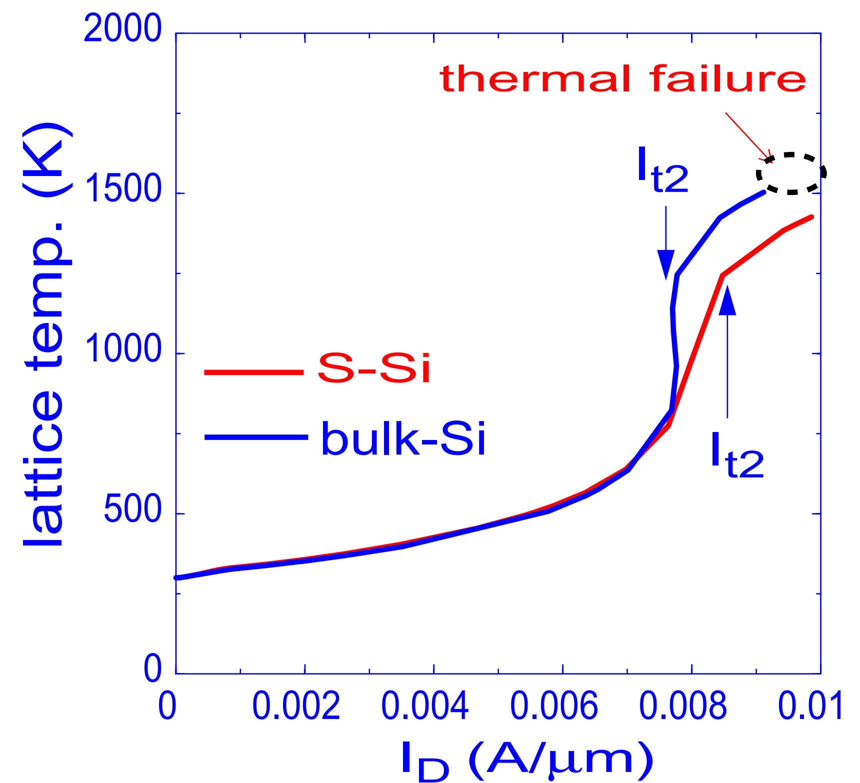




High Current Operations

- Device simulation shows lower hold voltage (V_h) and higher 2nd breakdown current (I_{t2}) for strained-Si device due to its higher current gain and impact ionization rate





Lattice Temperature

- Higher bipolar current gain (β) and uniform current conduction in high current operation for S-Si - ESD protection device

bulk-Si

S G D

T>1650K

300K

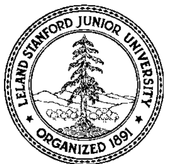
Lattice Tem
Linear
1800
1500
1300
1100
900
700
500
300

strained-Si

T=1500K

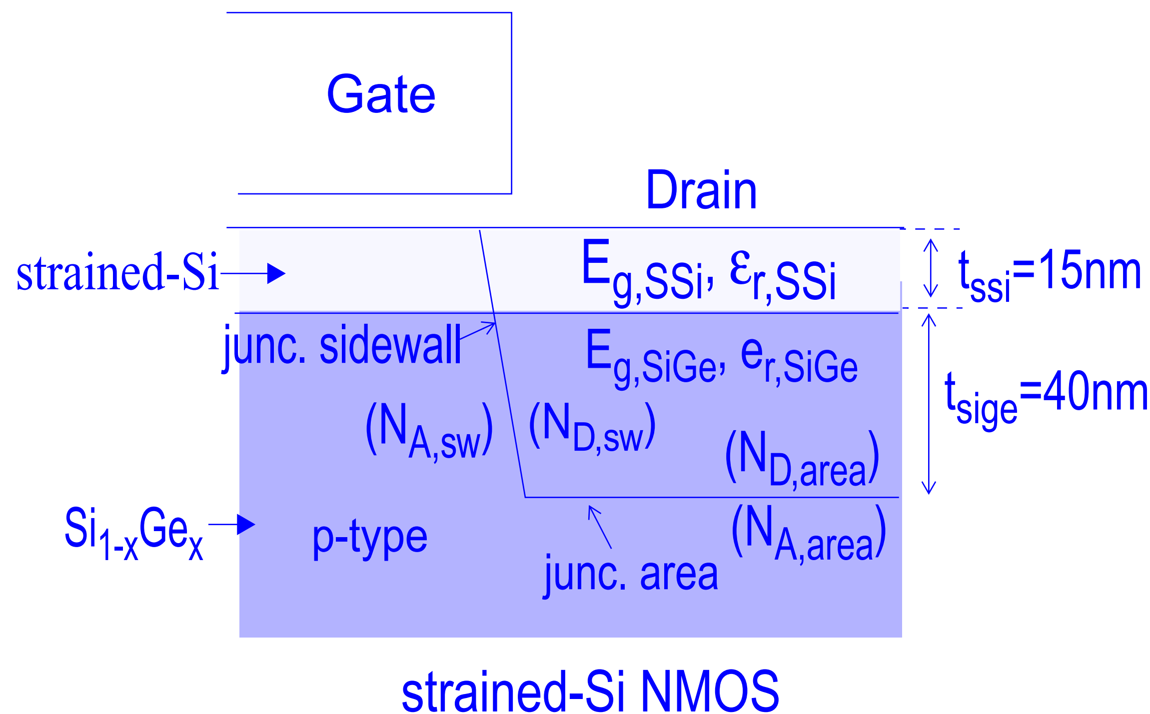
300K

Lattice Tem
Linear
1800
1500
1300
1100
900
700
500
300



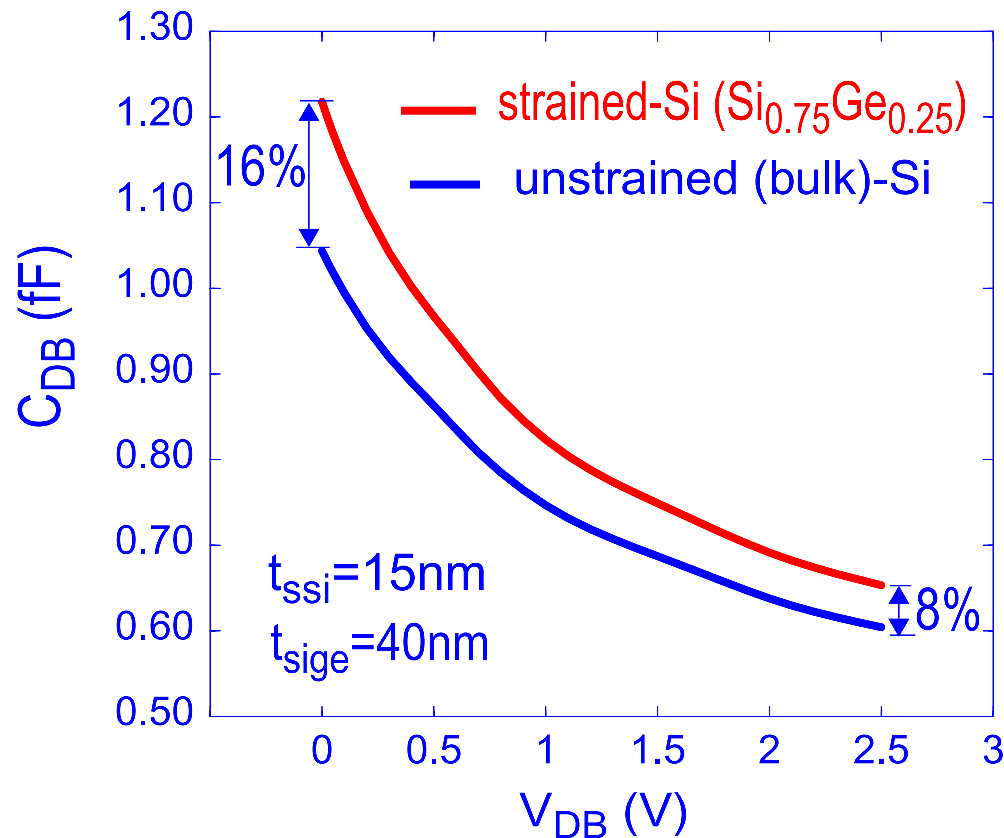
Junction Capacitance in S-Si

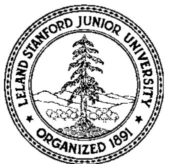
- Drain-to-bulk junction capacitance (C_{DB}) in S-Si is larger than bulk-Si's due to the increased $\varepsilon_{r,ssi}$ and $\varepsilon_{r,sige}$
- ~10% increased junction capacitance and (K. Rim, ISSCC'01) in S-Si than bulk-Si



Junc. Capacitances for S- and bulk-Si

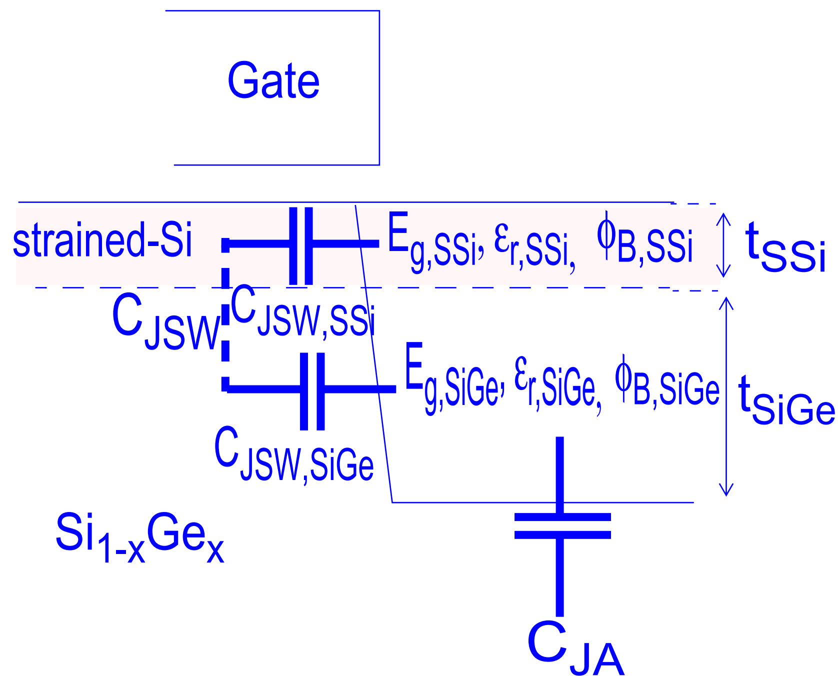
- Comparisons of MEDICI simulated junction capacitances between S-Si and bulk-Si
- 16% greater junction capacitance for S-Si at zero-bias





Compact Junc. Capacitance Model

- Area capacitance (C_{JA}) with the built-in potential of SiGe
- Sidewall capacitance (CJSW) considers both $C_{jsw,ssi}$ and $C_{jsw,sige}$ from two different materials



$$C_{JA} = C_{JA0}(1+V_{DB}/\phi_{b,sige})^{-MJ}$$

$$C_{JSW} = C_{JSW,ssi}+C_{JSW,sige}$$

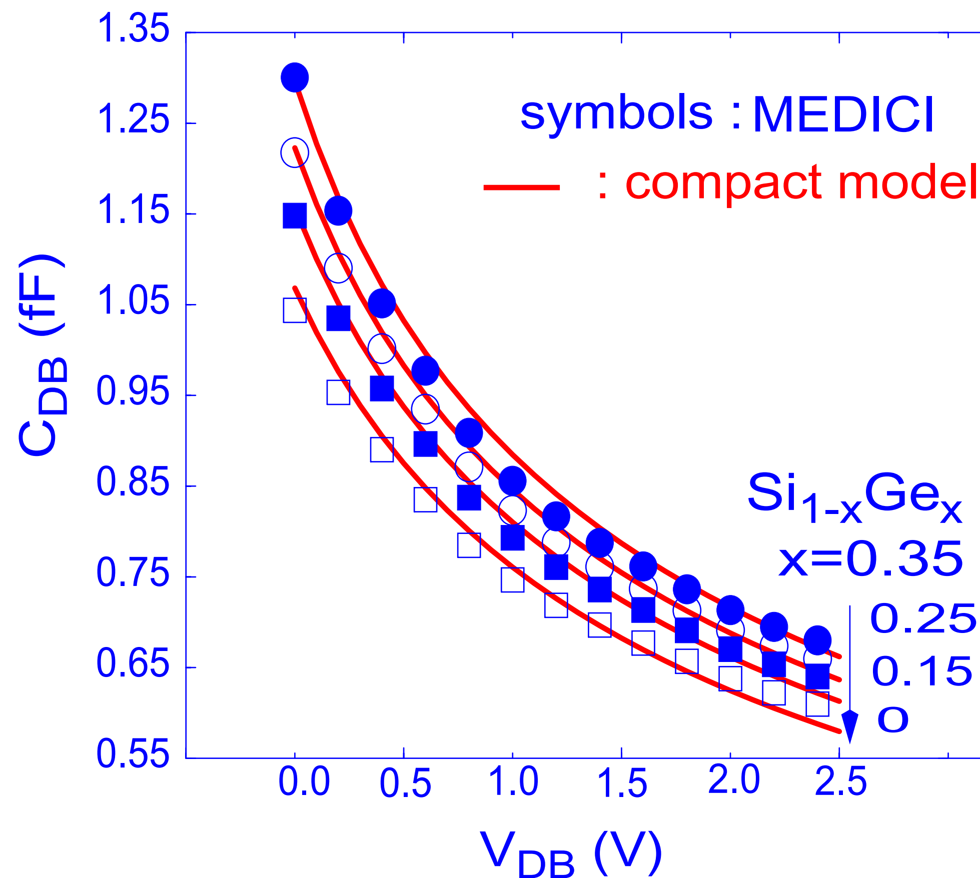
$$= \frac{C_{JSW0}}{t_{ssi}\varepsilon_{r,ssi}+t_{sige}\varepsilon_{r,sige}} \times$$

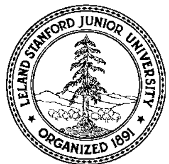
$$[\, t_{ssi}\varepsilon_{r,ssi}(1+V_{DB}/\phi_{b,ssi})^{-MJSW} + t_{sige}\varepsilon_{r,sige}(1+V_{DB}/\phi_{b,sige})^{-MJSW}]$$

where C_{JSW0} is zero-bias junction sidewall capacitance (F/cm)

Results of the Compact Junc. Cap. Model

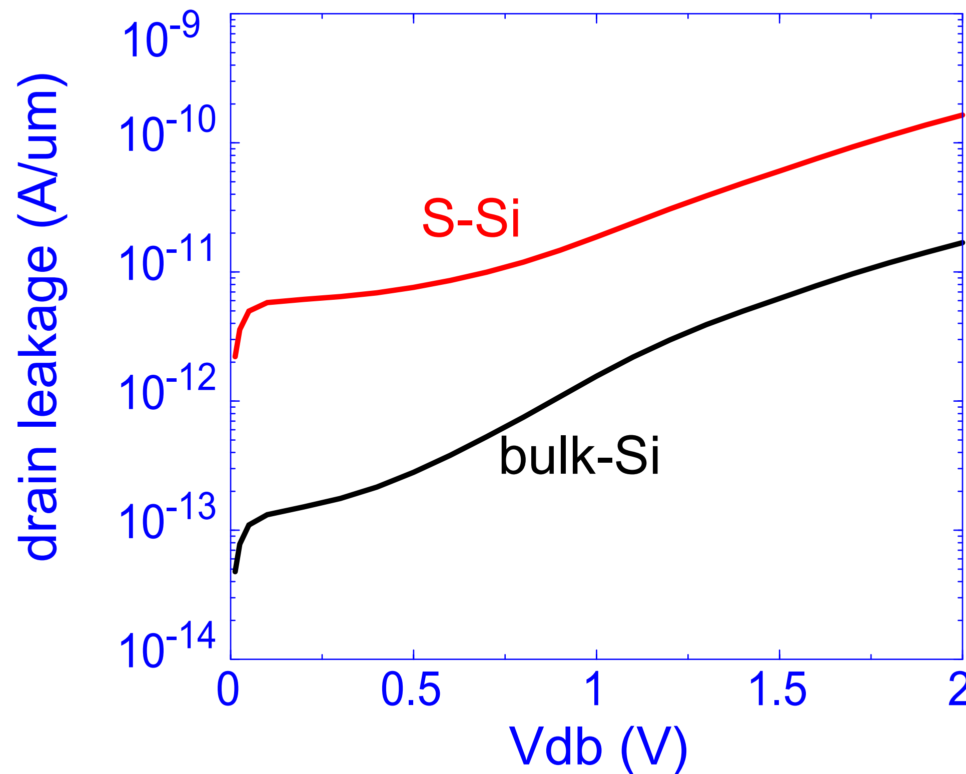
- Comparisons between numerical (MEDICI) and compact junction capacitance model for different Ge-mole fractions

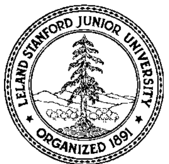




Junction Leakage Current (Future Plan)

- ~X10 higher junction leakage current in S-Si than bulk-Si devices due to the narrower bandgap and defect density: enhanced band-to-band tunneling
- Compact junction leakage current model is necessary





Summary

- Stress relaxation effects due to STI can reduce the tensile stress and degrade device performance in small strained-Si device: bad news!
- S-Si can be a reliable ESD protection device due to its high bipolar current gain and uniform conduction: good news!
- Compact junction capacitance model for circuit simulation
- Compact junction leakage current model is also necessary