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Geometry- and Bias-Dependence of Normalized Transconductances in Deep Submicron CMOS



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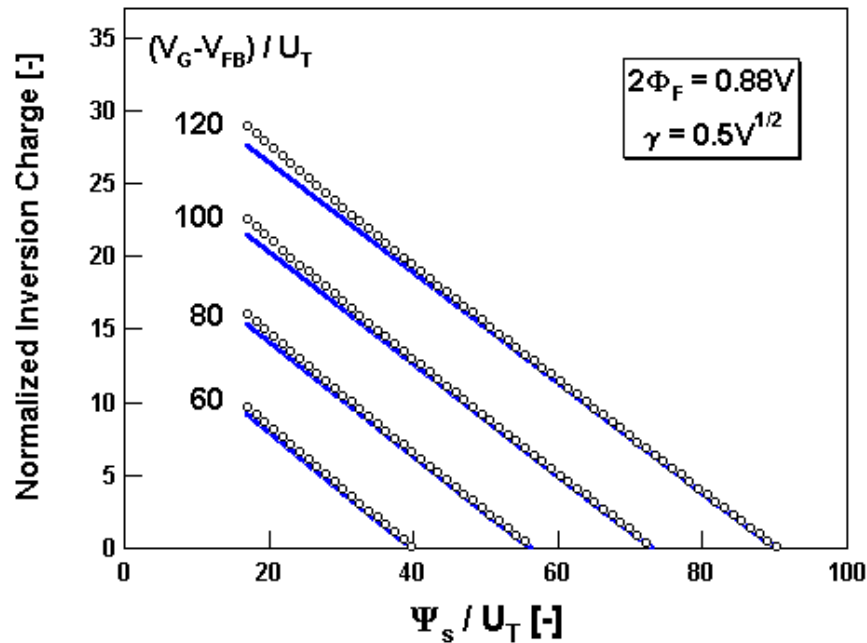
Outline

- Introduction
- EKV MOSFET Model Basics
- Normalized Transconductances Method
 - Analysis vs. level of inversion and channel length
- Examples using EKV3.0 MOSFET model with 0.25um, 0.13um CMOS
- Conclusions

Introduction

- Rapid evolution & increasing complexity of CMOS technology
- Moderate/weak inversion increasingly important.
 - Analog/mixed signal, wireless RF, LV-LP battery operated equipment requires novel circuit solutions.
- Need for efficient analog design methods
 - Rapid evaluation of design trade-offs:
gain, bandwidth, linearity, matching, noise, chip area.
 - Hand-calculation and full circuit simulation.
- Transconductance method based on EKV MOS transistor model:
 - Normalization of *current, voltage, transconductances,...*
 - Analysis of MOSFET vs. *level of inversion & channel length.*
 - EKV 3.0 MOSFET model for deep submicron CMOS.

MOSFET Basics -- Linearization of Q_i



Inversion Charge Linearization: $\frac{dQ_i'}{C_{ox}} \cong n \cdot d\Psi_S$

Pinch-off Surface Potential: $\Psi_{SP} \equiv \Psi_S|_{Q_i=0}$

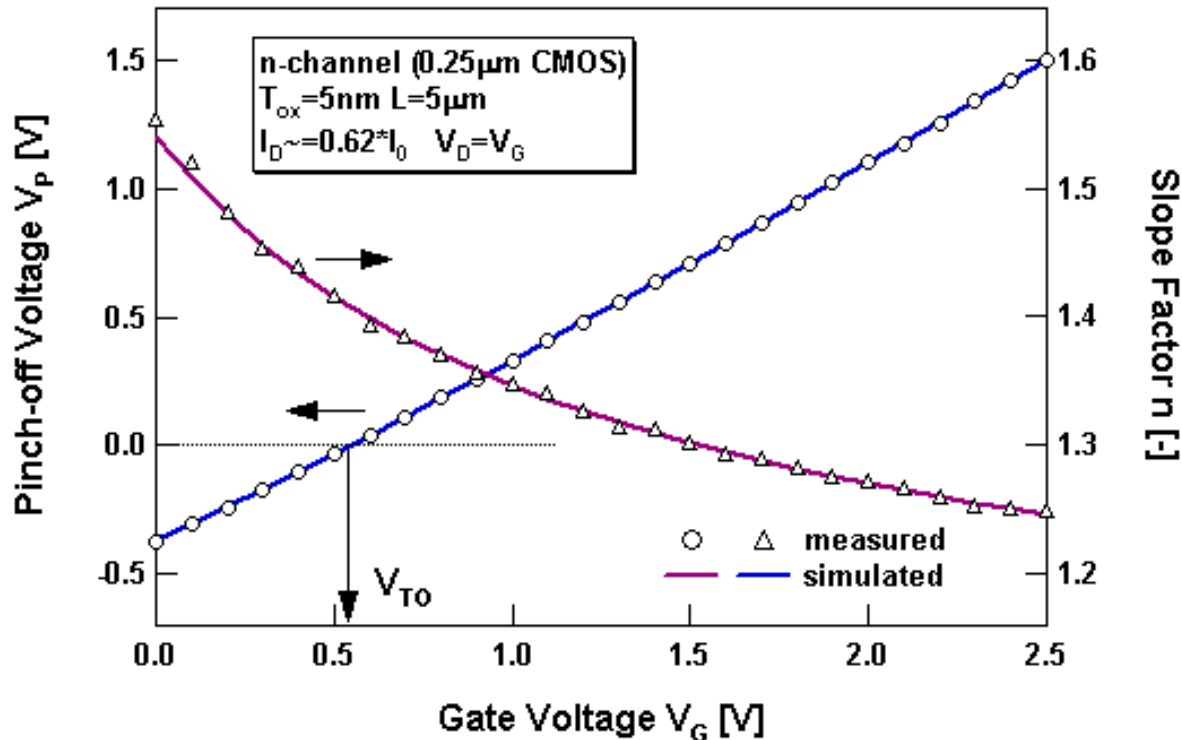
Pinch-off Voltage: $V_P \equiv \Psi_{SP} - \phi$

- Consider charge and voltage balance:

$$-\frac{Q_i'}{C_{ox}} = \gamma \sqrt{U_T} \cdot \left[\sqrt{\frac{\Psi_S}{U_T}} + \exp\left[\frac{\Psi_S - 2\phi_F - V_{ch}}{U_T}\right] - \sqrt{\frac{\Psi_S}{U_T}} \right] \quad V_G = V_{FB} + \Psi_S + \gamma \sqrt{\Psi_S} - \frac{Q_i'}{C_{ox}}$$

- Q_i' is almost linear w.r.t. surface potential Ψ_S at fixed V_G .
- Linearization is essential to analytic charge-sheet model.

Pinch-off Voltage, Slope Factor



Slope Factor:

$$n \cong \frac{\partial V_G}{\partial V_P} = 1 + \frac{\gamma}{2\sqrt{\phi + V_P}}$$

Pinch-off Voltage:

$$V_P \cong \frac{V_G - V_{TO}}{n}$$

$$V_{TO} = V_{FB} + \phi + \gamma\sqrt{\phi}$$

$$\gamma = \frac{\sqrt{2q\epsilon_{si}N_{sub}}}{C'_{ox}} \quad C'_{ox} = \frac{\epsilon_{ox}}{T_{ox}}$$

$$\phi \cong 2\phi_F + m \cdot U_T = U_T \cdot \left[2\ln\left(\frac{N_{sub}}{n_i}\right) + m \right]$$

- V_P , n account for the substrate effect
- T_{ox} , N_{sub} , V_{FB} , same parameters as in surface potential model

Charge Sheet Model

- Consider drift and diffusion current transport, use linearization:

$$I_D \cdot dx = \mu W [-Q'_i \cdot d\Psi_S + U_T \cdot dQ'_i] = \mu W \left[\frac{-Q'_i}{nC'_{ox}} + U_T \right] \cdot dQ'_i$$

- Integrate from source to drain: $I_D = 2nU_T^2 \cdot \mu C'_{ox} \frac{W}{L} \cdot (i_f - i_r)$

- with current-charge relationships: $i_{f(r)} = q_{f(r)}^2 + q_{f(r)}$ or, $q_{f(r)} = \sqrt{1/4 + i_{f(r)}}$

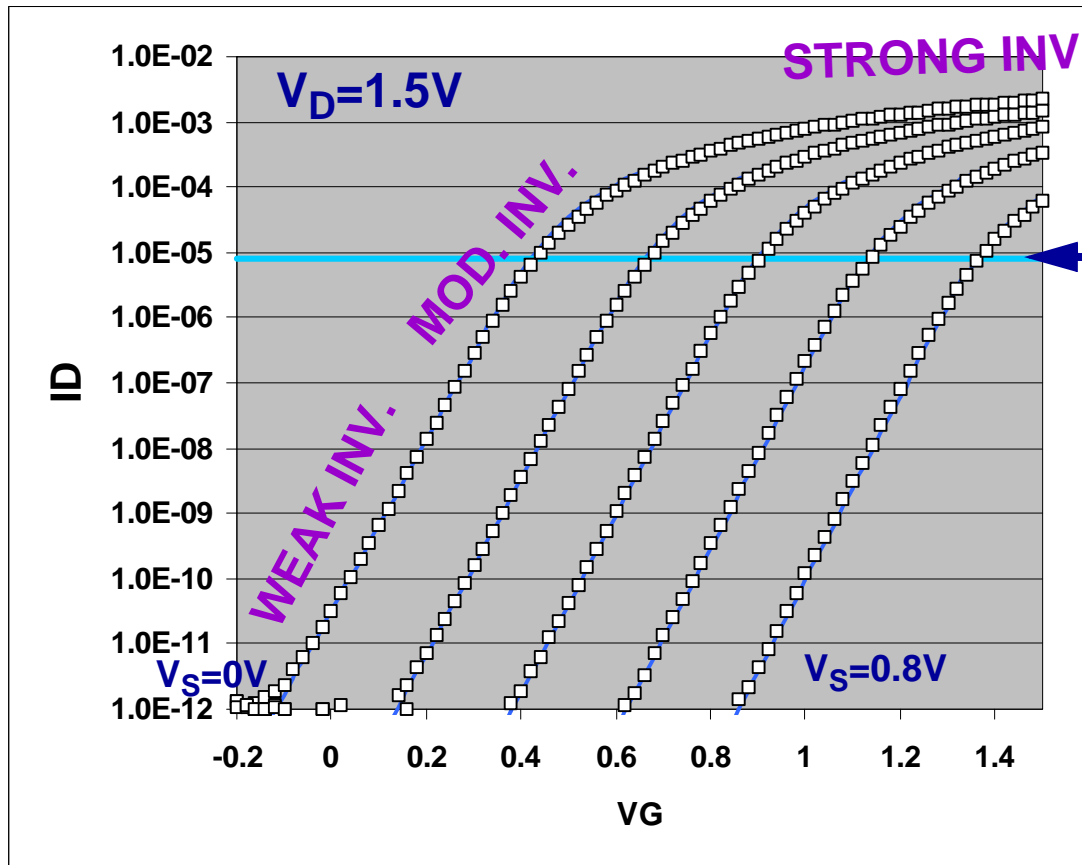
- Consider channel conductance: $\frac{dI_D}{dV_{ch}} = \mu \cdot \frac{W}{L} \cdot (-Q'_i)$

- ... in normalized form: $\frac{di_{f(r)}}{dV_{S(D)}} = q_{f(r)} = \sqrt{\frac{1}{4} + i_{f(r)}} = i_{f(r)} \cdot G(i_{f(r)})$

- Integration yields Voltage-Charge relationship:

$$V_P - V_{S(D)} = 2q_{f(r)} + \ln(q_{f(r)})$$

Normalization of Drain Current and Voltages



Inversion Coefficient:

$$IC = I_D / I_{Spec}$$

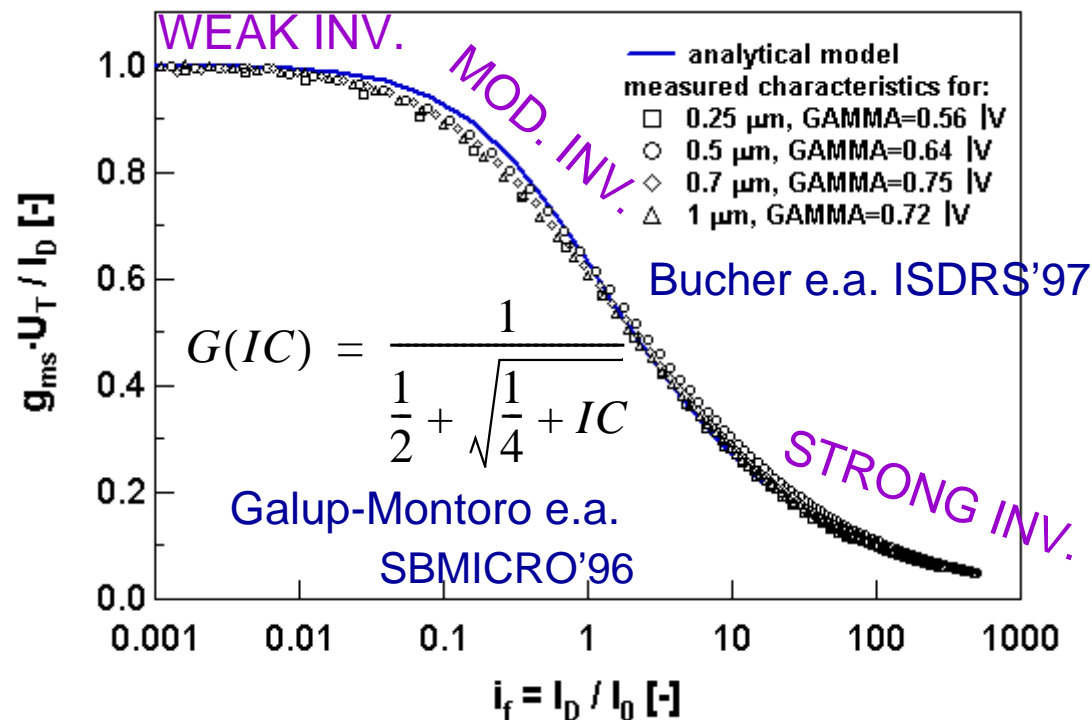
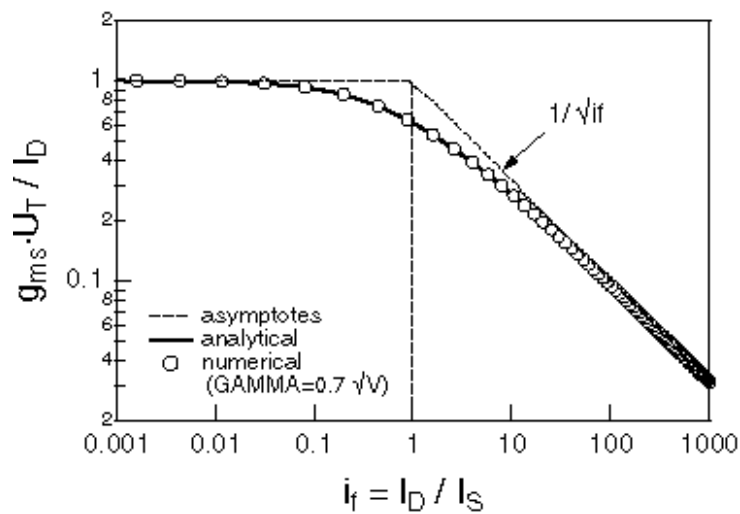
Specific Current:

$$I_{Spec} = I_0 \cdot \frac{W}{L}$$

$$= 2nU_T^2 \mu C'_{ox} \cdot \frac{W}{L}$$

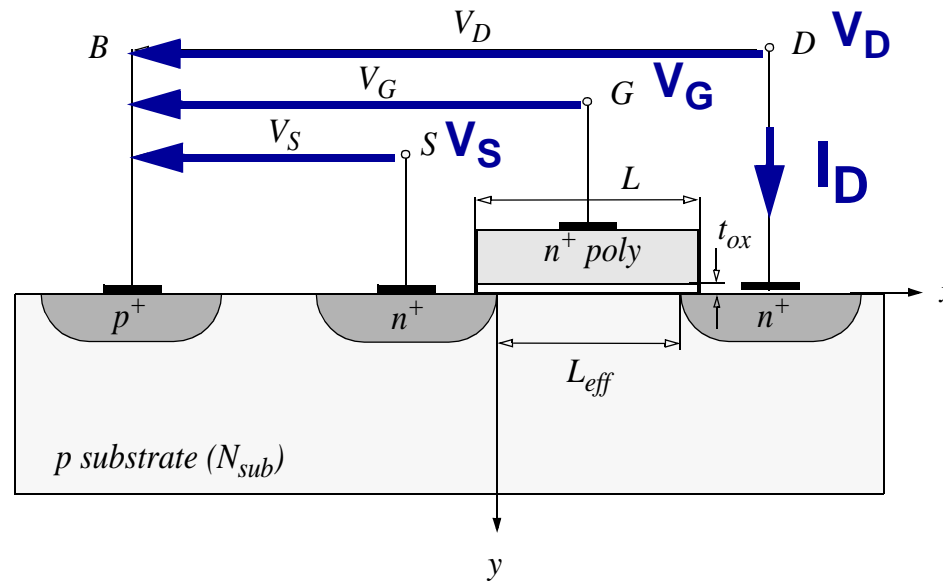
- Inversion Coefficient (IC) is meaningful for operation in *saturation*
 - ... covering all the range from weak to strong inversion
- Normalization of voltages by $U_T = kT/q$: $v_{G(S,D)} = V_{G(S,D)} / U_T$.

Transconductance-to-Current Ratio



- $G(IC)$: normalized transconductance-to-current ratio:
 - compared to exact surface potential model
- $G(IC)$ vs. IC is a *universal* characteristic of the MOSFET
 - ... independent of bias (saturation), Temp., technology (long-channel).

MOS Transistor Transconductances



- Source-, gate-, drain- and substrate transconductances:

$$g_{ms} \equiv - \left. \frac{\partial I_D}{\partial V_S} \right|_{V_G, V_D} \quad g_{mg} \equiv \left. \frac{\partial I_D}{\partial V_G} \right|_{V_S, V_D} \quad g_{md} \equiv \left. \frac{\partial I_D}{\partial V_D} \right|_{V_G, V_S}$$

$$g_{mb} = g_{ms} - g_{mg} - g_{md}$$

Transconductances Analysis

■ Fundamental relationships: $g_{mg} = \frac{g_{ms} - g_{md}}{n}$ $g_{mb} = \frac{n-1}{n} g_{mg}$

■ Transconductance-to-current ratios: $G_x \equiv \frac{g_{mx} \cdot U_T}{I_D}$

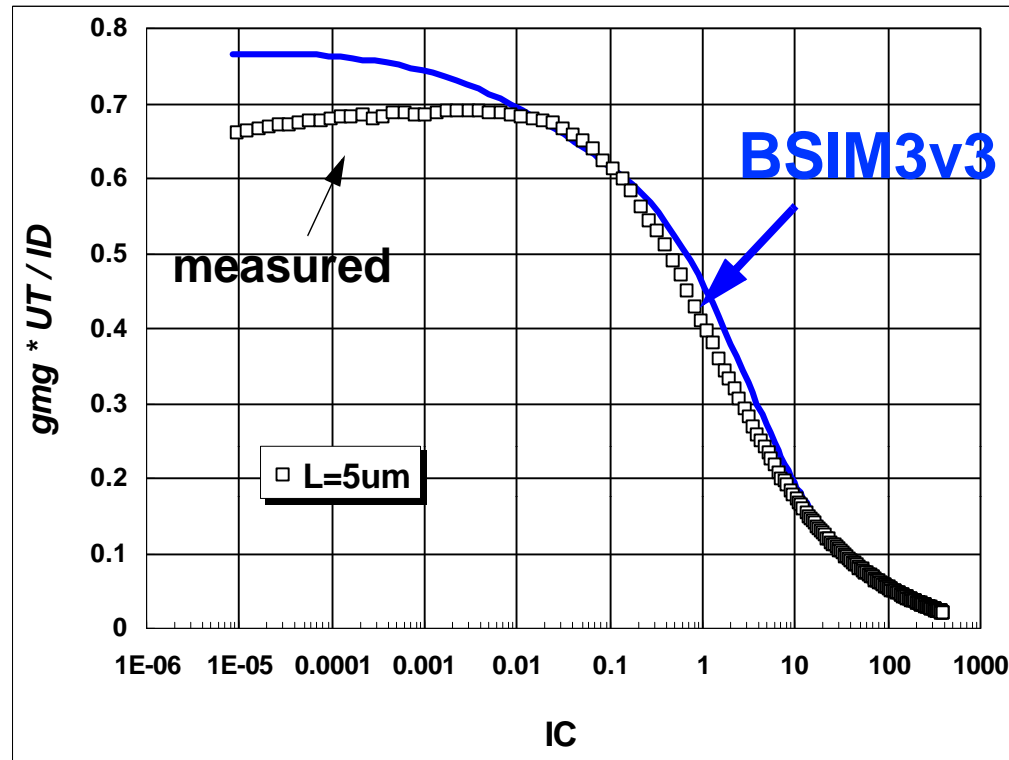
■ 1st-order expressions of transconductance-to-current ratios:

$$G_G \cong \frac{G(IC)}{n} \quad G_S \cong G(IC) \quad G_G \cong \frac{n-1}{n} G(IC)$$

$$G_D \cong G(IC) \cdot \frac{\partial V_P}{\partial V_D} + \frac{U_T}{n} \cdot \frac{\partial n}{\partial V_D}$$

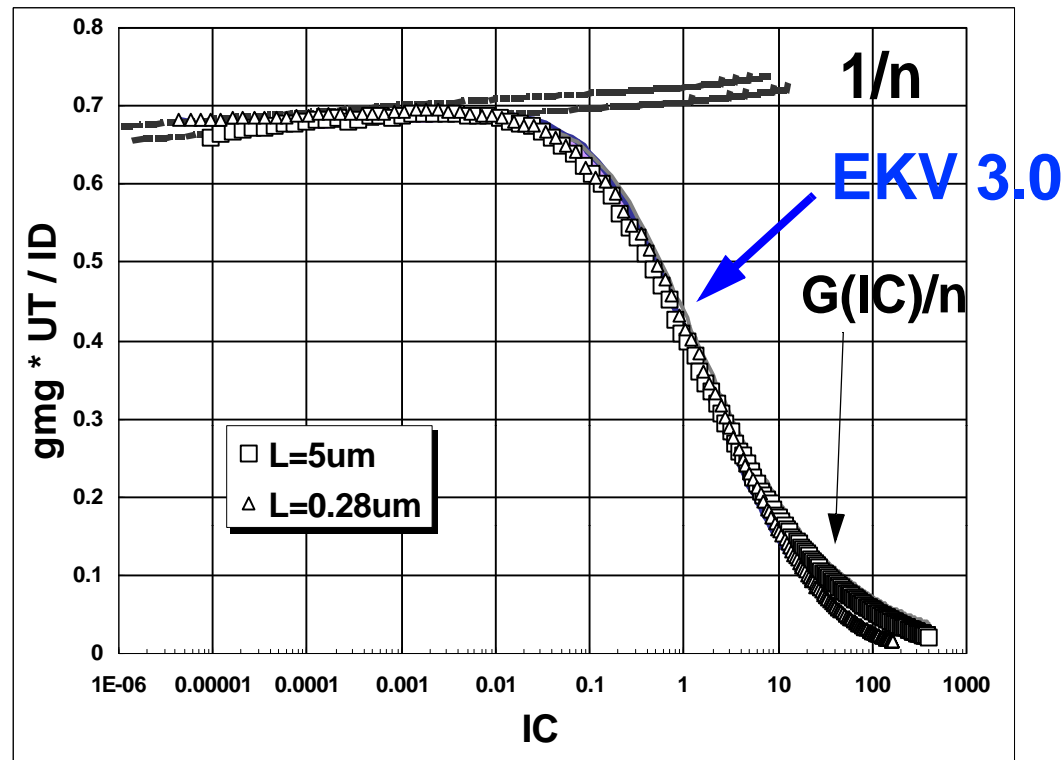
- 1st-order expressions are valid mostly in moderate & weak inversion.
- G_D is also directly dependent on $G(IC)$ and short-channel effects in V_P , n

Gate Transconductance



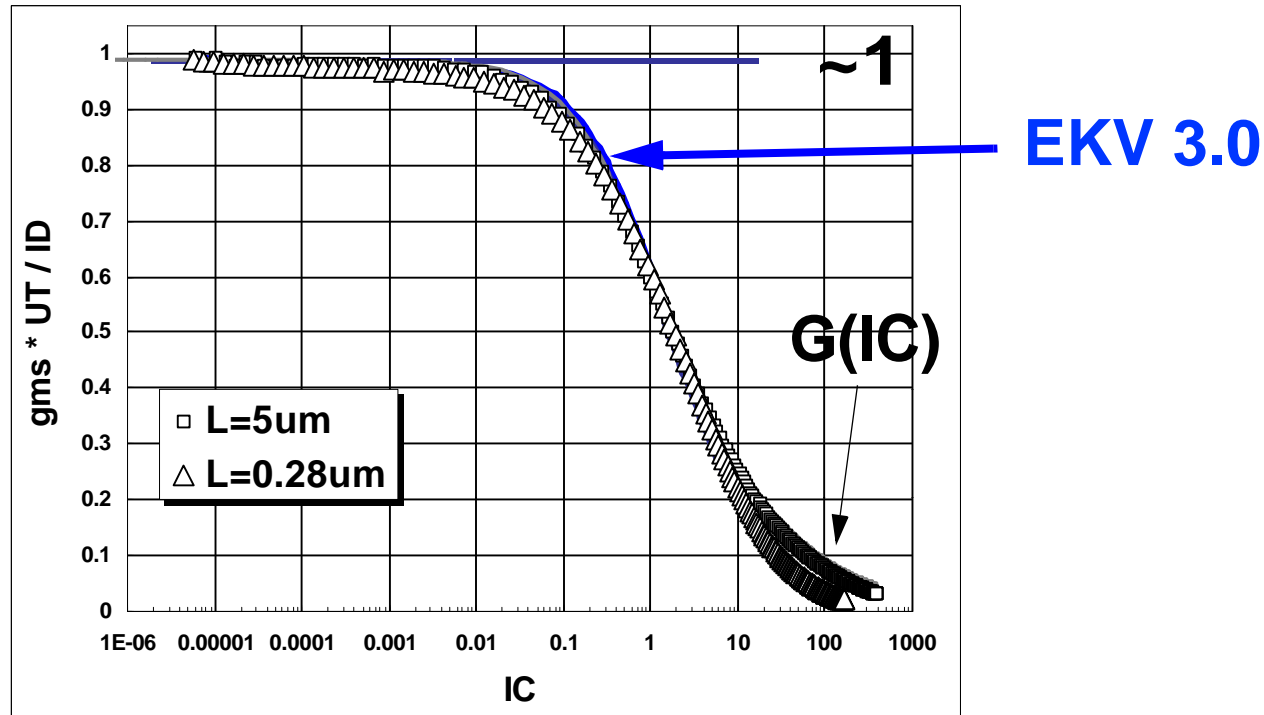
- $g_m \cdot U_T / I_D$ vs. I_D / I_{spec}
 - BSIM3v3 cannot fit a large range in moderate/weak inversion (parameter extraction dependent; but the problem is structural).
- measured at $V_S=0$, $V_D=V_G$ (saturation).

Gate Transconductance



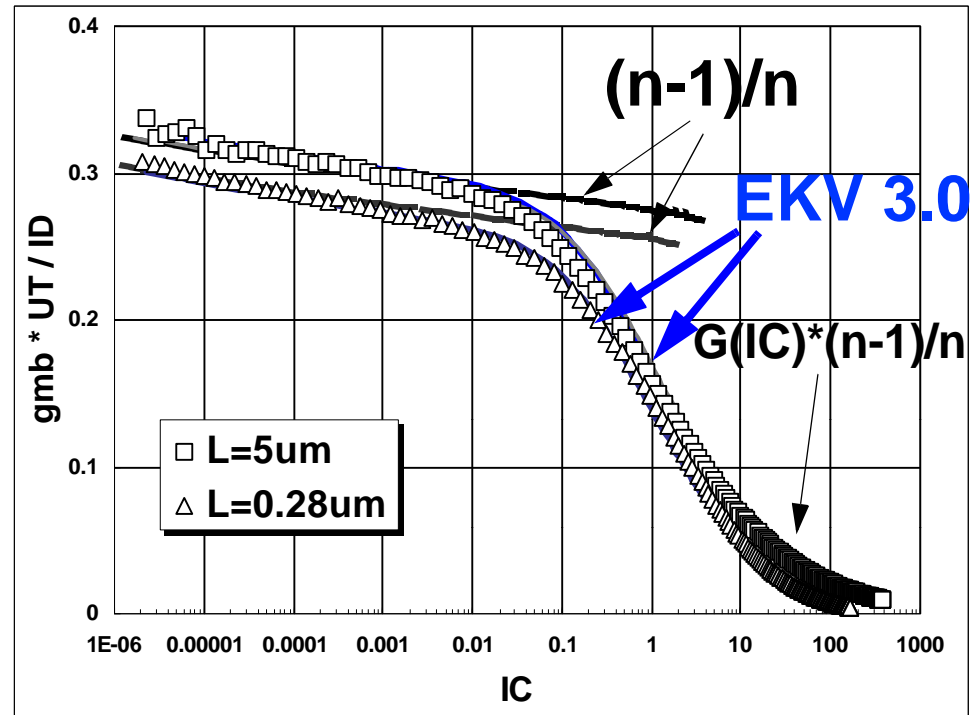
- EKV 3.0 fit from weak to strong inversion, for long & short-channel devices (NMOS)
 - Asymptote in weak inversion: $1/n$
- Weak inversion slope ($S \sim \ln 10 \cdot n \cdot U_T$) is dependent on I_C .

Source Transconductance



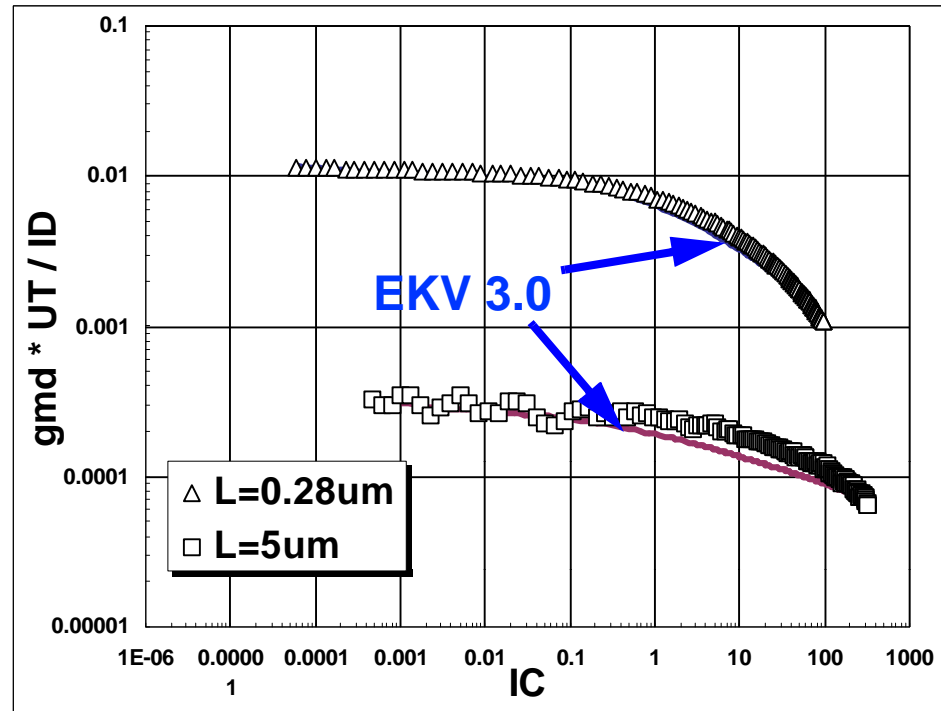
- $g_{ms} * U_T / I_D$ vs. I_C is universal
 - indep. of: V_G , Temp., W , L (except very short transistors)
 - Asymptote in weak inversion: ~ 1
- $g_{mg} \approx g_{ms} / n$ (saturation)

Substrate Transconductance



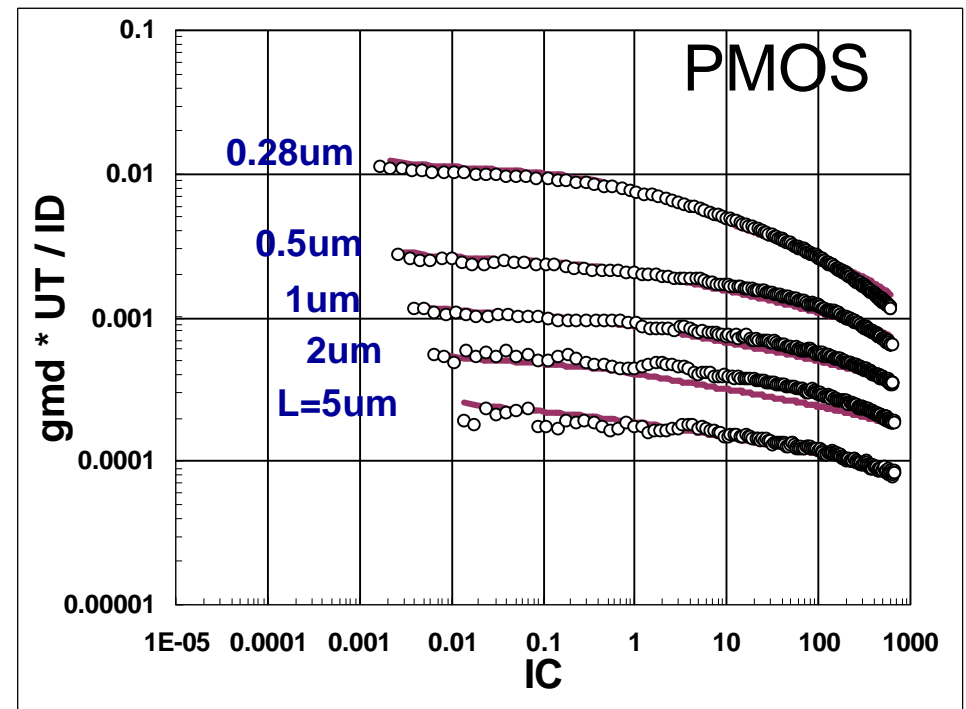
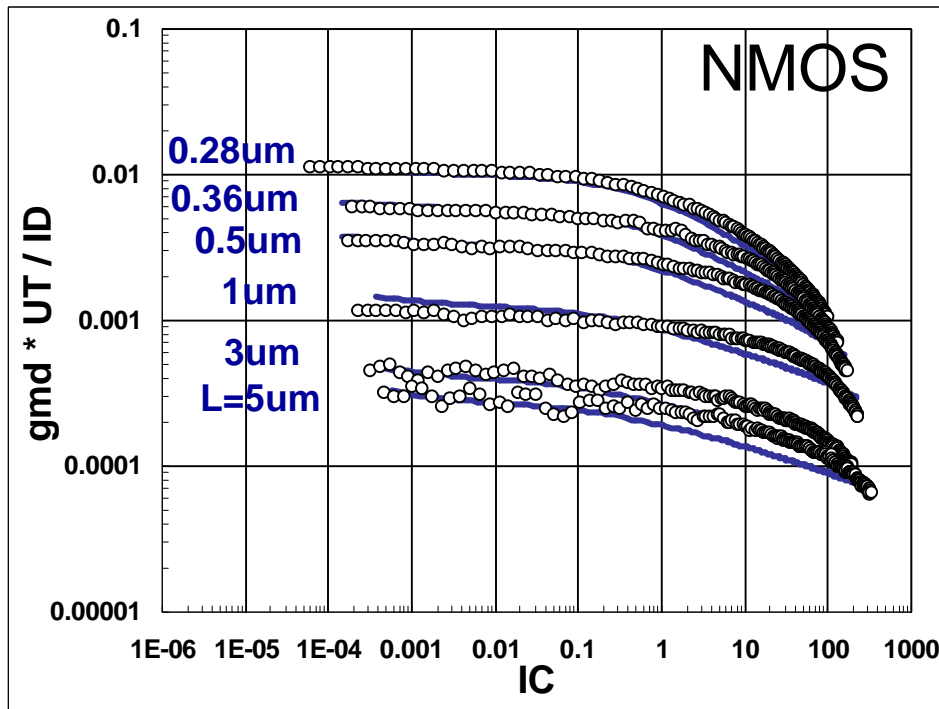
- $g_{mb} \cdot U_T / I_D$ vs. I_C is dependent on substrate effect
 - Asymptote in weak inversion: $(n-1)/n$
- $g_{mb} \approx g_{ms} \cdot (n-1)/n$

Drain Transconductance



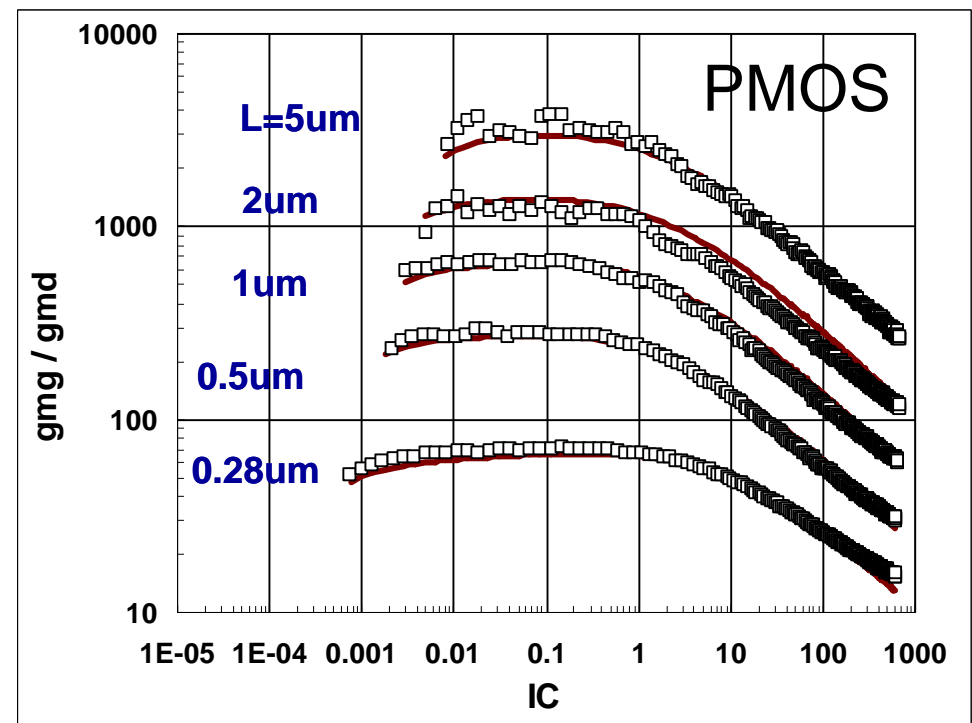
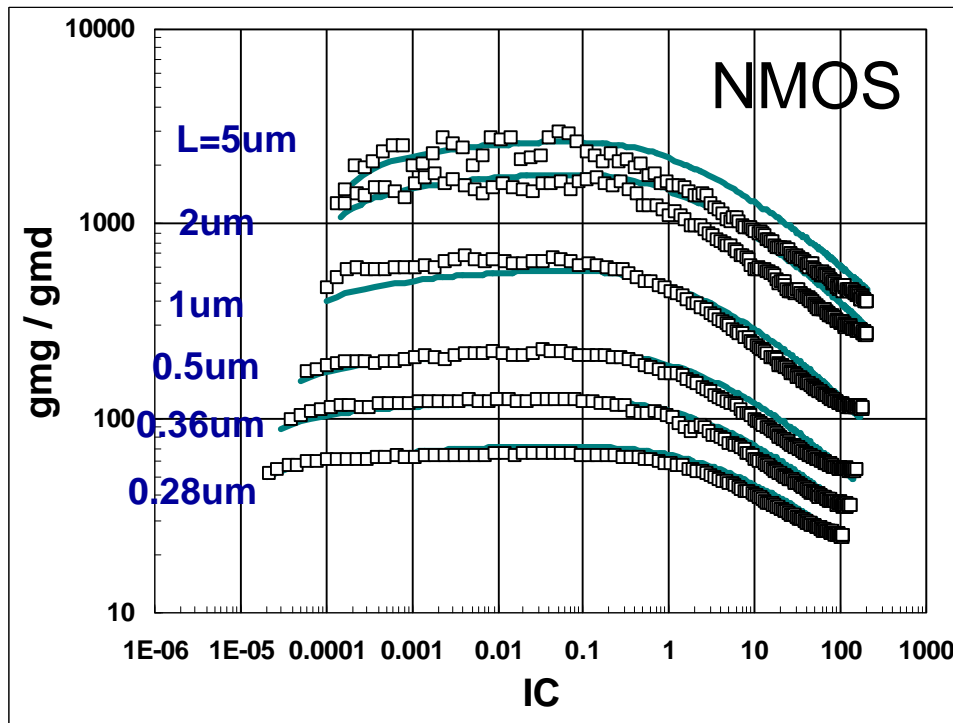
- $g_{md} * U_T / I_D = U_T / V_A$ where $V_A = I_D / g_{md}$ is “Early voltage”.
- $g_{md} * U_T / I_D$ shows very strong dependence on L !
- 1st-order G_D tends to underestimate the measured $g_{md} * U_T / I_D$

Drain Transconductance



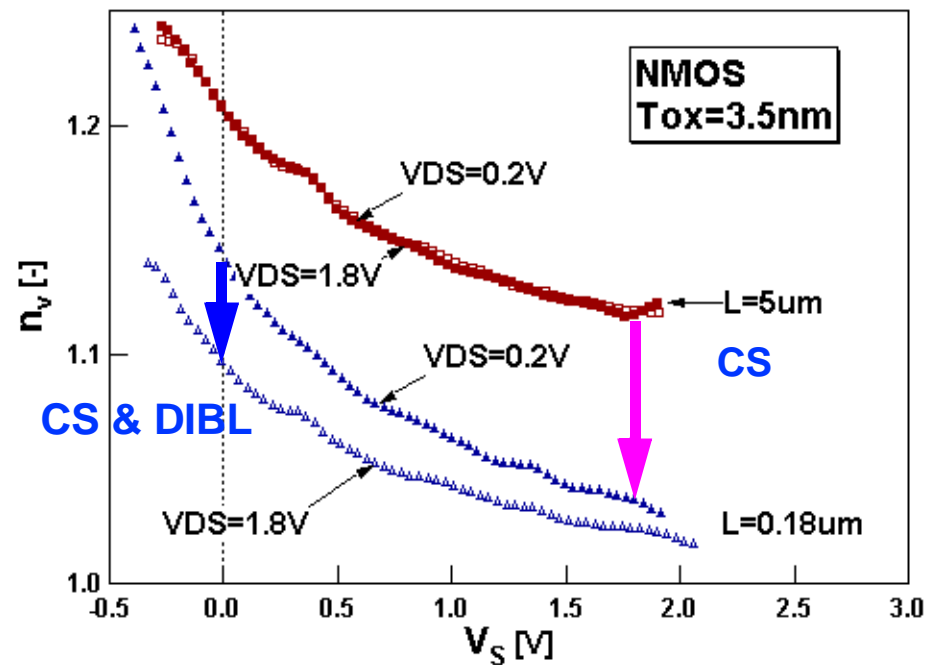
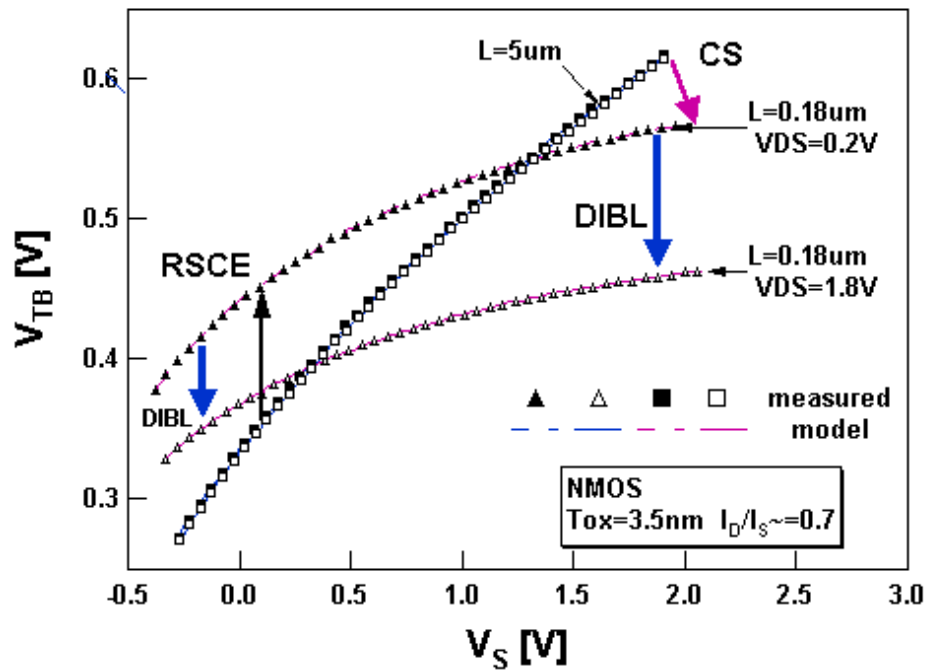
- $g_{md} * U_T / I_D$ reveals different scaling for NMOS and PMOS
 - WI: dominated by DIBL, Charge-sharing
 - SI: dominated by Vel. Sat., CLM, self-heating
- EKV 3.0 shows excellent $g_{md} * U_T / I_D$ modeling with IC, L

DC Self-Gain



- Intrinsic gain g_{mg} / g_{md} is highest in moderate (!!) inversion, long-channel devices
- EKV 3.0 shows excellent scaling abilities.

Short Channel V_T , n

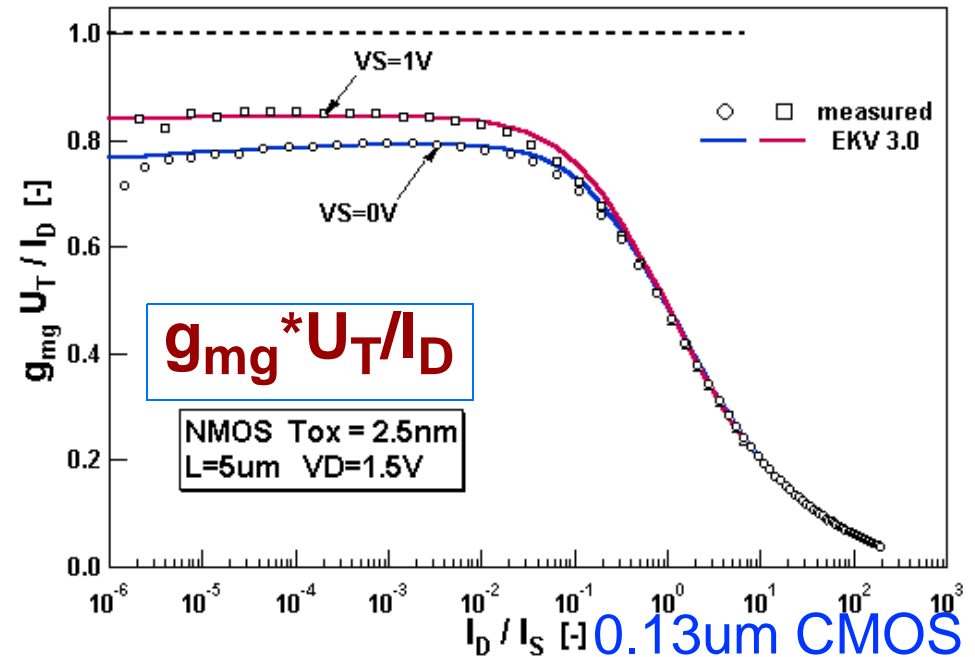
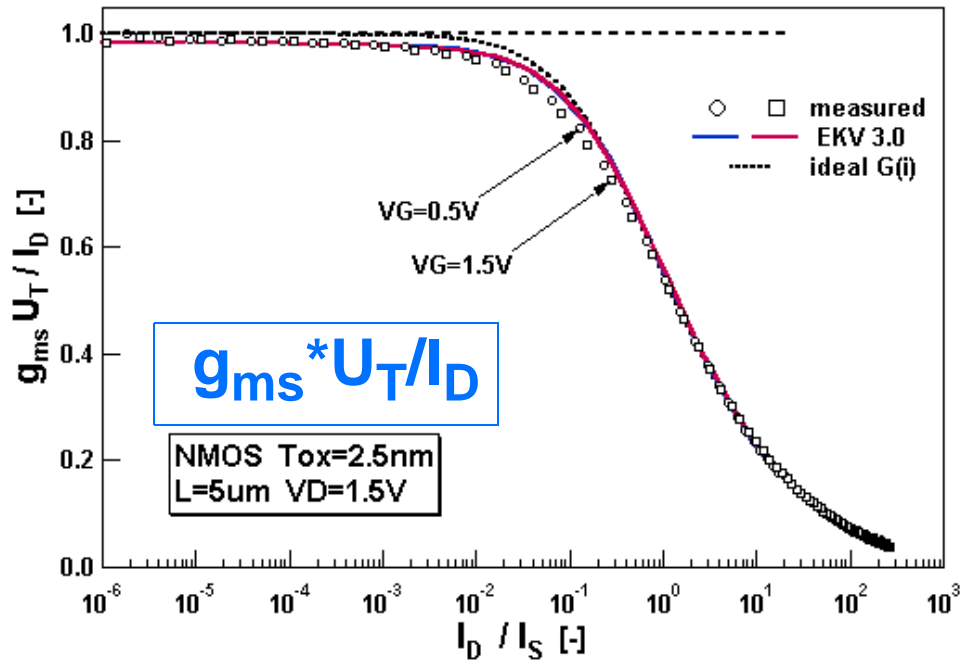


0.18um CMOS

■ Combination of all effects:

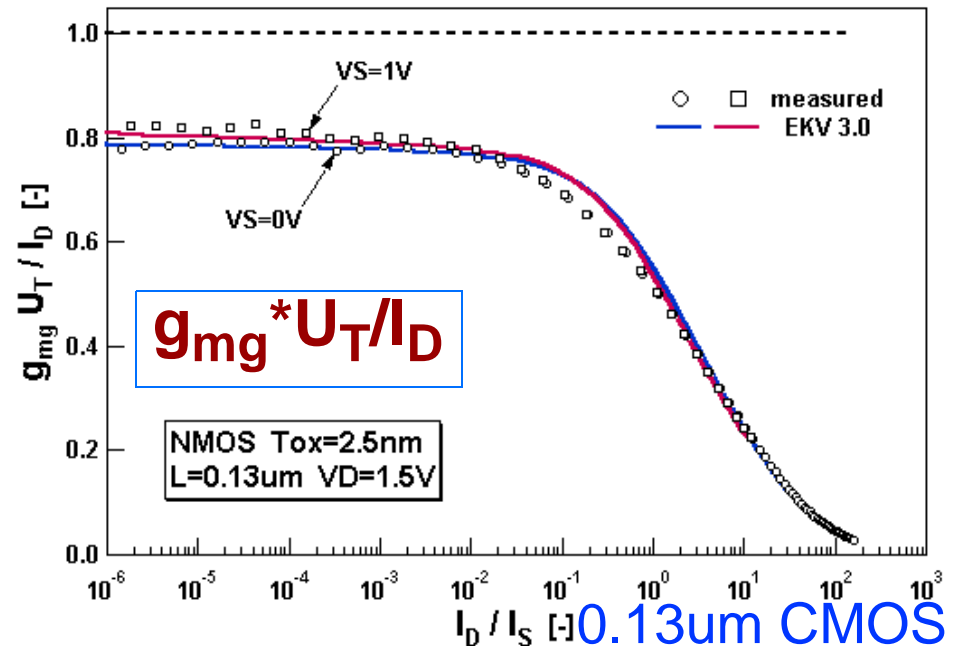
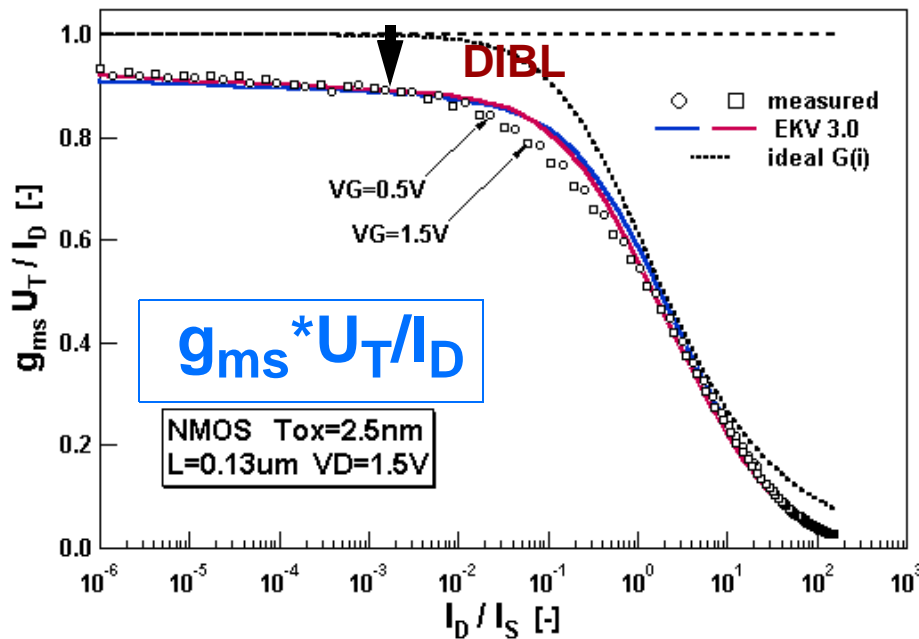
- Charge Sharing (CS) reduces substrate effect
- DIBL reduces threshold voltage @ short L, high V_D (*but not only!!!*)

Normalized $g_{ms}(g)/I_D$, long-channel



- Source- and gate transconductance-to-current ratio ($L=5\mu m$)
 - $g_{ms} * U_T / I_D$ is universal
 - $g_{mg} * U_T / I_D$ is affected by substrate effect: $g_{mg} = g_{ms} / n_v$

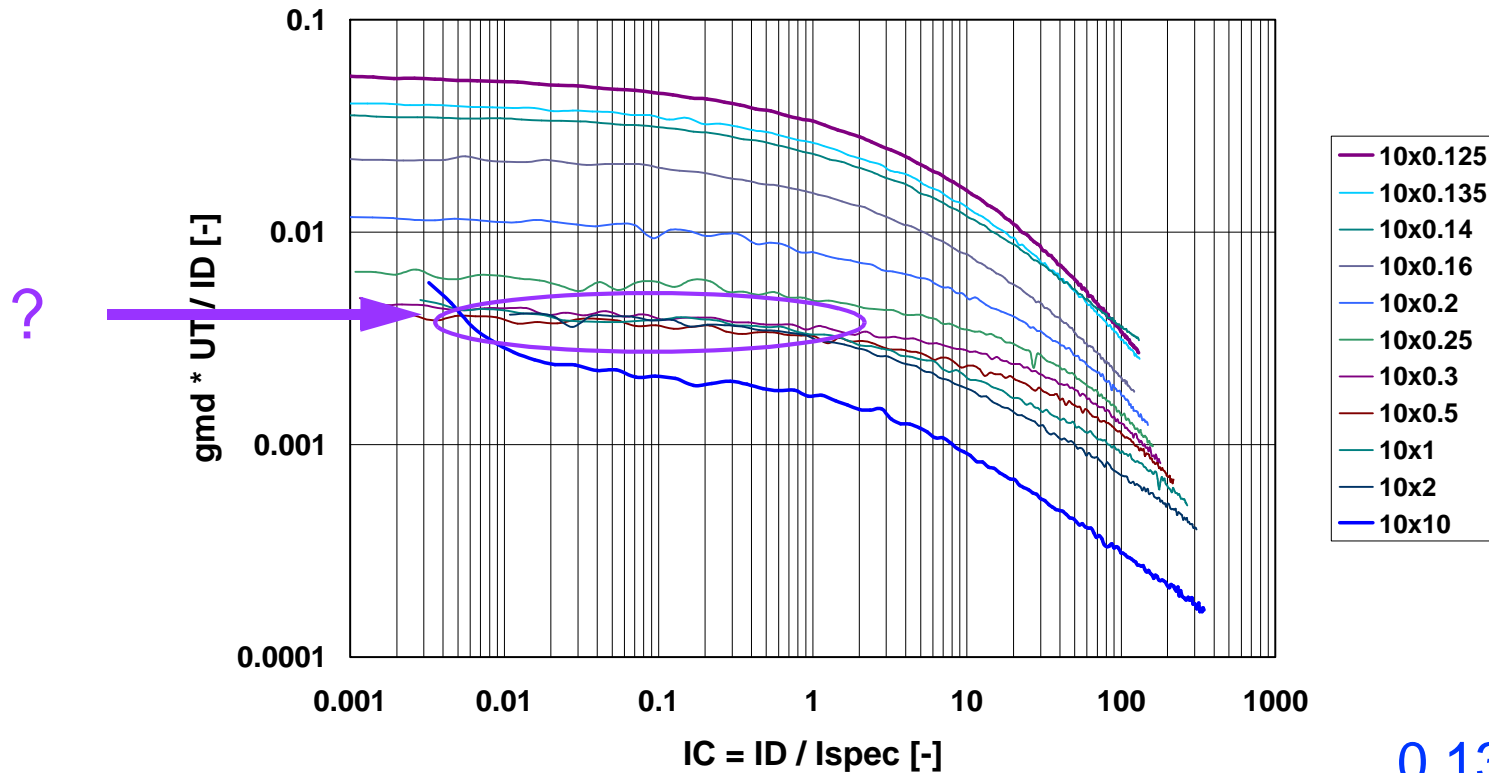
Normalized $g_{m(s)}/I_D$, short channel



0.13um CMOS

- Transconductance-to-current ratio vs. (log) current ($L=0.13\mu\text{m}$)
 - DIBL lowers $g_{ms} * U_T / I_D$ asymptote in weak inversion
 - Charge-sharing reduces substrate effect n_v for short-channel
- Excellent overall capabilities for EKV3.0 to model g/I_D vs. I_D .

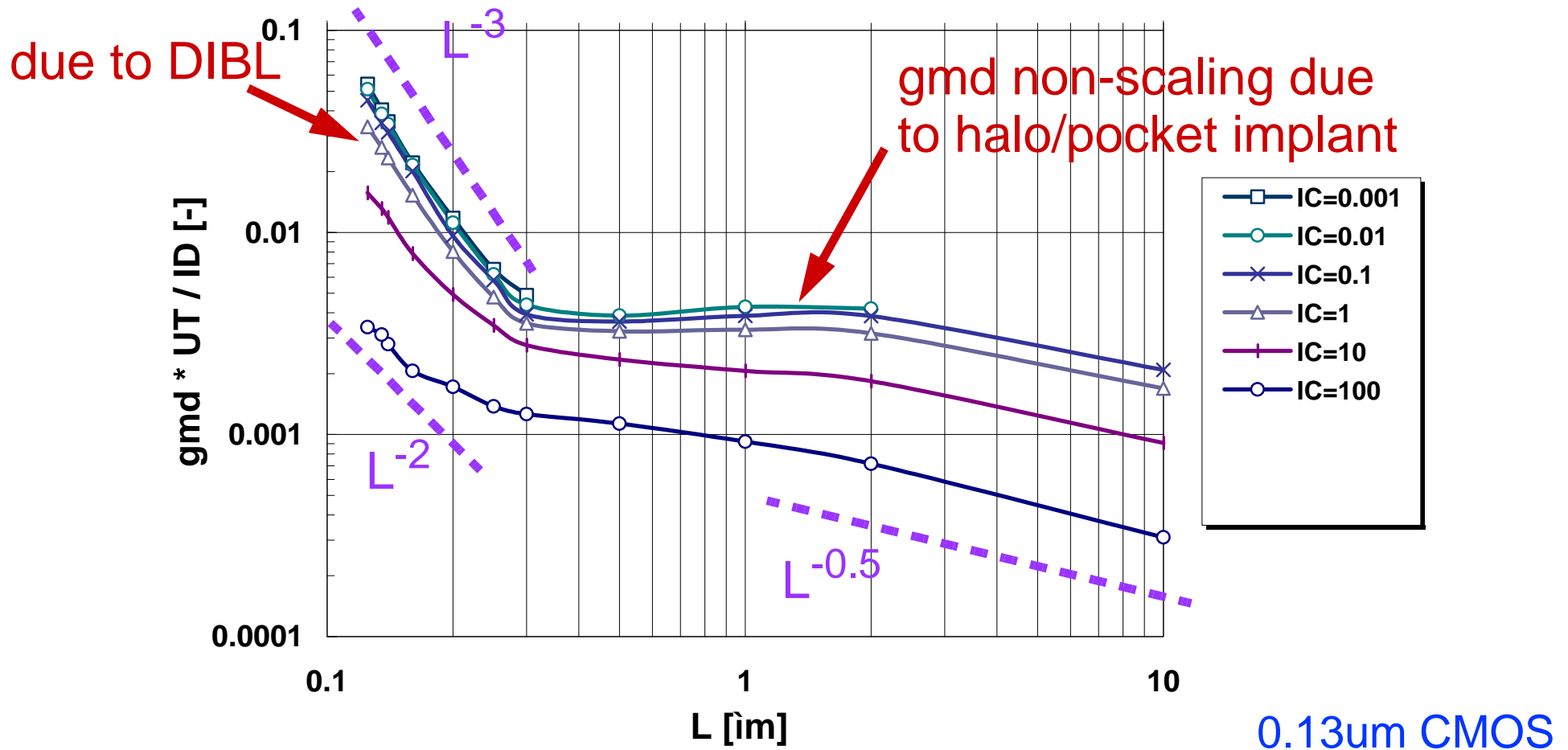
Normalized gmd vs. IC



0.13um CMOS

- Normalized gmd is generally dependent on IC
 - worse for short-channel, weak inversion
 - Scaling anomaly?

Normalized gmd vs. L (fixed IC)



- Scaling anomalies of normalized gmd with pocket/halo CMOS
 - Usual “design” assumption: normalized gmd $\sim L^{-1}$ -- *almost never met!*

Summary -- gmd scaling in pocket-CMOS

- Short-channel normalized gmd shows:
 - $\sim L^{-2}$ dependence *in strong inversion*
 - $\sim L^{-3}$ dependence *in weak inversion*
- Intermediate channel length: *deterioration* of normalized gmd
 - Shows a *scaling anomaly* in normalized gmd
- Long-channel gmd shows $\sim L^{-0.5}$ dependence
- Conclusion: pocket implants improve short-channel gmd, but degrade long-channel gmd
 - Cause: (drain-side) barrier-lowering in longer-channel devices
Chatterjee e.a. VLSI Symp. 1999, Buss e.a. IEDM 1999

Conclusions

- EKV MOS transistor model provides ideal framework for analysis of fundamental MOS characteristics
 - Consistent normalization of model quantities
- Analysis of Source, Gate, Substrate & Drain Transconductances with EKV
 - Simultaneous modeling vs. level of inversion (IC) and channel lengths
 - Provides useful information for advanced analog IC design -- parameter extraction -- MOSFET model benchmarking.
- *Short-channel scaling* of normalized gmd:
 - Strong inversion $\sim L^{-1} \dots L^{-2}$
 - Weak/moderate inversion: gmd $\sim L^{-3}$
- *Scaling anomaly* in normalized gmd due to pocket/halo implant @ intermediate channel lengths -- *shown for the first time*.
 - Long-channel pocket implant effect under development.

Contact

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EKV2.6 website:

<http://legwww.epfl.ch/ekv/>

EKV3.0 Model Tutorial:

Thursday March 11, 1:30 PM

