Geometry- and Bias-Dependence of Normalized Transconductances in Deep Submicron CMOS

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Outline

- Introduction
- EKV MOSFET Model Basics
- Normalized Transconductances Method
  - Analysis vs. level of inversion and channel length
- Examples using EKV3.0 MOSFET model with 0.25um, 0.13um CMOS
- Conclusions
Introduction

- Rapid evolution & increasing complexity of CMOS technology
- Moderate/weak inversion increasingly important.
  - Analog/mixed signal, wireless RF, LV-LP battery operated equipment requires novel circuit solutions.
- Need for efficient analog design methods
  - Rapid evaluation of design trade-offs: gain, bandwidth, linearity, matching, noise, chip area.
  - Hand-calculation and full circuit simulation.
- Transconductance method based on EKV MOS transistor model:
  - Normalization of current, voltage, transconductances,...
  - Analysis of MOSFET vs. level of inversion & channel length.
  - EKV 3.0 MOSFET model for deep submicron CMOS.
MOSFET Basics -- Linearization of Qi

Consider charge and voltage balance:

\[ -\frac{Q_i'}{C_{ox}} = \gamma \sqrt{U_T} \cdot \left[ \frac{\Psi_S}{U_T} + \exp\left[\frac{\Psi_S - 2\Phi_F - V_{ch}}{U_T}\right] \right] - \sqrt{\frac{\Psi_S}{U_T}} \]

\[ V_G = V_{FB} + \Psi_S + \gamma \sqrt{\Psi_S} - \frac{Q_i'}{C_{ox}} \]

- \( Q_i' \) is almost linear w.r.t. surface potential \( \Psi_S \) at fixed \( V_G \).
- Linearization is essential to analytic charge-sheet model.

Inversion Charge Linearization:

\[ \frac{dQ_i'}{C_{ox}} \approx n \cdot d\Psi_S \]

Pinch-off Surface Potential:

\[ \Psi_{SP} \equiv \Psi_S \mid Q_i = 0 \]

Pinch-off Voltage:

\[ V_P \equiv \Psi_{SP} - \phi \]
Pinch-off Voltage, Slope Factor

\[ n \approx \frac{\partial V_G}{\partial V_P} = 1 + \frac{\gamma}{2\sqrt{\phi + V_P}} \]

**Slope Factor:**

**Pinch-off Voltage:**

\[ V_P \approx \frac{V_G - V_{TO}}{n} \]

\[ V_{TO} = V_{FB} + \phi + \gamma \sqrt{\phi} \]

\[ \gamma = \frac{\sqrt{2q\varepsilon_{si}N_{sub}}}{C'_{ox}} \quad C'_{ox} = \frac{\varepsilon_{ox}}{T_{ox}} \]

\[ \phi \approx 2\phi_F + m \cdot U_T = U_T \cdot \left[ 2\ln\left(\frac{N_{sub}}{n_i}\right) + m \right] \]

- \( V_P, n \) account for the substrate effect
- \( T_{ox}, N_{sub}, V_{FB} \), same parameters as in surface potential model
Charge Sheet Model

- Consider drift and diffusion current transport, use linearization:

\[
I_D \cdot dx = \mu W[-Q'_i \cdot d\Psi_S + U_T \cdot dQ'_i] = \mu W\left[-\frac{Q'_i}{nC'_{ox}} + U_T\right] \cdot dQ'_i
\]

- Integrate from source to drain:

\[
I_D = 2nU_T^2 \cdot \mu C'_{ox} \frac{W}{L} \cdot (i_f - i_r)
\]

- with current-charge relationships:

\[
i_{f(r)} = q_{f(r)}^2 + q_{f(r)} \quad \text{or,} \quad q_{f(r)} = \sqrt{1/4 + i_{f(r)}}
\]

- Consider channel conductance:

\[
\frac{dI_D}{dV_{ch}} = \mu \cdot \frac{W}{L} \cdot (-Q'_i)
\]

- ... in normalized form:

\[
\frac{di_{f(r)}}{d\nu_{S(D)}} = q_{f(r)} = \sqrt{1/4 + i_{f(r)}} = i_{f(r)} \cdot G(i_{f(r)})
\]

- Integration yields Voltage-Charge relationship:

\[
\nu_P - \nu_{S(D)} = 2q_{f(r)} + \ln(q_{f(r)})
\]
Normalization of Drain Current and Voltages

Inversion Coefficient (IC) is meaningful for operation in **saturation** ... covering all the range from weak to strong inversion

Normalization of voltages by \( U_T = kT/q \): \( \nu_{G(S,D)} = V_{G(S,D)}/U_T \).

Inversion Coefficient:
\[
IC = \frac{I_D}{I_{Spec}}
\]

Specific Current:
\[
I_{Spec} = I_0 \cdot \frac{W}{L} = 2nU_T^2 \mu C'_{ox} \cdot \frac{W}{L}
\]
Transconductance-to-Current Ratio

- $G(\text{IC})$: normalized transconductance-to-current ratio:
  - compared to exact surface potential model
- $G(\text{IC})$ vs. IC is a *universal* characteristic of the MOSFET
  - ... independent of bias (saturation), Temp., technology (long-channel).
MOS Transistor Transconductances

- Source-, gate-, drain- and substrate transconductances:

\[
g_{ms} = - \left. \frac{\partial}{\partial V_S} (I_D) \right|_{V_G,V_D} \\
g_{mg} = \left. \frac{\partial I_D}{\partial V_G} \right|_{V_S,V_D} \\
g_{md} = \left. \frac{\partial I_D}{\partial V_D} \right|_{V_G,V_S}
\]

\[
g_{mb} = g_{ms} - g_{mg} - g_{md}
\]
Transconductances Analysis

- Fundamental relationships:
  \( g_{mg} = \frac{g_{ms} - g_{md}}{n} \quad g_{mb} = \frac{n - 1}{n} g_{mg} \)

- Transconductance-to-current ratios:
  \( G_x \equiv \frac{g_{mx} \cdot U_T}{I_D} \)

- 1st-order expressions of transconductance-to-current ratios:
  \( G_G \equiv \frac{G(IC)}{n} \quad G_S \equiv G(IC) \quad G_G \equiv \frac{n - 1}{n} G(IC) \)
  \( G_D \equiv G(IC) \cdot \frac{\partial V_P}{\partial V_D} + \frac{U_T}{n} \cdot \frac{\partial n}{\partial V_D} \)

- 1st-order expressions are valid mostly in moderate & weak inversion.
- \( G_D \) is also directly dependent on \( G(IC) \) and short-channel effects in \( V_P, n \)
Gate Transconductance

- $g_m * U_T / I_D$ vs. $I_D / I_{spec}$
  - BSIM3v3 cannot fit a large range in moderate/weak inversion (parameter extraction dependent; but the problem is structural).
- measured at $V_S = 0$, $V_D = V_G$ (saturation).
Gate Transconductance

- EKV 3.0 fit from weak to strong inversion, for long & short-channel devices (NMOS)
  - Asymptote in weak inversion: $1/n$
- Weak inversion slope ($S \approx \ln 10 \cdot n \cdot U_T$) is dependent on IC.
Source Transconductance

- $g_{ms} U_T/I_D$ vs. IC is universal
  - indep. of: VG, Temp., W, L (except very short transistors)
  - Asymptote in weak inversion: $\sim 1$

- $g_{mg} \sim g_{ms}/n$ (saturation)
Substrate Transconductance

- $g_{mb}^*U_T/I_D$ vs. IC is dependent on substrate effect
  - Asymptote in weak inversion: $(n-1)/n$
- $g_{mb} \sim g_{ms}^*(n-1)/n$
Drain Transconductance

- $g_{md} \frac{U_T}{I_D} = \frac{U_T}{V_A}$ where $V_A = \frac{I_D}{g_{md}}$ is “Early voltage”.
- $g_{md} \frac{U_T}{I_D}$ shows very strong dependence on $L$!
- 1st-order $G_D$ tends to underestimate the measured $g_{md} \frac{U_T}{I_D}$
Drain Transconductance

- $g_{md} * U_T / I_D$ reveals different scaling for NMOS and PMOS
  - W.I: dominated by DIBL, Charge-sharing
  - S.I: dominated by Vel. Sat., CLM, self-heating
- EKV 3.0 shows excellent $g_{md} * U_T / I_D$ modeling with IC, L
Intrinsic gain $g_{mg} / g_{md}$ is highest in moderate (!!!) inversion, long-channel devices.

EKV 3.0 shows excellent scaling abilities.
Short Channel VT, n

- Combination of all effects:
  - Charge Sharing (CS) reduces substrate effect
  - DIBL reduces threshold voltage @ short L, high $V_D$ (*but not only!!!*)
Normalized gms(g)/ID, long-channel

- Source- and gate transconductance-to-current ratio (L=5um)
  - \( g_{ms} \cdot U_T / I_D \) is universal
  - \( g_{mg} \cdot U_T / I_D \) is affected by substrate effect: \( g_{mg} = g_{ms} / n_v \)
Normalized gmg(s)/ID, short channel

- Transconductance-to-current ratio vs. (log) current (L=0.13um)
  - DIBL lowers $g_{ms}U_T/I_D$ asymptote in weak inversion
  - Charge-sharing reduces substrate effect $n_v$ for short-channel
- Excellent overall capabilities for EKV3.0 to model $g/I_D$ vs. $I_D$. 

0.13um CMOS
Normalized gmd vs. IC

Normalized gmd is generally dependent on IC

- worse for short-channel, weak inversion
- Scaling anomaly?

0.13um CMOS
Scaling anomalies of normalized gmd with pocket/halo CMOS

- Usual “design” assumption: normalized gmd $\sim L^{-1}$ -- almost never met!
Summary -- gmd scaling in pocket-CMOS

- Short-channel normalized gmd shows:
  - \( \sim L^{-2} \) dependence in strong inversion
  - \( \sim L^{-3} \) dependence in weak inversion
- Intermediate channel length: deterioration of normalized gmd
  - Shows a scaling anomaly in normalized gmd
- Long-channel gmd shows \( \sim L^{-0.5} \) dependence
- Conclusion: pocket implants improve short-channel gmd, but degrade long-channel gmd
  - Cause: (drain-side) barrier-lowering in longer-channel devices
    Chatterjee e.a. VLSI Symp. 1999, Buss e.a. IEDM 1999
Conclusions

- EKV MOS transistor model provides ideal framework for analysis of fundamental MOS characteristics
  - Consistent normalization of model quantities
- Analysis of Source, Gate, Substrate & Drain Transconductances with EKV
  - Simultaneous modeling vs. level of inversion (IC) and channel lengths
  - Provides useful information for advanced analog IC design -- parameter extraction -- MOSFET model benchmarking.
- Short-channel scaling of normalized gmd:
  - Strong inversion \( \sim L^{-1..-2} \)
  - Weak/moderate inversion: \( \text{gmd} \sim L^{-3} \)
- Scaling anomaly in normalized gmd due to pocket/halo implant @ intermediate channel lengths -- shown for the first time.
  - Long-channel pocket implant effect under development.
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EKV2.6 website:

http://legwww.epfl.ch/ekv/

EKV3.0 Model Tutorial:

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