

Workshop on Compact Modeling
The 7th International Conference on Modeling and Simulation of Microsystems

(Boston, Massachusetts, USA. March 9–11, 2004)

Overview

Compact Models (CMs) for circuit simulation have been at the heart of CAD tools for circuit design over the past decades, and are playing an ever increasingly important role in the nanometer system-on-chip (SOC) era. Although not highly “visible” to circuit designers and technology developers, a compact model plays the key role in accuracy and efficiency of the circuit simulator being used by designers as well as a bridge to the technology to which the design is to be fabricated. Like the role CM is played in circuit simulation, CM developers play the similar role in bridging the circuit designers and technology developers. As the mainstream MOS technology is scaled into the nanometer regime, development of a truly physical and predictive compact model for circuit simulation that covers geometry, bias, temperature, DC, AC, RF, and noise characteristics becomes a major challenge. This demands that CM developers work more closely with the technology people and the design community.

Objective

Workshop on Compact Modeling (WCM) is one of the first of its kind in bringing people in the CM field together. The *objective* of WCM is to create a truly open forum for discussion among experts in the field as well as feedback from technology developers, circuit designers, and CAD tool vendors. The creation of WCM is a natural response of the CM community to the increasing demand in the field, and it will position itself as a premier forum for CM developers in information exchange and promotion of modeling diversity. Ultimately, the result of such a forum will benefit not only the model developers, but also as a service to the entire technology, modeling, and design communities.

Scope

The *scope* of WCM covers compact models for circuit simulation, which is centered at the mainstream MOS intrinsic models and extended to SOI, bipolar, interconnect, extrinsic, statistical, numerical-based, and reliability models. The key application is for circuit simulation and, hence, numerical simulation and pure theoretical and experimental work will not be within the scope of WCM.

Topics

The *topics* for WCM are largely categorized into the following areas:

- Bulk MOS intrinsic models
- SOI/double-gate/floating-gate MOS models
- Bipolar/HBT/SiGe/GaN/JFET models
- RF/noise/scalable capacitance/NQS models
- Statistical/predictive/process-based models
- Interconnection/passive device models

- Extrinsic/parasitic element models
- Reliability/hot carrier/tunneling/ESD models
- Atomic-level/quantum-mechanical compact models
- Numerical/TCAD/behavioral/table-based models
- Model parameter extraction and optimization
- Model–simulator interface and standardization

WCM-MSM2004

The third *Workshop on Compact Modeling* (WCM-MSM2004) will be held in collaboration with *the 7th International Conference on Modeling and Simulation of Microsystems* at **Nanotech 2004** in Boston, Massachusetts, USA on March 9–11, 2004. It is planned to have an *Invited-Speaker Session*, a contributed *Poster Session*, as well as a *Tutorial Session*.

Invited Speakers

Invited speakers from all over the world (11 countries) are listed below:

- *Narain Arora*, Cadence Design Systems, USA
- *Matthias Bucher*, Technical University of Crete, Greece
- *Mansun Chan*, Hong Kong University of Science and Technology, Hong Kong
- *Yuhua Cheng*, Skyworks Solutions, USA
- *Jamal Deen*, McMaster University, Canada
- *Robert Dutton*, Stanford University, USA
- *Carlos Galup-Montoro*, Universidade Federal de Santa Catarina, Brazil
- *Dirk Klaassen*, Philips Research Laboratories, The Netherlands
- *Shiuh-Wuu Lee*, Intel, USA
- *Juin Liou*, University of Central Florida, USA
- *Colin McAndrew*, Motorola, USA
- *James Meindl*, Georgia Institute of Technology, USA
- *Mitiko Miura-Mattausch*, Hiroshima University, Japan
- *Paolo Pavan*, Università di Modena e Reggio Emilia, Italy
- *Michael Schroter*, University of Technology Dresden, Germany
- *Michael Shur*, Rensselaer Polytechnic Institute, USA
- *Xuemei Xi*, University of California at Berkeley, USA
- *Zhiping Yu*, Tsinghua University, China
- *Xing Zhou*, Nanyang Technological University, Singapore

Workshop Program

There are 19 invited papers, which are categorized in the following topic areas (speakers underlined):

Advanced device models (SiGe, GaN, Ballistic MOS):

- Technology Limits and Compact Model for SiGe Scaled FETs
Chang-Hoon Choi and Robert W. Dutton, Stanford University, US
- Compact Models for AlGaIn/GaN MOS Devices
M. S. Shur, G. Simin, A. Khan, and R. Gaska, Rensselaer Polytechnic Institute, US

- Ballistic MOS Model (BMM) Considering Full 2D Quantum Effects
Zhiping Yu, Dawei Zhang, and Lilin Tian, Tsinghua University, CN

Bulk MOS intrinsic models:

- Geometry- and Bias-Dependence of Normalized Transconductances in Deep Submicron CMOS
M. Bucher, D. Kazazis, F. Krummenacher**, National Technical University Athens, GR, *Brown University, US, **Swiss Federal Institute of Technology, Lausanne, CH*
- Self-Consistent DC, AC, Noise and Mismatch for the MOSFET
C. Galup-Montoro, M. C. Schneider, A. Arnaud, and H. Klimach, Universidade Federal de Santa Catarina, BR
- Recent Enhancements of MOS Model 11
R. van Langevelde, A. J. Scholten, and D. B. M. Klaassen, Philips Research Laboratories, NE
- Noise Modeling with HiSIM Based on Self-Consistent Surface-Potential Description
M. Miura-Mattausch, S. Hosokawa, D. Navarro, H. Ueno, H. J. Mattausch, T. Ohguro, S. Kumashiro, M. Taguchi, T. Kage, and S. Miyamoto, Hiroshima University, JP
- The Development of Next Generation BSIM for Sub-100nm Mixed-Signal Circuit Simulation
Xuemei Xi, Jin He, Mansun Chan, Chung-Hsun Lin, Mohan Dunga, Babak Heyderi, Hui Wan, Ali M. Niknejad, and Chenming Hu, University of California at Berkeley, US
- Unified Regional Approach to Consistent and Symmetric DC/AC Modeling of Deep-Submicron MOSFETs
Xing Zhou, Siau Ben Chiah, Karthik Chandrasekaran, Khee Yong Lim, Lap Chan*, and Sanford Chu*, Nanyang Technological University, *Chartered Semiconductor Manufacturing, SG*

Interconnect models:

- Modeling and Characterization of Wire Inductance for High Speed VLSI Design
Narain D. Arora and Li Song, Cadence Design Systems, US
- Emerging Challenges in Compact Modeling
Shiuh-Wuu Lee, Paul Packan, Changhong Dai, and Nagib Hakim, Intel, US

Passive device models:

- R3, an Accurate JFET and 3-Terminal Diffused Resistor Model
Colin McAndrew, Motorola, US

RF/noise models:

- Advanced MOSFET Modeling for RF IC Design
Yuhua Cheng, Skyworks Solutions, US
- RF Noise Models of MOSFETs – A Review
Saman Asgaran and M. Jamal Deen, McMaster University, CA

Bipolar models:

- Bias Dependent Modeling of Collector-Base Junction Effects in Bipolar Transistors

Michael Schroter and H. Tran, University of Technology Dresden, DE

Double-gate MOS models:

- Quasi-2D Compact Modeling for Double-Gate MOSFET
Mansun Chan, Jin He, Xuemei Xi*, Chung-Hsun Lin*, Tze Yin Man, Xinnan Lin, Ping K. Ko, Ali M. Niknejad, and Chenming Hu**, Hong Kong University of Science and Technology, HK, *University of California at Berkeley, US
- Compact, Physics-Based Modeling of Nanoscale Limits of Double-Gate MOSFETs
Qiang Chen, Lihui Wang, Raghunath Murali, and James D. Meindl, Georgia Institute of Technology, US

Floating-gate MOS models:

- Floating Gate Devices: Operation and Compact Modeling
Paolo Pavan, Luca Larcher, and Andrea Marmiroli, Università di Modena e Reggio Emilia, IT

ESD models:

- Compact MOSFET Model for Electrostatic Discharge (ESD) Applications
Juin J. Liou and Xiaofeng Gao, University of Central Florida, US

Poster Session

Poster presentations in the scope of “compact models for circuit simulation” are solicited. A **10-minute oral briefing** for each poster paper is planned before the poster presentation session.

Contributed poster papers are listed below (presenters underlined):

- A Non-Charge-Sheet Analytical Theory of Undoped Symmetric Double-Gate MOSFETs from the Exact Solution of Poisson’s Equation using SPP Approach
Jin He, Xuemei Xi, Chung-Hsun Lin, Mansun Chan, Ali Niknejad, and Chenming Hu, University of California at Berkeley, US
- An Exact Analytical Model of Undoped Body MOSFETs using the SPP Approach
Jin He, Xuemei Xi, Mansun Chan, Ali Niknejad, and Chenming Hu, University of California at Berkeley, US
- Linear Cofactor Difference Extrema of MOSFET’s Drain Current and Their Application in Parameter Extraction
Jin He, Xuemei Xi, Mansun Chan, Ali Niknejad, and Chenming Hu, University of California at Berkeley, US
- Threshold-Voltage-Based Regional Modeling of MOSFETs with Symmetry and Continuity
Siau Ben Chiah, Xing Zhou, Karthik Chandrasekaran, Khee Yong Lim, Lap Chan*, and Sanford Chu**, Nanyang Technological University, *Chartered Semiconductor Manufacturing, SG
- Physics-Based Scalable Threshold-Voltage Model for Strained-Silicon MOSFETs
Karthik Chandrasekaran, Xing Zhou, and Siau Ben Chiah, Nanyang Technological University, SG
- An Analytical Subthreshold Current Model for Ballistic Double-Gate MOSFETs

J. L. Autran, D. Munteanu, O. Tintori, M. Aubert, and E. Decarre, Laboratoire Matériaux et Microélectronique de Provence, FR

- Quantum-Mechanical Analytical Modeling of Threshold Voltage in Long-Channel Double-Gate MOSFET with Symmetric and Asymmetric Gates
J. L. Autran, D. Munteanu, O. Tintori, S. Harrison, E. Decarre, and T. Skotnicki*, Laboratory for Materials and Microelectronics of Provence, *STMicroelectronics, FR*
- Improved Compact Model for Four-Terminal DG MOSFETs
T. Nakagawa, T. Sekigawa, T. Tsutsumi, M. Hioki, E. Suzuki, and H. Koike, National Institute of Advanced Industrial Science and Technology, *Meiji University, JP*
- Predicting the SOI History Effect Using Compact Models
M. H. Na, J. S. Watts, E. J. Nowak, R. Q. Williams, and W. F. Clark, IBM, US
- New Capabilities for Verilog-A Implementations of Compact Device Models
M. Mierzwinski, P. O'Halloran, B. Troyanovsky, K. Mayaram, and R. Dutton**, Tiburon Design Automation, *Oregon State University, **Stanford University, US*
- A Practical Method to Extract Extrinsic Parameters for the Silicon MOSFET Small-Signal Model
Sheng-Chun Wang, Guo-Wei Huang, Kun-Ming Chen, Hua-Chou Tseng, and Tsun-Lai Hsu*, National Nano Device Laboratories, *United Microelectronics Corporation, TW*
- Automatic BSIM3/4 Model Parameter Extraction with Penalty Functions
Yuri Mahotin and Eugeny Lyumkis, Integrated Systems Engineering, US
- A Trial Report: HiSIM-1.2 Parameter Extraction for 90 nm Technology
Yoshihisa Iino, Silvaco Japan, JP
- Extraction of Extrinsic Series Parameter in RF CMOS
M. S. Alam and G. A. Armstrong, The Queen's University of Belfast, UK, *AMU, IN*
- Analytic Formulae for the Impact Ionization Rate for Use in Compact Models of Ultra-Short Semiconductor Devices
Hedley Morris, Monica M. De Pass**, and Henok Abebe, USC Information Sciences Institute, *San Jose State University, **Claremont Graduate University, US*
- On the Correlations Between Model Process Parameters in Statistical Modeling
Jirí Slezák, Aleš Litschmann, Stanislav Banáš, Radim Mlcoušek, and Martin Kejhar, ON Semiconductor, CZ
- Characterization and Modeling of Silicon Tapered Inductors
A. S. Peng, K. M. Chen, G. W. Huang, H. Y. Chen, and C. Y. Chang*, National Nano Device Laboratories, *National Chiao Tung University, TW*

Tutorial Session

Two tutorials are offered as listed below:

- Review of the EKV3.0 MOSFET Model
Matthias Bucher, Technical University of Crete, Greece
- RF CMOS: Current Status and Compact Modeling
Juin Liou, University of Central Florida, USA

Call for Participation

Workshop on Compact Modeling is initiated as a forum for model developers as well as interaction with the technology/design communities. It is mainly in the form of invited presentations for the specific topics in the compact modeling area. The topics cover all

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important aspects of compact model development and deployment, within the main theme – *compact models for circuit simulation*. Please visit the following website for updates:

<http://www.nanotech2004.com/WCM2004.html>

<http://www.ntu.edu.sg/home/exzhou/WCM/WCM2004/wcm04.htm>

For WCM-related enquiries, please contact *Dr. Xing Zhou* (exzhou@ntu.edu.sg). For general MSM-related enquiries, please contact *Ms. Sarah Wenning* (wenning@cr.org).

WCM-MSM2004, being the third one, will prove to be interesting and useful for people in a broad spectrum of fields: compact model developers, process engineers, device physicists, and circuit designers, in a variety of disciplines: universities, research institutions, chip manufacturers, wafer fabs, fabless companies, consulting firms, parameter-extraction tool and circuit-simulator vendors.

All are invited to participate in this exciting event!

WCM websites:

<http://www.nanotech2004.com/WCM2004.html>

<http://www.ntu.edu.sg/home/exzhou/WCM/>

(Updated: February 23, 2004)

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PROGRAM

(Note: For any changes/updates, please refer to website: <http://www.nanotech2004.com/2004program.html>)

DAY 1

WCM-1: Tuesday, March 9, 9:50 – 11:30

Session chair: *Xing Zhou, Nanyang Technological University*

- WCM Welcome and Introduction
Xing Zhou, Nanyang Technological University
- Technology Limits and Compact Model for SiGe Scaled FETs
R. W. Dutton and C.-H. Choi, Stanford University, US
- Compact Models for AlGaN/GaN MOS Devices
M. S. Shur, G. Simin, A. Khan, and R. Gaska, Rensselaer Polytechnic Institute, US
- Ballistic MOS Model (BMM) Considering Full 2D Quantum Effects
Z. Yu, D. Zhang, and L. Tian, Tsinghua University, CN

WCM-2: Tuesday, March 9, 13:30 – 15:00

Session chair: *Robert Dutton, Stanford University*

- Geometry- and Bias-Dependence of Normalized Transconductances in Deep Submicron CMOS
M. Bucher, D. Kazazis, F. Krummenacher**, Technical University of Crete, GR, *Brown University, US, **Swiss Federal Institute of Technology, Lausanne, CH*
- Self-Consistent DC, AC, Noise and Mismatch for the MOSFET
C. Galup-Montoro, M. C. Schneider, A. Arnaud, and H. Klimach, Universidade Federal de Santa Catarina, BR
- Recent Enhancements of MOS Model 11
R. van Langevelde, A. J. Scholten, and D. B. M. Klaassen, Philips Research Laboratories, NL

WCM-3: Tuesday, March 9, 15:30 – 17:00

Session chair: *Dirk Klaassen, Philips Research Laboratories*

- Noise Modeling with HiSIM Based on Self-Consistent Surface-Potential Description
M. Miura-Mattausch, S. Hosokawa, D. Navarro, S. Matsumoto, H. Ueno, H. J. Mattausch, T. Ohguro, T. Iizuka, M. Taguchi, T. Kage, and S. Miyamoto, Hiroshima University, JP
- The Development of Next Generation BSIM for Sub-100nm Mixed-Signal Circuit Simulation
X. Xi, J. He, M. Dunga, C.-H. Lin, B. Heyderi, H. Wan, M. Chan, A. M. Niknejad, and C. Hu, University of California at Berkeley, US
- Unified Regional Approach to Consistent and Symmetric DC/AC Modeling of Deep-Submicron MOSFETs

X. Zhou, S. B. Chiah, K. Chandrasekaran, K. Y. Lim*, L. Chan*, and S. Chu*, *Nanyang Technological University*, *Chartered Semiconductor Manufacturing, SG

DAY 2

WCM-4: Wednesday, March 10, 8:30 – 10:00

Session chair: *Jamal Deen, McMaster University*

- Modeling and Characterization of Wire Inductance for High Speed VLSI Design
N. D. Arora and L. Song, Cadence Design Systems, US
- Emerging Challenges in Compact Modeling
S.-W. Lee, P. Packan, C. Dai, and N. Hakim, Intel, US
- R3, an Accurate JFET and 3-Terminal Diffused Resistor Model
C. McAndrew, Motorola, US

WCM-5: Wednesday, March 10, 10:30 – 12:00

Session chair: *Mitiko Miura-Mattausch, Hiroshima University*

- Advanced MOSFET Modeling for RF IC Design
Y. Cheng, Skyworks Solutions, US
- RF Noise Models of MOSFETs – A Review
S. Asgaran and M. Jamal Deen, McMaster University, CA
- Bias Dependent Modeling of Collector-Base Junction Effects in Bipolar Transistors
M. Schroter and H. Tran, University of Technology Dresden, DE

WCM-6: Wednesday, March 10, 13:30 – 15:30

Session chair: *Shiuh-Wuu Lee, Intel*

- Quasi-2D Compact Modeling for Double-Gate MOSFET
M. Chan, T. Y. Man, J. He, X. Xi*, C.-H. Lin*, X. Lin, P. K. Ko, A. M. Niknejad, and C. Hu*, Hong Kong University of Science and Technology, HK, *University of California at Berkeley, US*
- Compact, Physics-Based Modeling of Nanoscale Limits of Double-Gate MOSFETs
Q. Chen, L. Wang, R. Murali, and J. D. Meindl, Georgia Institute of Technology, US
- Floating Gate Devices: Operation and Compact Modeling
P. Pavan, L. Larcher, and A. Marmiroli, Università di Modena e Reggio Emilia, IT
- Compact MOSFET Model for ESD Applications
J. J. Liou and X. Gao, University of Central Florida, US

Poster Oral Briefing: Wednesday, March 10, 15:50 – 17:00

Session chair: *Zhiping Yu, Tsinghua University*

- A Non-Charge-Sheet Analytical Theory of Undoped Symmetric Double-Gate MOSFETs from the Exact Solution of Poisson's Equation using SPP Approach
J. He, X. Xi, C.-H. Lin, M. Chan, A. Niknejad, and C. Hu, University of California at Berkeley, US
- An Exact Analytical Model of Undoped Body MOSFETs using the SPP Approach
J. He, X. Xi, M. Chan, A. Niknejad, and C. Hu, University of California at Berkeley, US
- Linear Cofactor Difference Extrema of MOSFET's Drain Current and Their Application in Parameter Extraction
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- Threshold-Voltage-Based Regional Modeling of MOSFETs with Symmetry and Continuity
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- Physics-Based Scalable Threshold-Voltage Model for Strained-Silicon MOSFETs
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- An Analytical Subthreshold Current Model for Ballistic Double-Gate MOSFETs
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- Quantum-Mechanical Analytical Modeling of Threshold Voltage in Long-Channel Double-Gate MOSFET with Symmetric and Asymmetric Gates
J. L. Autran, D. Munteanu, O. Tintori, S. Harrison, E. Decarre, and T. Skotnicki*, Laboratory for Materials and Microelectronics of Provence, *STMicroelectronics, FR*

Poster Session: Wednesday, March 10, 18:00 – 20:00
(Posters will remain till Thursday.)

DAY 3

Poster Oral Briefing: Thursday, March 11, 8:30 – 10:10
Session chair: *Juin Liou, University of Central Florida*

- Improved Compact Model for Four-Terminal DG MOSFETs
T. Nakagawa, T. Sekigawa, T. Tsutsumi, M. Hioki, E. Suzuki, and H. Koike, National Institute of Advanced Industrial Science and Technology, *Meiji University, JP*
- Predicting the SOI History Effect Using Compact Models
M. H. Na, J. S. Watts, E. J. Nowak, R. Q. Williams, and W. F. Clark, IBM, US
- New Capabilities for Verilog-A Implementations of Compact Device Models
M. Mierzewski, P. O'Halloran, B. Troyanovsky, K. Mayaram, and R. W. Dutton**, Tiburon Design Automation, *Oregon State University, **Stanford University, US*
- A Practical Method to Extract Extrinsic Parameters for the Silicon MOSFET Small-Signal Model
S.-C. Wang, G.-W. Huang, K.-M. Chen, H.-C. Tseng, and T.-L. Hsu*, National Nano Device Laboratories, *United Microelectronics Corporation, TW*
- Automatic BSIM3/4 Model Parameter Extraction with Penalty Functions
Y. Mahotin and E. Lyumkis, Integrated Systems Engineering, US
- A Trial Report: HiSIM-1.2 Parameter Extraction for 90 nm Technology
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- Extraction of Extrinsic Series Parameter in RF CMOS
M. S. Alam and G. A. Armstrong, The Queen's University of Belfast, UK, *AMU, IN*
- Analytic Formulae for the Impact Ionization Rate for Use in Compact Models of Ultra-Short Semiconductor Devices
H. Morris, M. M. De Pass**, and H. Abebe, USC Information Sciences Institute, *San Jose State University, **Claremont Graduate University, US*
- On the Correlations Between Model Process Parameters in Statistical Modeling
J. Slezák, A. Litschmann, S. Banáš, R. Mlcoušek, and M. Kejhar, ON Semiconductor, CZ
- Characterization and Modeling of Silicon Tapered Inductors
A. S. Peng, K. M. Chen, G. W. Huang, H. Y. Chen, and C. Y. Chang*, National Nano Device Laboratories, *National Chiao Tung University, TW*

Poster Session: Thursday, March 11, 10:00 – 12:00

Tutorials: Thursday, March 11, 13:30 – 16:30

- Review of the EKV3.0 MOSFET Model
Matthias Bucher, Technical University of Crete, Greece
- RF CMOS: Current Status and Compact Modeling
Juin Liou, University of Central Florida, USA