

PHILIPS

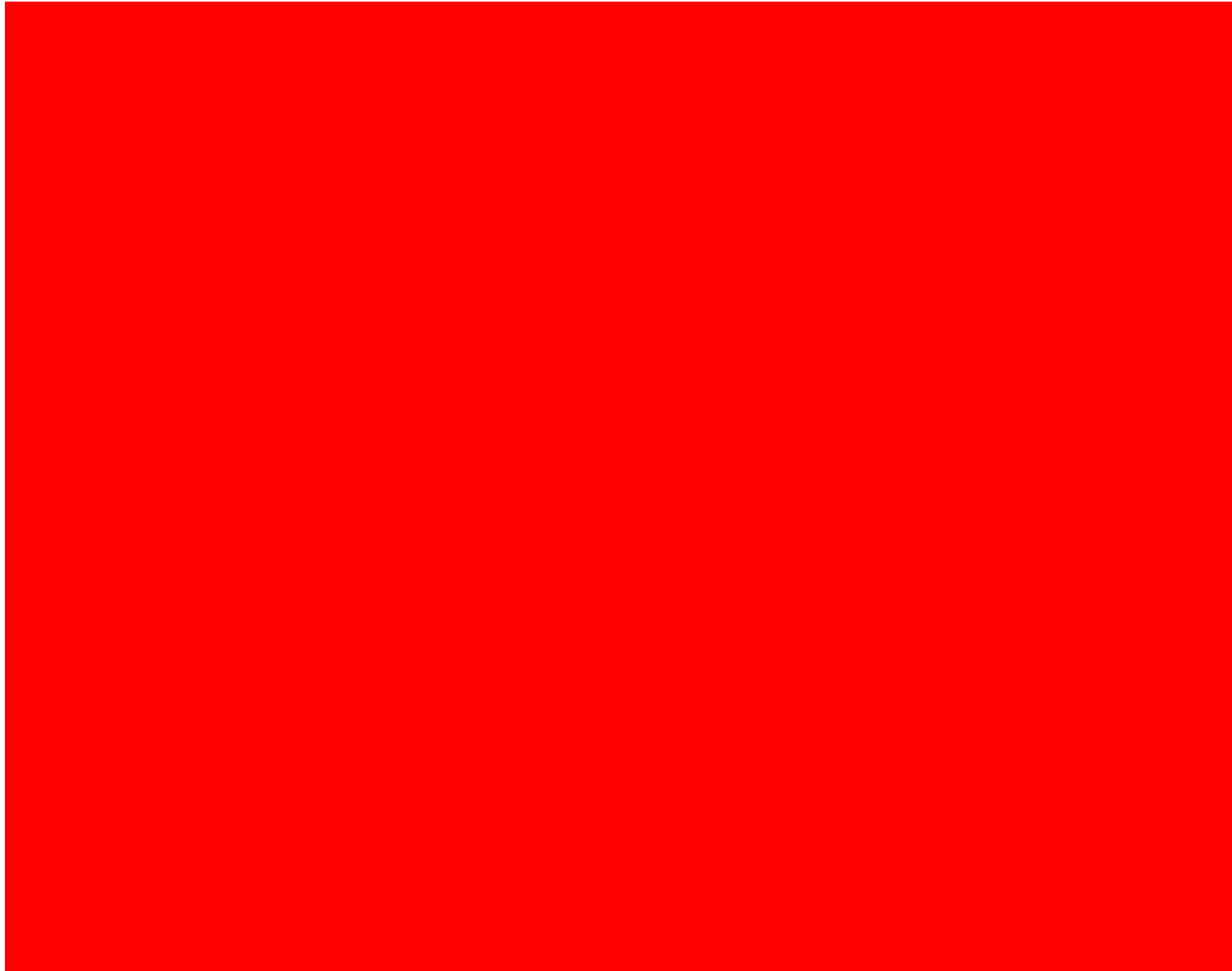
The Role of Compact Models in the Fab and Fabless Business

D.B.M. Klaassen

MSM Workshop on Compact Modeling

San Francisco, CA

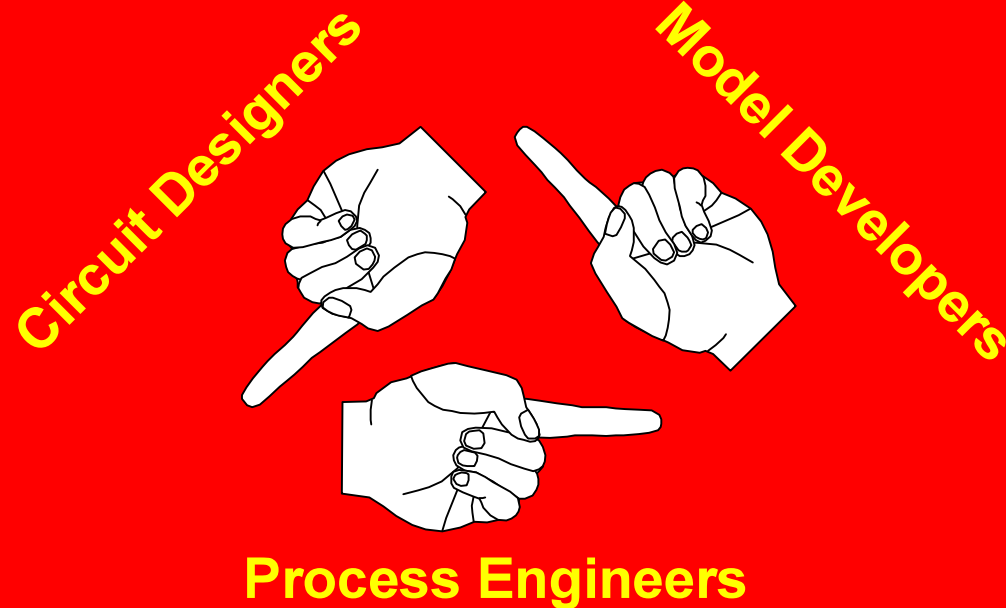
February, 2003



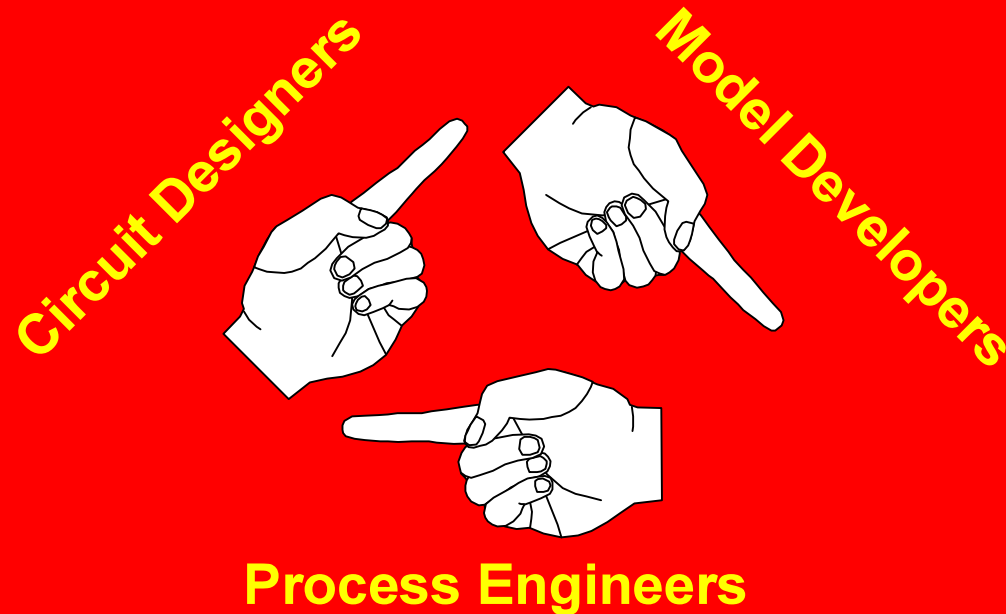
when chips are down,

**when chips are down,
the finger pointing starts....**

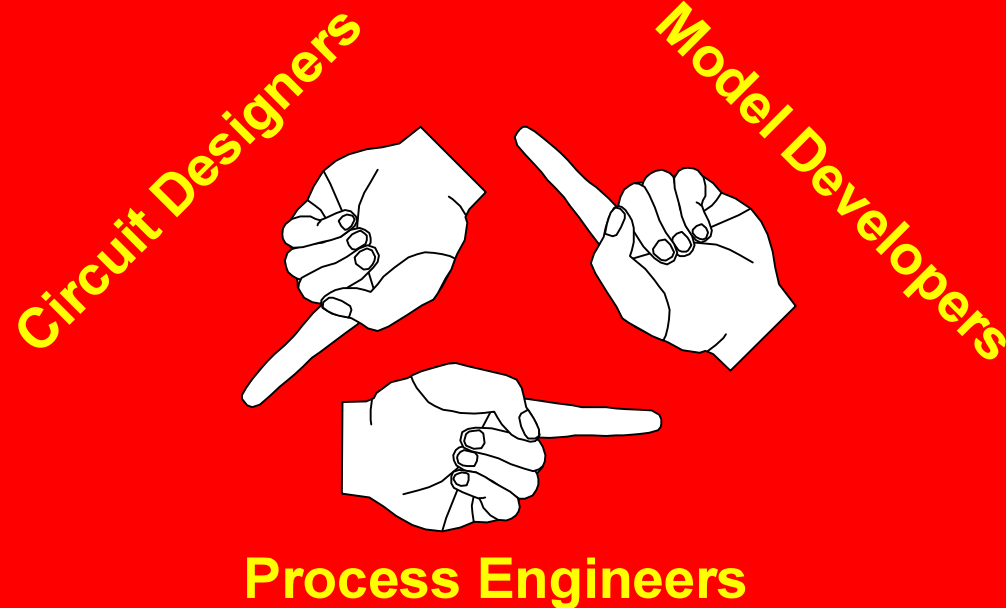
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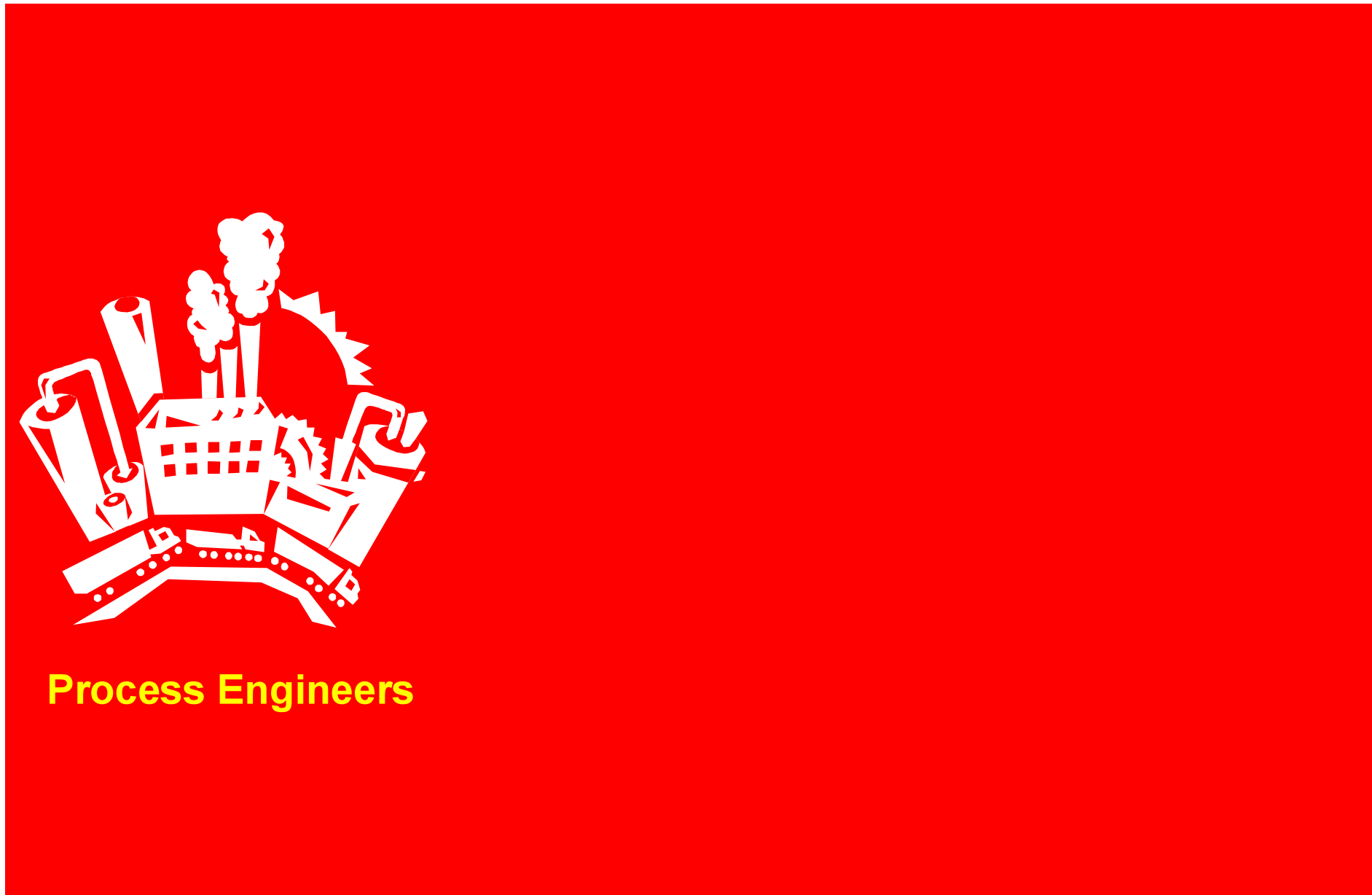


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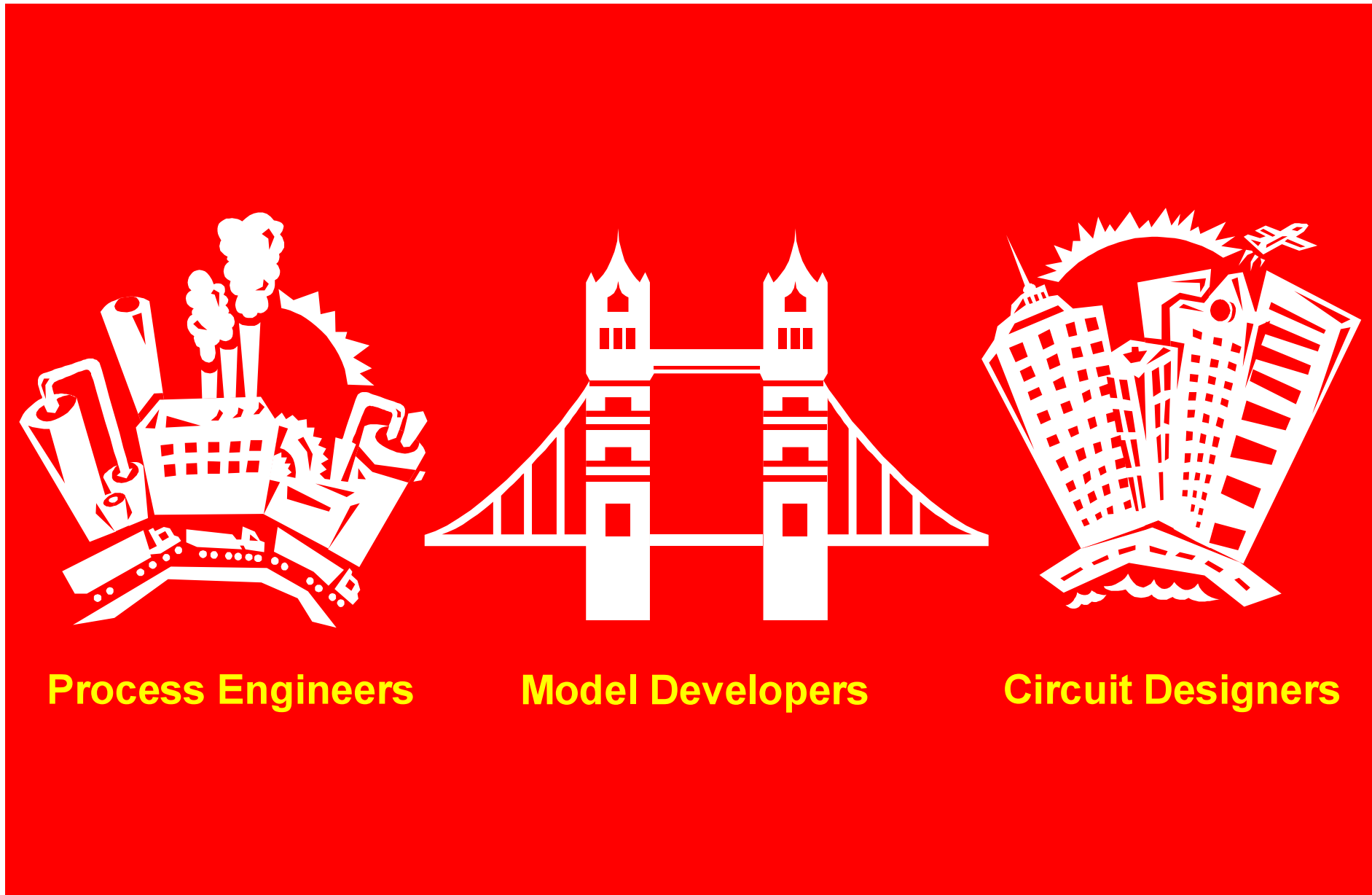




Process Engineers



Circuit Designers



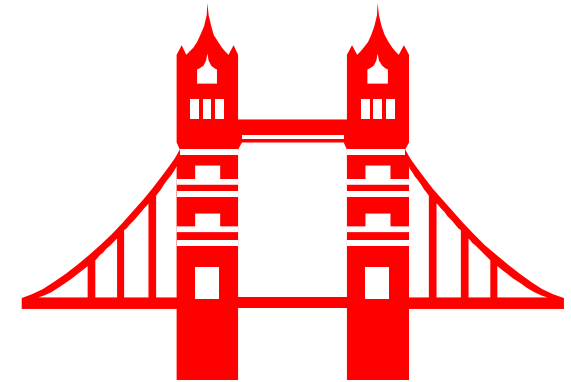
compact model requirements

- all quantities relevant for designers
 - current
 - drain
 - gate
 - conductance
 - transconductance
 - capacitances, i.e. charges
 - noise
 - $1/f$ (or “flicker”) noise
 - thermal
 - high-frequency, e.g. induced gate noise
 - distortion



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 - **capable of mimicking process variations**



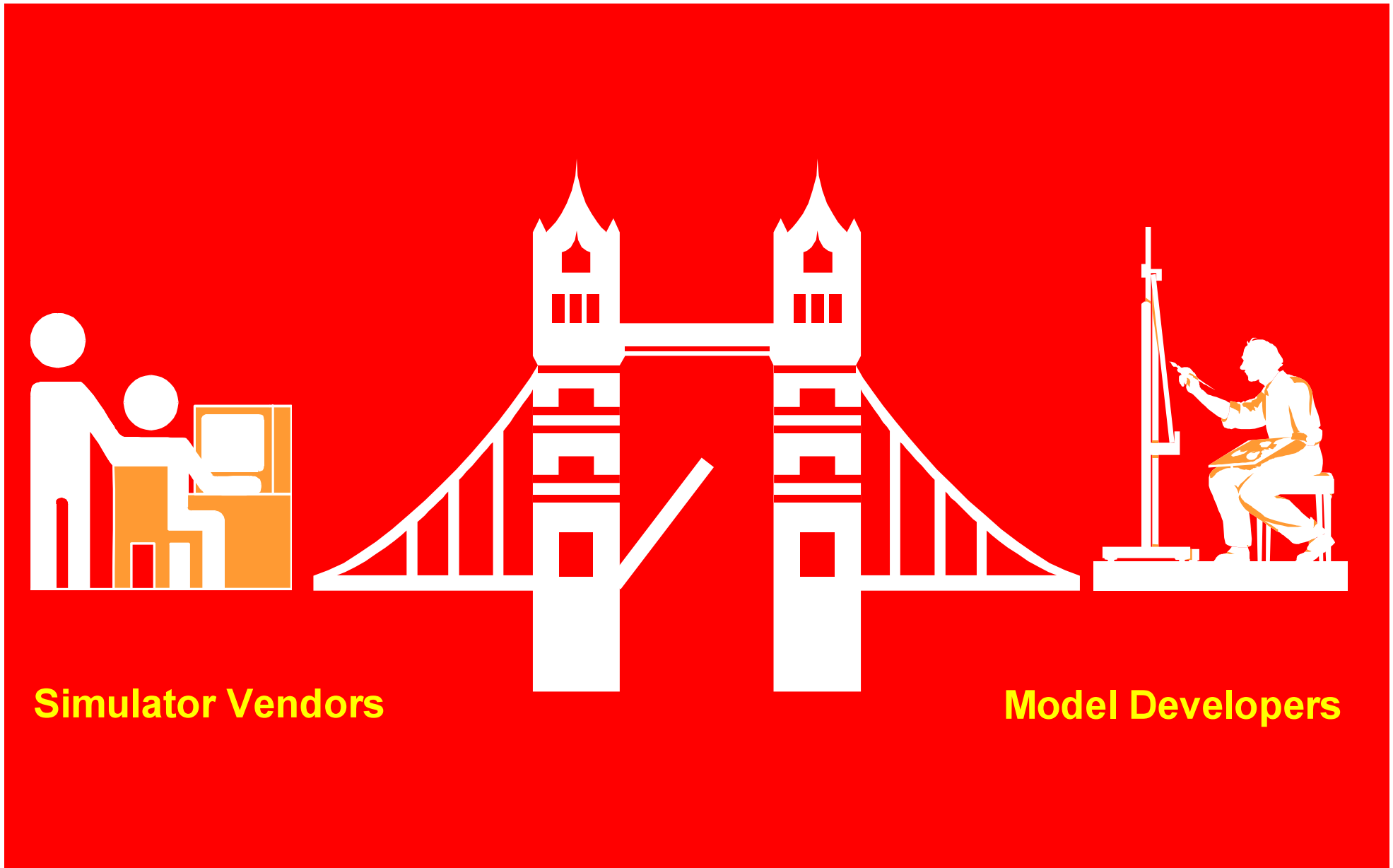
compact model activities at Philips

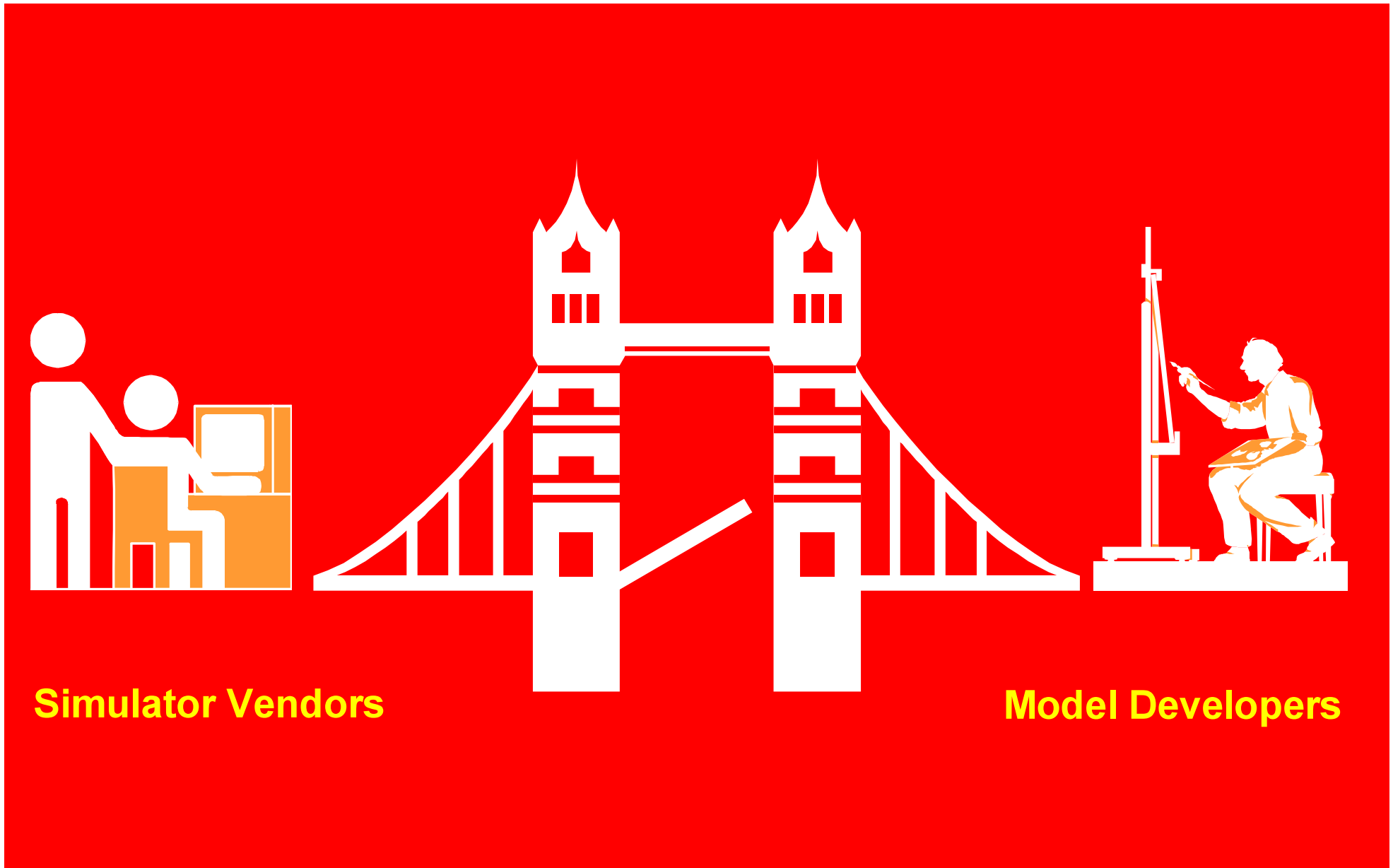
- in-house development at Philips Research
 - CMOS: MOS Model 9, MOS Model 11
 - bipolar: Mextram 503, Modella, Mextram 504
 - LDMOS
 -
- in close contact with
 - designers
 - characterization groups in production centres
 - (in-house) circuit simulator development
- source code and documentation in public domain

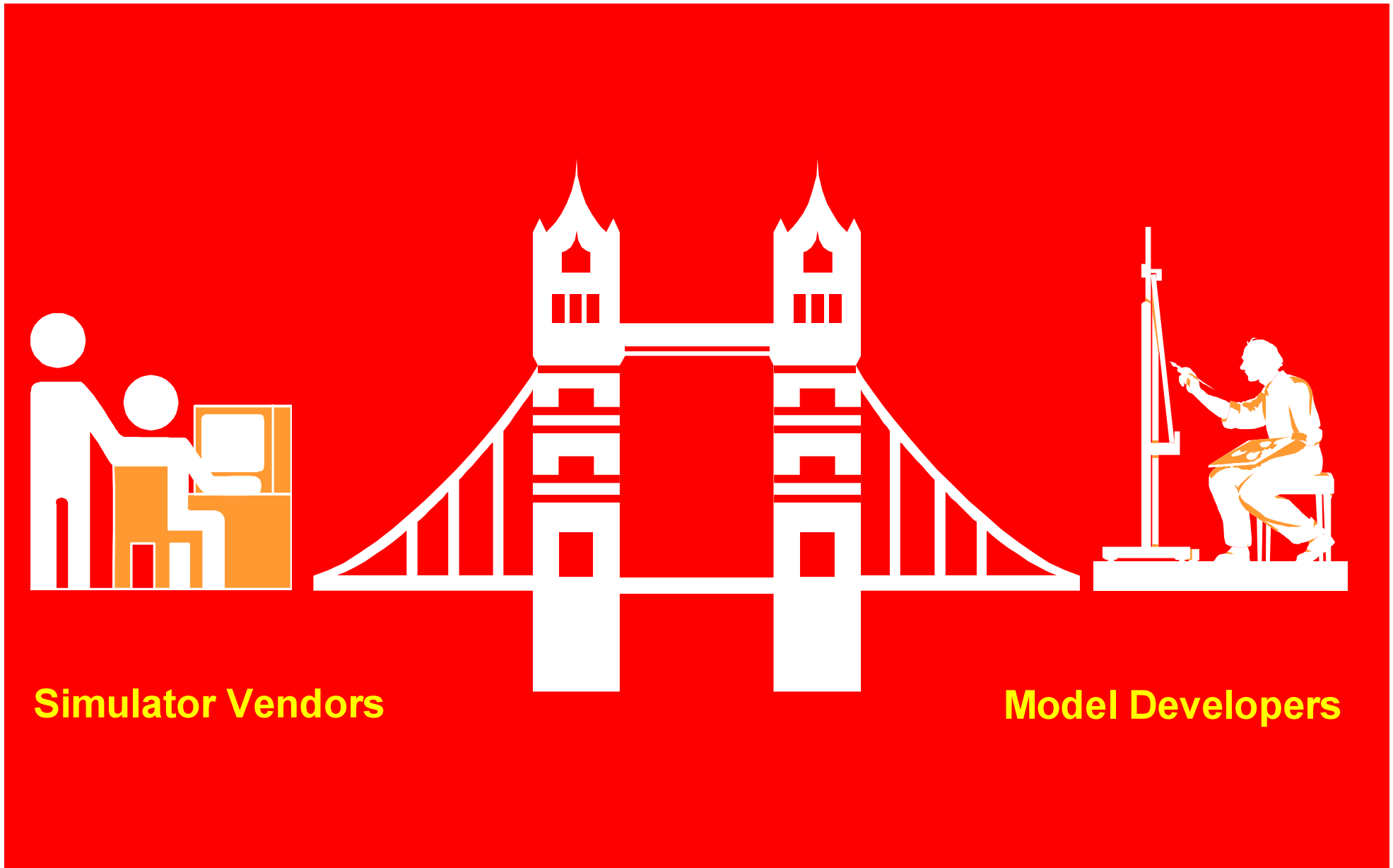
http://www.semiconductors.philips.com/Philips_Models

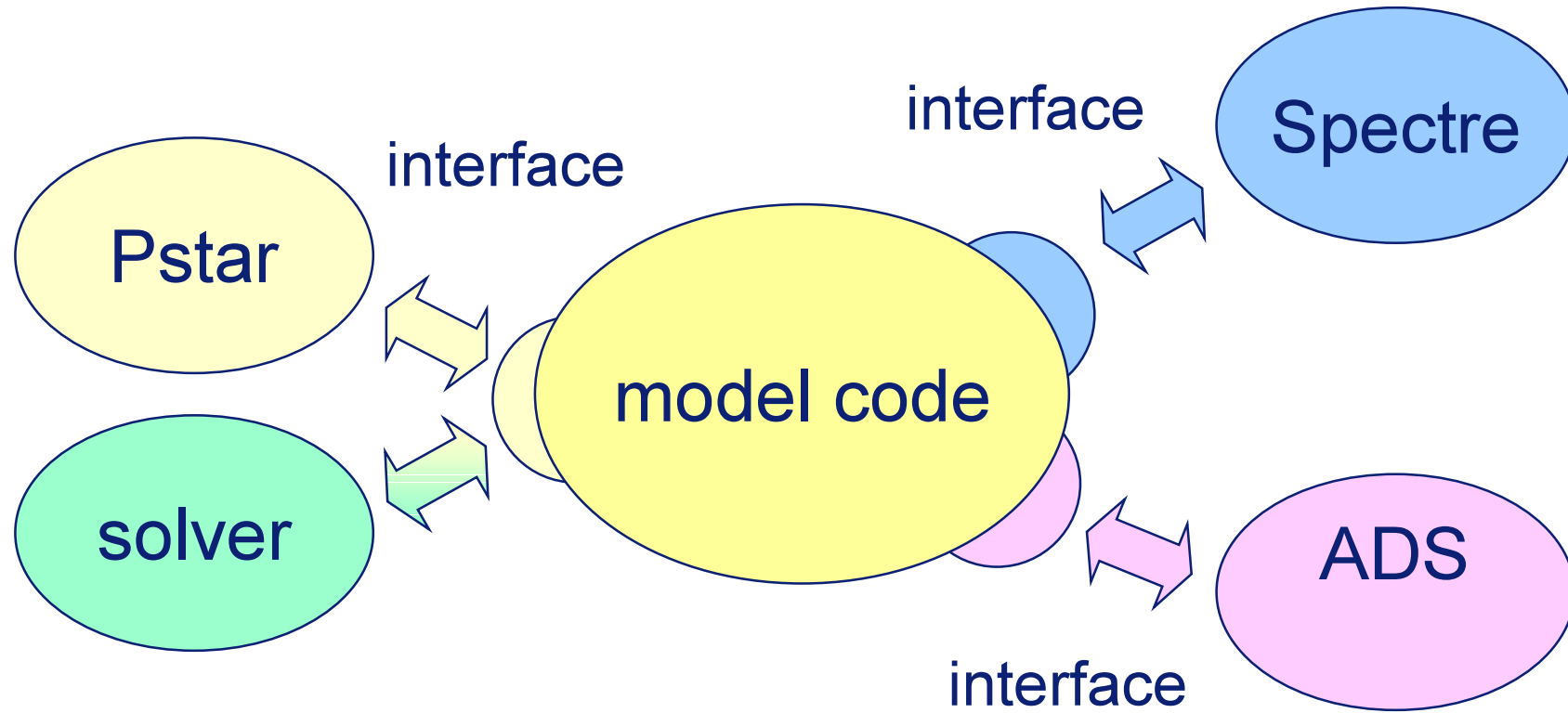
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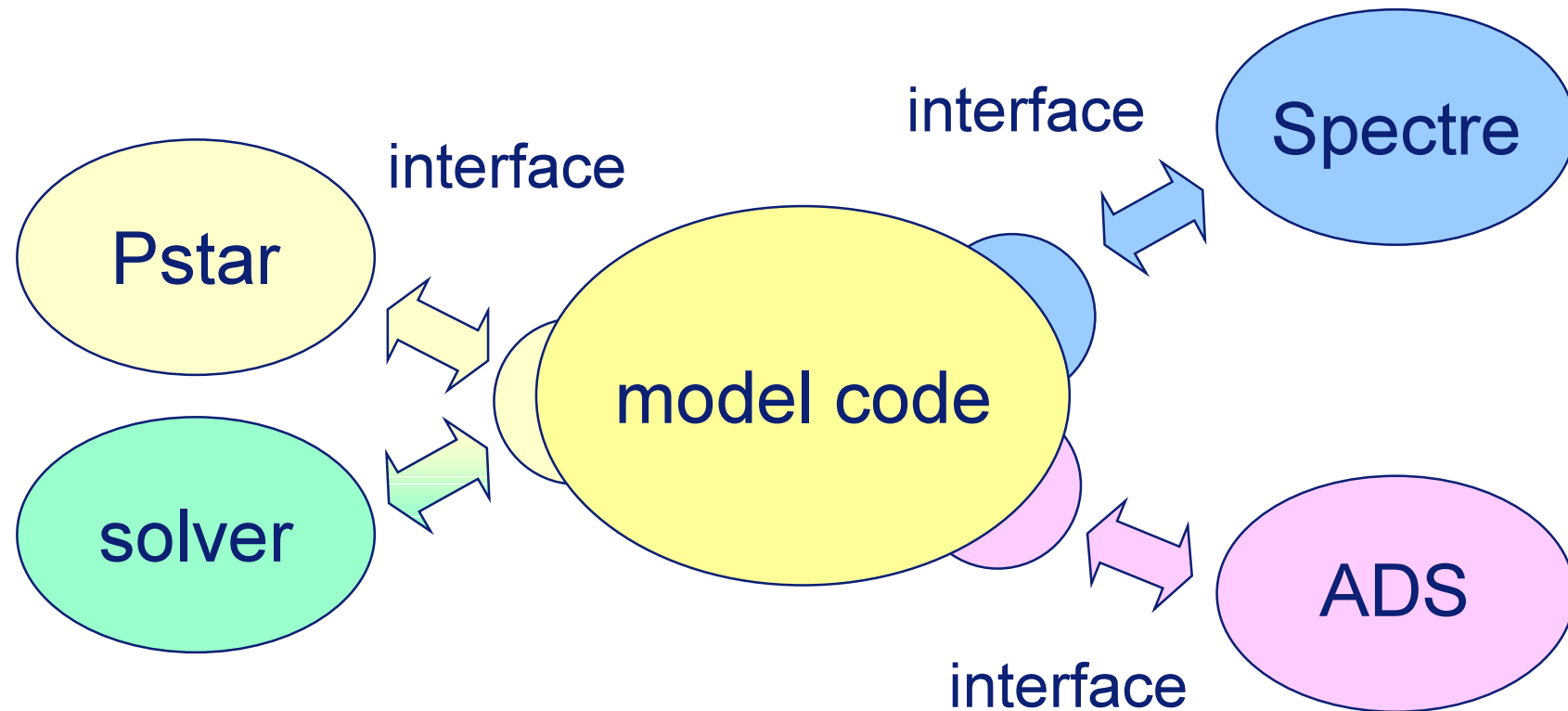
- easy exchange with customers
- implementation in commercial software
- co-operation with third parties on compact modelling
- to raise the bar for standardization candidates
- http://www.semiconductors.philips.com/Philips_Models











approach emerging in public domain

- compact model development and definition in Verilog-A
- "translator" from Verilog-A to C-code

