A Surface-Potential-Based n-MOSFET Gate Tunneling Current Model

Xin Gu, Gennady Gildenblat,
Department of Electrical Engineering
The Pennsylvania State University
Glen Workman, Surya Veeraraghavan
DigitalDNA Laboratories, Motorola
Shye Shapira and Kevin Stiles
Agere Systems

Outline

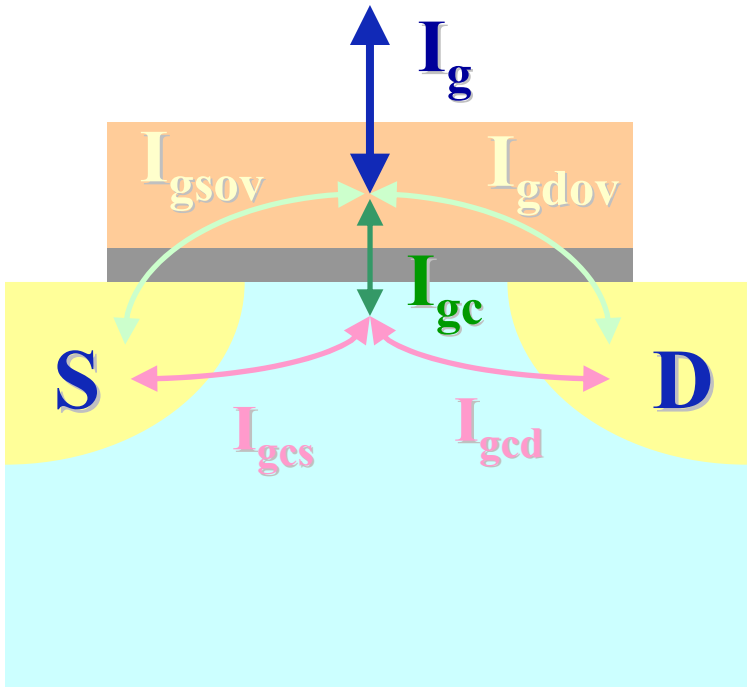
- Introduction
- Tunneling current density
- Gate tunneling current
- Drain bias dependence and partition
- Model Verification
- Conclusions

Introduction – Overview

- Aggressive scaling of t_{ox} (below 30Å) $\Rightarrow$ substantial I_g in MOSFETs
- First principle approach is not suited for compact models
- Most of the existing compact models don't include the physics-based carrier statistics $\Rightarrow$ unphysical results i.e. $I_g \neq 0$ when $V_{gs}=V_{bs}=V_{ds}=0$
- I_g in the overlap regions is significant, requiring the physics-based modeling
- In n-MOSFET, only the tunneling of the electrons in the conduction band needs to be considered

Introduction – SP Gate Current Model

- $I_g = I_{gc} + I_{gsov} + I_{gdov}$; the overlap components are modeled using physics-based approach
- $I_{gc} = I_{gcs} + I_{gcd}$; partition is achieved using a physics-based approach
- The physically correct carrier statistics included in the Esaki-Tsu formula is implemented efficiently
- The same form of model and identical parameters are used in all the three components
- No scaling parameters are required to fit the data



Tunneling Current Density

- Esaki-Tsu formula

$$J_g = J_0 \int D(E) F_s(E) \mathrm{d}E$$

- *D(E)* and *F_s(E)* are the transmission coefficient and the supply function at the given kinetic energy *E*, respectively

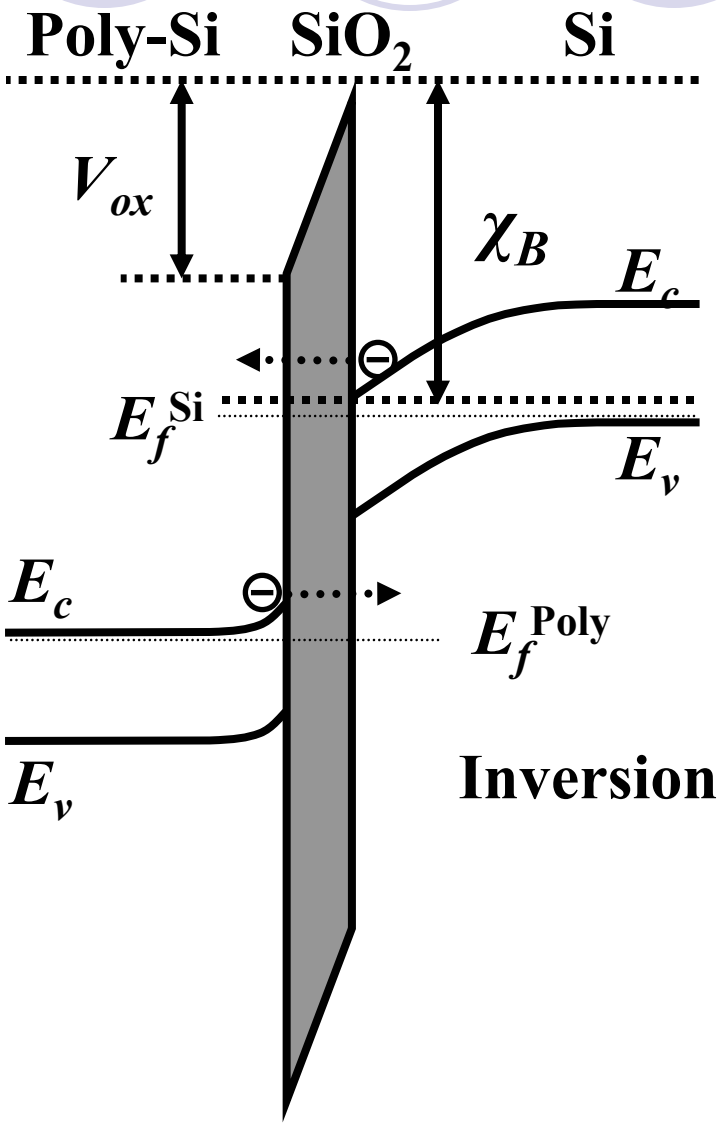
$$F_s = \ln\left(\frac{1+\Delta_{\mathrm{Si}}}{1+\Delta_{\mathrm{Poly}}}\right)$$

$$\Delta_{\mathrm{Si}} = \exp\left[\left(E_f^{\mathrm{Si}} - E\right)/k_B T\right]$$

$$\Delta_{\mathrm{Poly}} = \exp\left[\left(E_f^{\mathrm{Poly}} - E\right)/k_B T\right]$$

- At equilibrium

$$E_f^{\mathrm{Si}} = E_f^{\mathrm{Poly}} \Rightarrow F_s = 0 \Rightarrow J_g = 0$$

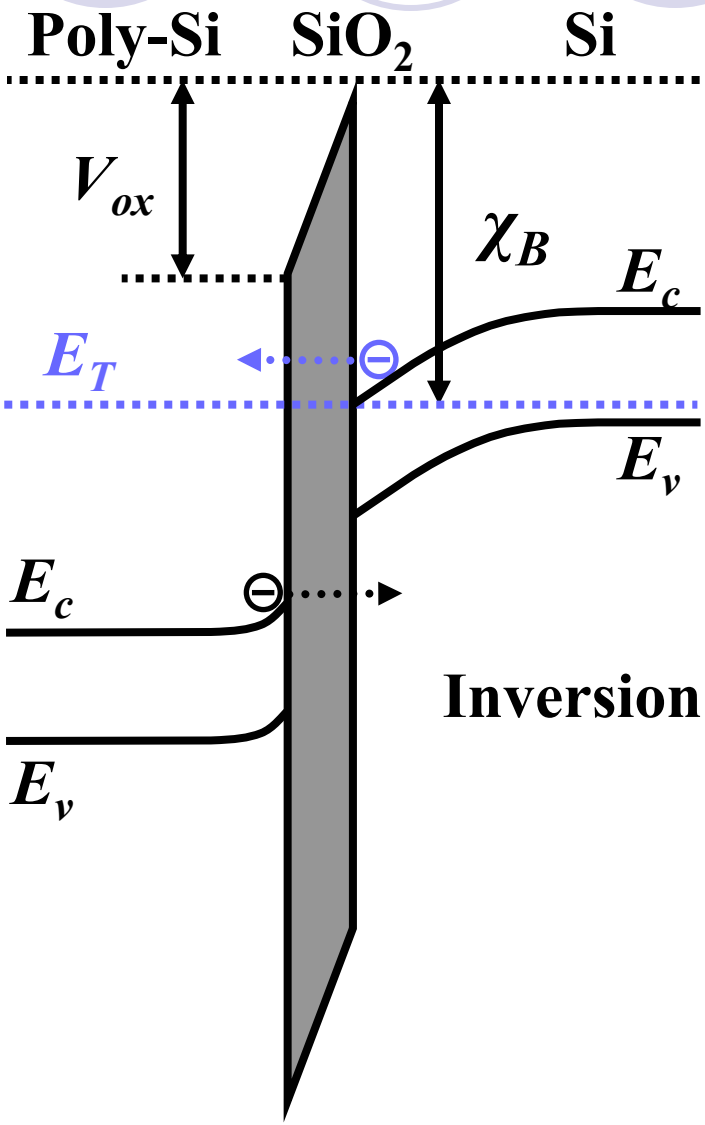


Tunneling Current Density (II)

- Numerical integration in the Esaki-Tsu formula prohibits it to be included in compact models
- Assuming that all the tunneling takes place at a constant energy, E_T, yields an analytical expression

$$J_g = J_0 D(E_T) F_s(E_T)$$

- The assumption reflects the fact that the most of electrons only occupy the states close to the band edge



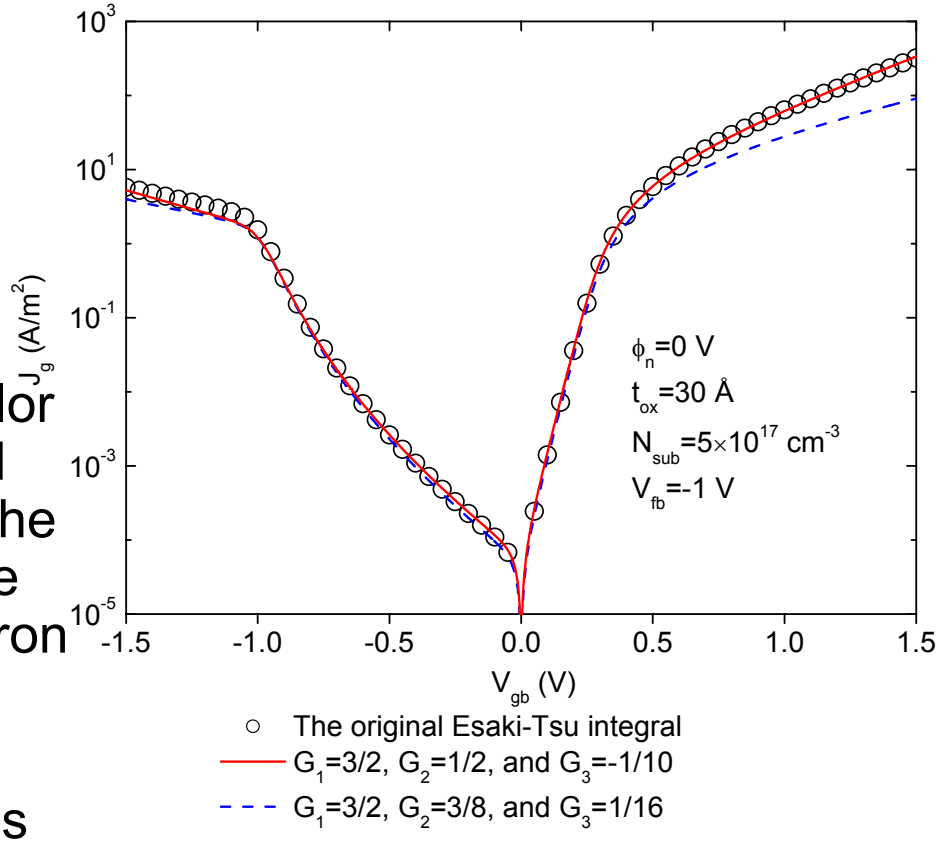
Tunneling Current Density (III)

- In WKB approximation,

$$D(E_T) = \exp\left[B\frac{\left(1-|V_{ox}|/\chi_B\right)^{3/2}-1}{|V_{ox}|/\chi_B}\right]$$

$$\cong \exp\left\{-B\left[G_1 + G_2\frac{|V_{ox}|}{\chi_B} + G_3\left(\frac{|V_{ox}|}{\chi_B}\right)^2\right]\right\}$$

- Ideally, G_1, G_2, and G_3 can be obtained by the second order Taylor expansion; here they are changed into model parameters to absorb the numerical difference as well as the uncertainties of the effective electron mass, etc.
- Comparison reveals that the approximation faithfully reproduces the original integral

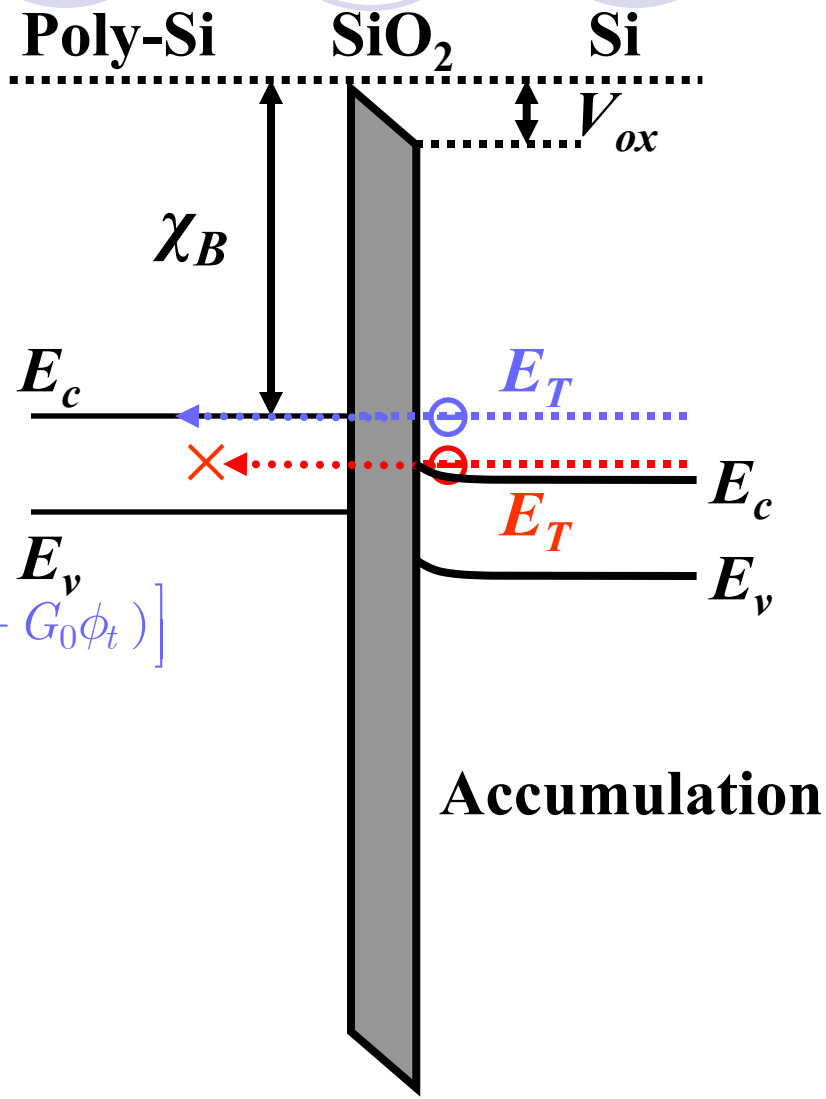


Tunneling Current Density (IV)

- When $V_{gb} > V_{fb}$,
  E_T = the conduction band edge in the Si surface
- When $V_{gb} \leq V_{fb}$,
  E_T = the conduction band edge in the Poly surface
- Smoothing function is used to provide the asymptotic transition

$$E_T = E_{Cs}^{\mathrm{Si}} + \frac{1}{2}\left[\sqrt{(V_{ox} - G_0\phi_t)^2 + 10^{-3}} - (V_{ox} - G_0\phi_t)\right]$$

- G_0 is used to mode the band misalignment between the polysilicon and silicon



Gate Tunneling Current – Overlap

- J_g in the overlap region is uniform

$$I_{gsov} = WL_{ov}J_g\left(V_{gs}\right)$$

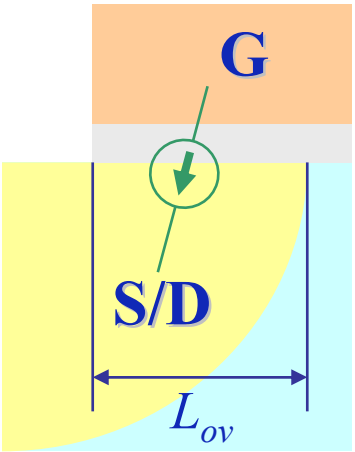
$$I_{gdov} = WL_{ov}J_g\left(V_{gd}\right)$$

- In scaled devices, L_{ov} is comparable to L_{eff}

  $\Longrightarrow$ significant overlap component

- In large devices, for small gate biases, V_{ox} in the overlap region is larger than in the channel region

  $\Longrightarrow$ significant overlap component



Gate Tunneling Current – Channel

- V_{ds} induces the position dependence of J_g along the channel

$$I_{gc} = W\int_0^L J_g(\mathrm{y})\mathrm{d}y; \qquad J_g(y) = J_0 F_s(y) D(\phi_m)\exp\left(-\frac{u}{u_0}\right)$$

$$\phi_m = (\phi_{ss} + \phi_{ss})/2;\ u = \phi_s - \phi_m; u_0 = \frac{\chi_B}{B[G_2(1 - 2G_3|Vox|/\chi_B)]}$$

- The integrals are evaluated analytically using the symmetric linearization method (Gildenblat and Chen WCM2002)

$$\mathrm{d}y/\mathrm{d}u = L(H-u)/H\phi$$

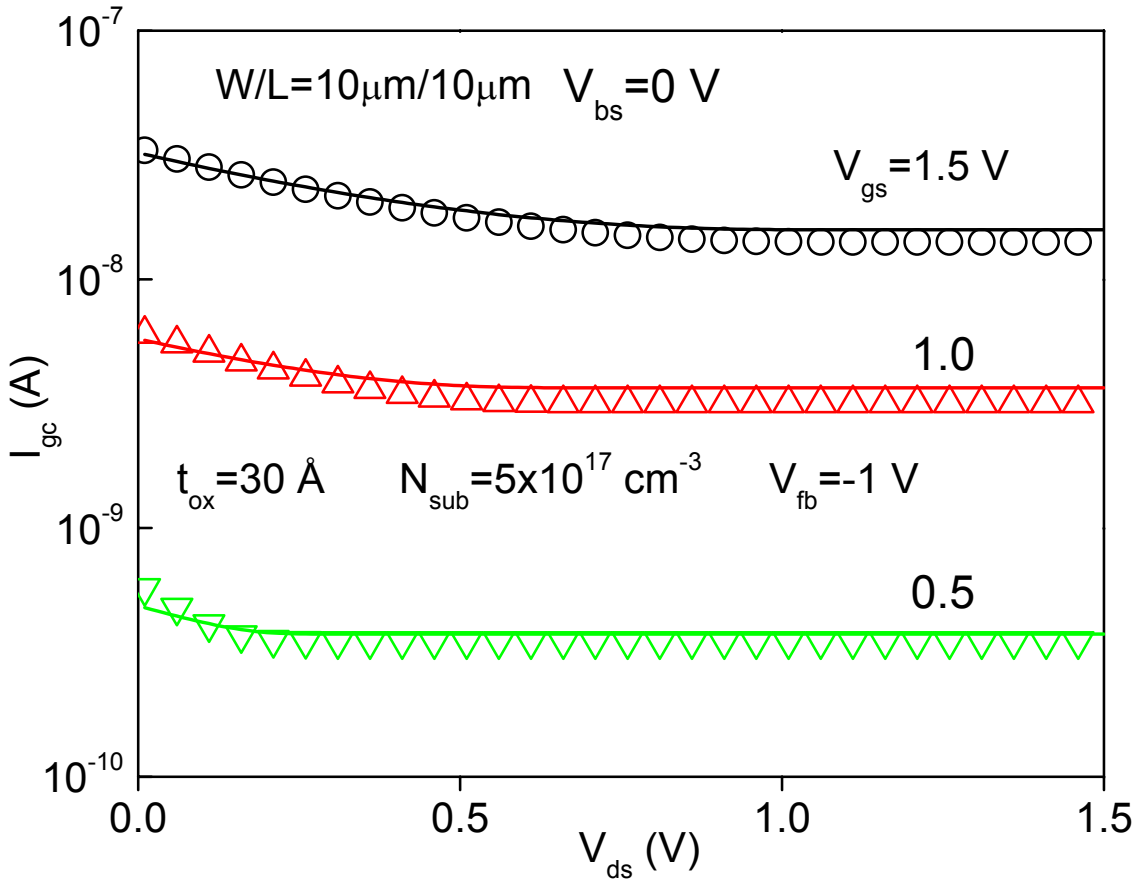
$$L: \text{channel length};\ H: \text{constant along the channel}; \phi = \phi_{sd} - \phi_{ss}$$

$$I_{gc} = I_{gc0}[(1-b)\sinh(x)/x + b\cosh(x)]$$

$$I_{gc0} = I_{gc}\big|_{V_{ds}=0}; x = \phi/2u_0; b = u_0/H$$

Shi *et al.* IEDM 2001 and van Langevelde *et al.* IEDM 2001

Gate Tunneling Current – Channel



Symbols: numerical integration
Solid Lines: analytical result

Gate Tunneling Current – Partition

- Partition of I_{gc} into the source and drain components, I_{gcs} and I_{gcd}, is crucial to compact models

$$I_{gd} = W\int_0^L J_g(y)\frac{y}{L}\mathrm{d}y; \qquad I_{gcs} = I_{gc} - I_{gcd}$$

- Repeating the algebra yields

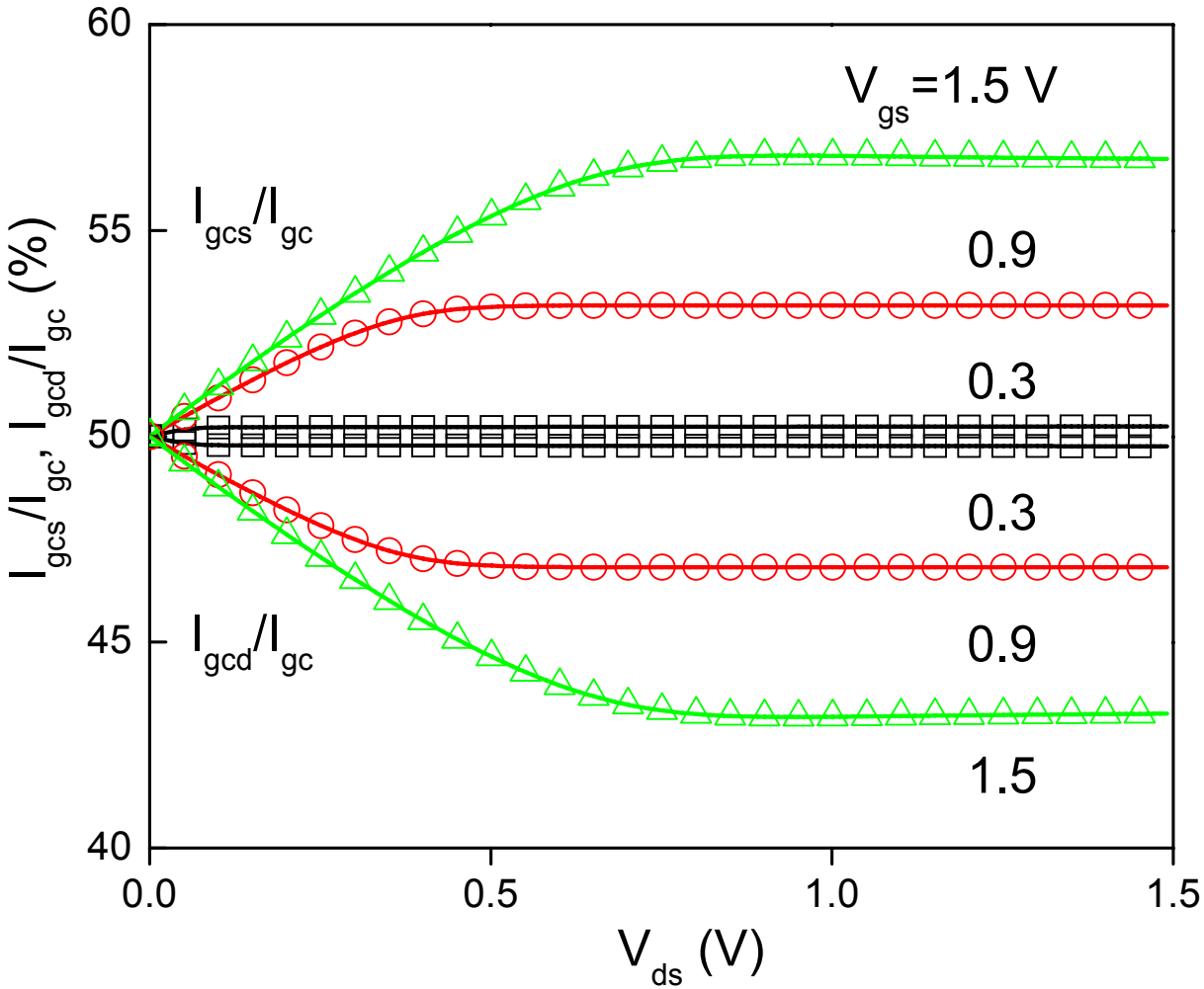
$$I_{gcd} = \frac{I_{gc}}{2} - \frac{I_{gc0}}{2}\frac{\sinh(x)}{x}\left\{\left(1-3b+3b^2\right)x - b(1-b)\left[\coth(x) - \frac{1}{x}\right]\right\}$$

- When $V_{ds} \rightarrow 0$ or in subthreshold region,

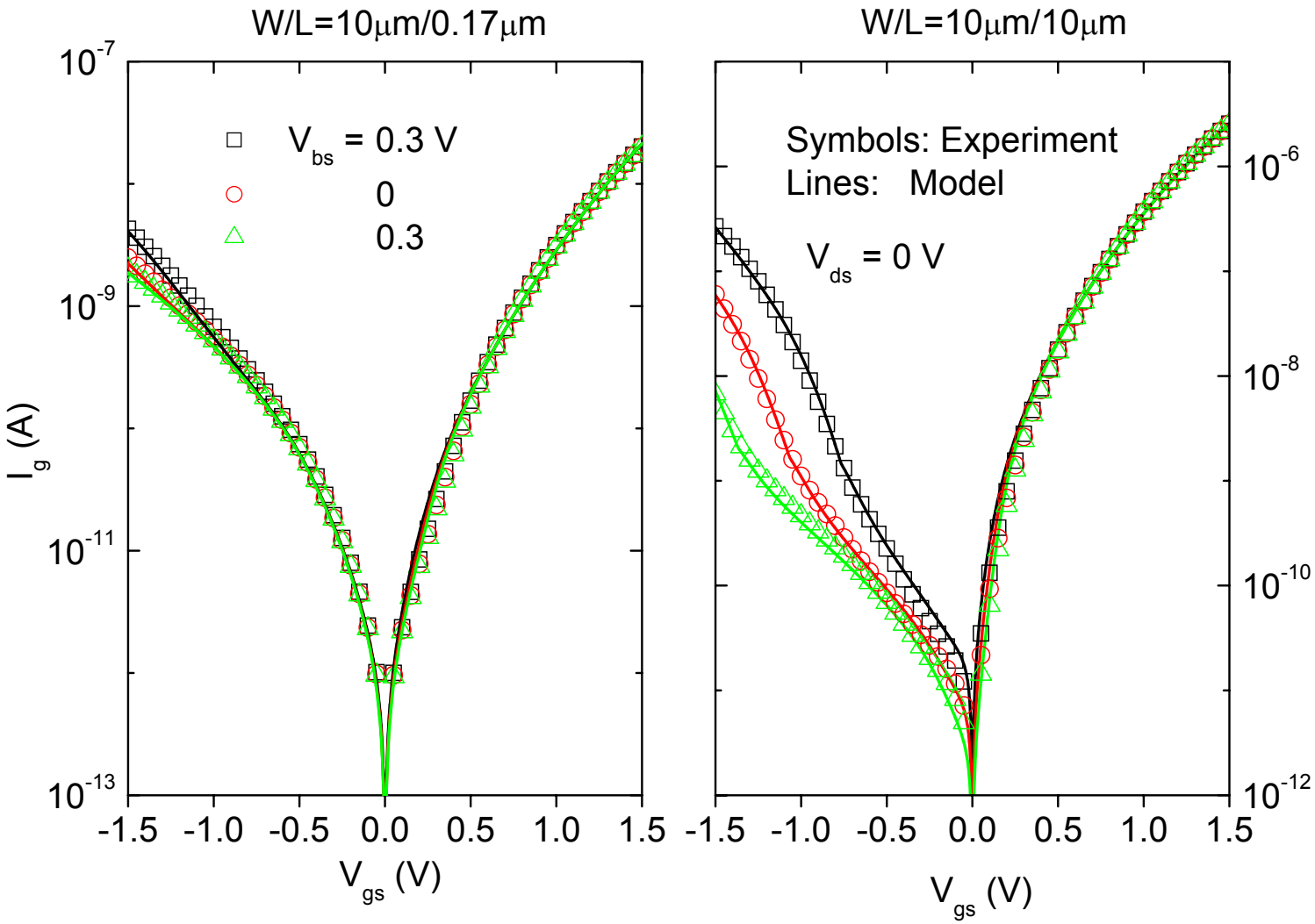
$$I_{gcd} \rightarrow \frac{I_{gc}}{2}$$

Shi *et al.* IEDM 2001 and van Langevelde *et al.* IEDM 2001

Gate Tunneling Current – Partition



Model Verification



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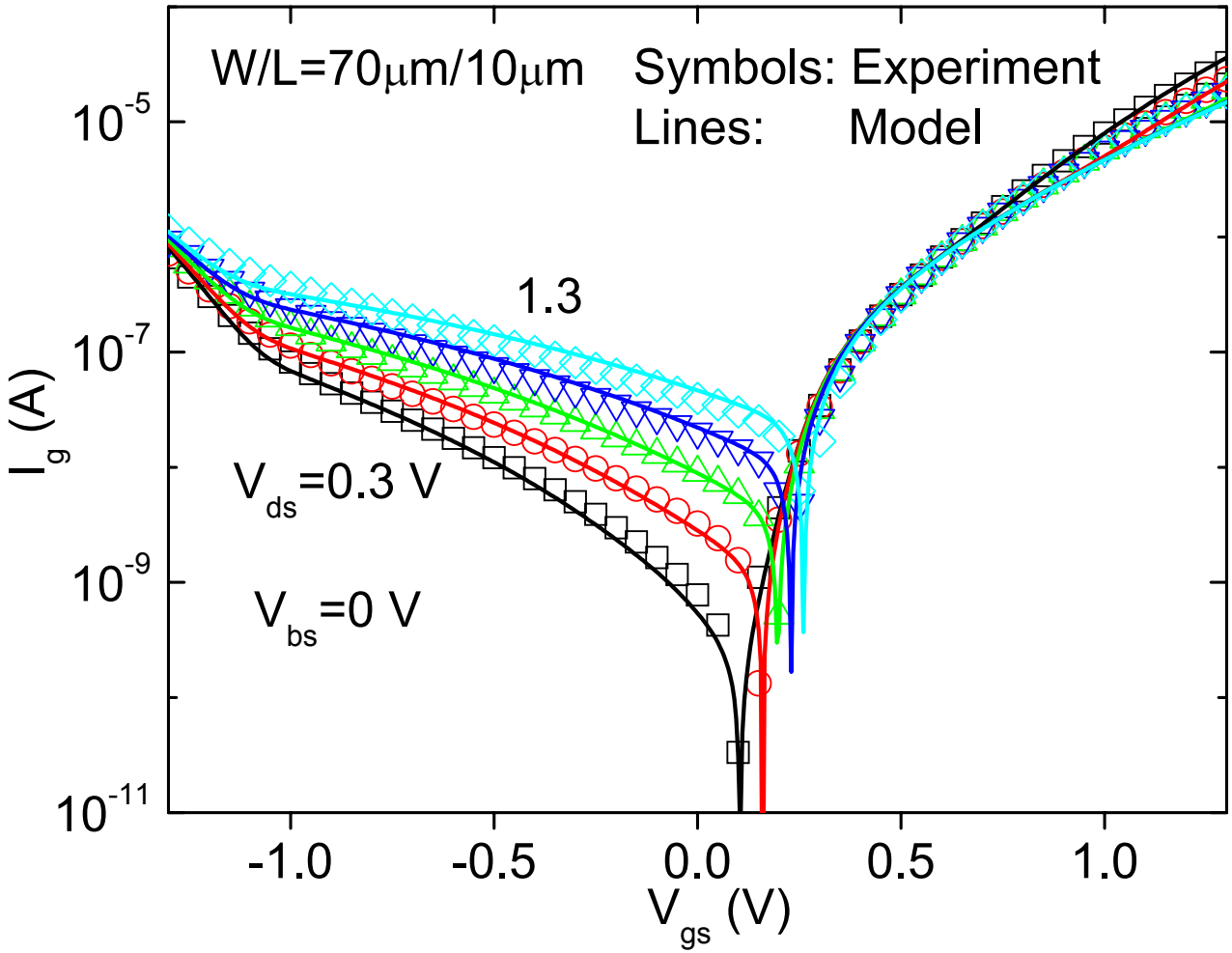

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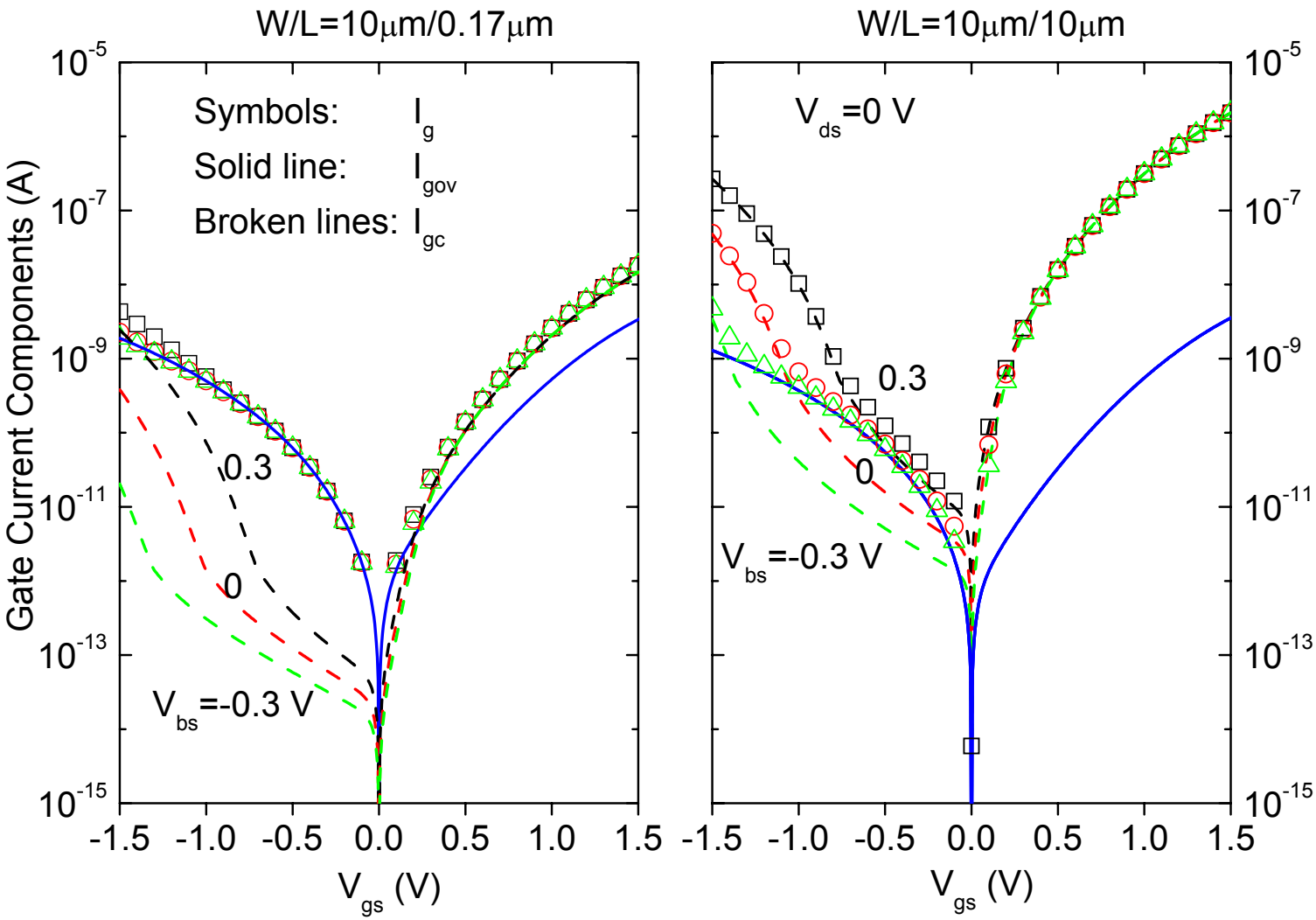

Conclusions – SP Gate Current Model

- Using surface-potential-based approach increases the physical content of the gate tunneling current model
- Physics-based carrier statistics are included efficiently, leading to physically correct results
- Overlap components are modeled sophisticatedly
- Drain bias dependence and source-drain partition of the channel component are accounted for using a physics-based approach
- All the three components have the same form of model and identical parameters
- Bias and geometry dependence of experimental data are reproduced without using scaling parameters

more information about SP model – gildenblat@psu.edu