

A Surface-Potential-Based Extrinsic Compact MOSFET Model

Xin Gu, Gennady Gildenblat,

*Department of Electrical Engineering
The Pennsylvania State University*

Glen Workman, Surya Veeraraghavan

DigitalDNA Laboratories, Motorola


Shye Shapira and Kevin Stiles

Agere Systems



Outline

- Introduction
- Streamlined analytical approximation of surface potential (ϕ_s)
- Overlap capacitance model
- Gate tunneling current model
- Substrate current model
- Noise sources
- Conclusions



Introduction – Overview

- Next generation compact MOSFET models – ϕ_s -based models
- Advantages of ϕ_s -based models over threshold-voltage-based models:
 - Increased physical content
 - Correct asymptotical behavior
 - Fewer model parameters and better accuracy
- Computational efficiency – not a problem any more! Accurate analytical approximations of ϕ_s have been worked out

Introduction – SP Model Structure

Core Model

Analytical ϕ_s Approximation

QM, Poly and (R)SCE effects

Lateral Gradient Factor

Single Expression for I_d

Consistent Intrinsic Charge



Extrinsic Model

Streamlined ϕ_s Approximation

Overlap Capacitance Model

Substrate Current Model

Gate Current Model

Noise Sources

Junctions

Gate and Substrate Resistances

Enhanced SP Model

Scattering Matrix Method

NQS version

Novel Devices

Streamlined Approximation of ϕ_s (I)

- Availability of ϕ_s in the overlap regions is crucial for the accurate modeling of the overlap capacitance and the gate tunneling current
- The minority charge in the overlap region can be neglected as a result of the high doping concentration

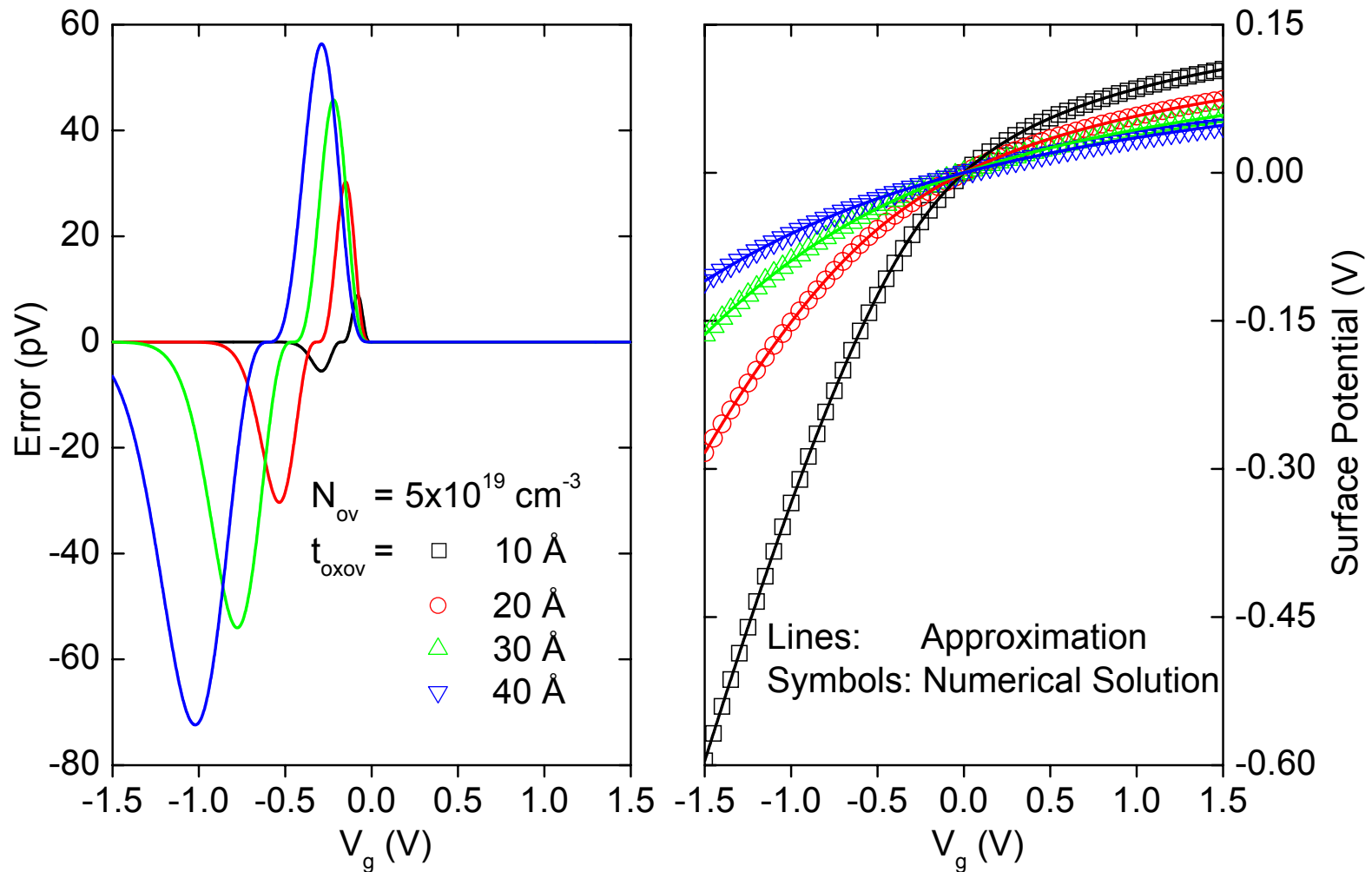
$$V_g - \phi_s = \gamma_{ov} \sqrt{\phi_t \exp(-\phi_s/\phi_t) + \phi_s - \phi_t}$$

- A simpler and more efficient approximation of ϕ_s has been developed for the overlap regions

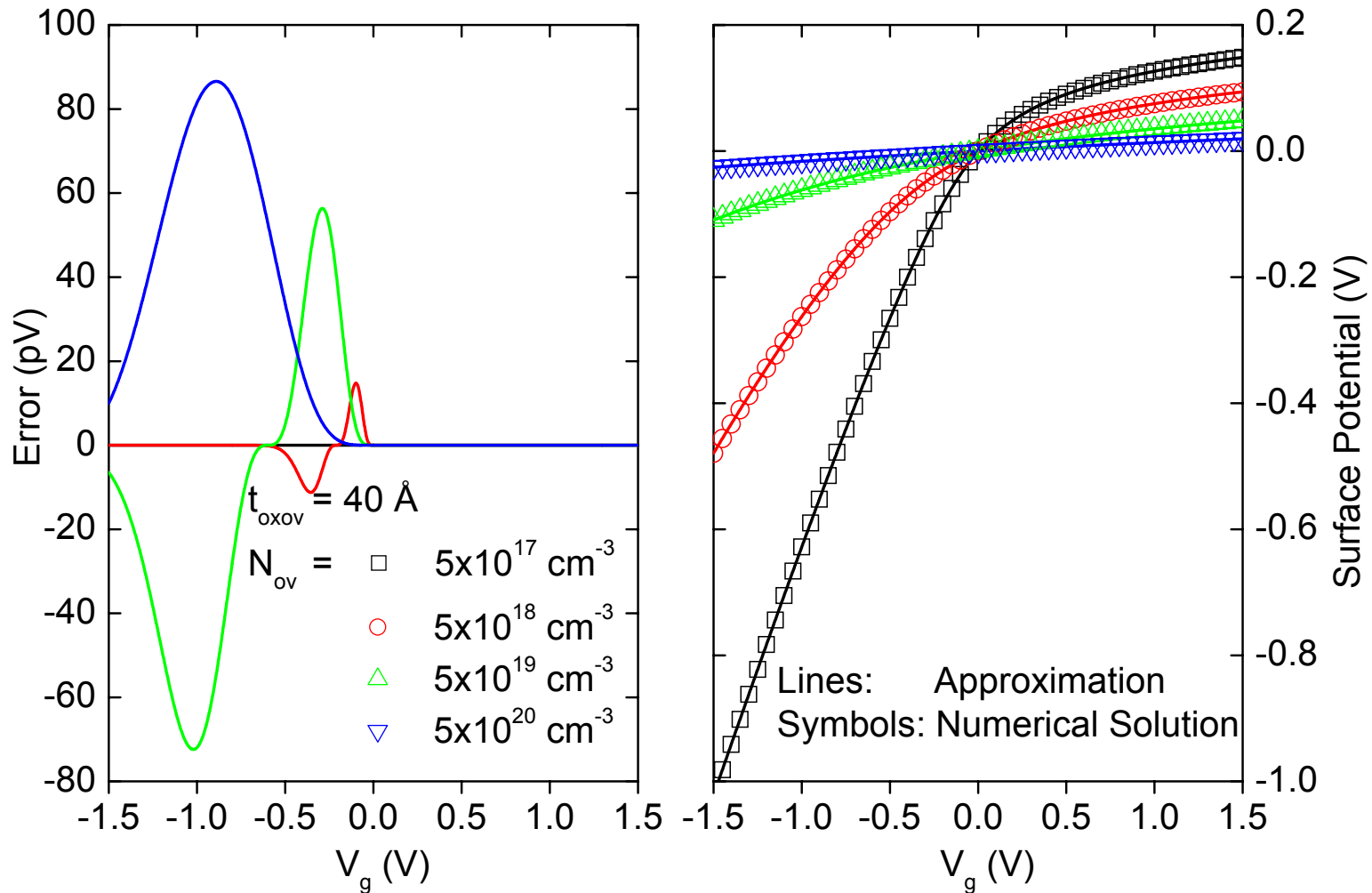
$$\phi_s = f(V_g)$$

- ϕ_s has the accuracy better than 1 nV in any case and excellent continuity

Streamlined Approximation of ϕ_s (II)

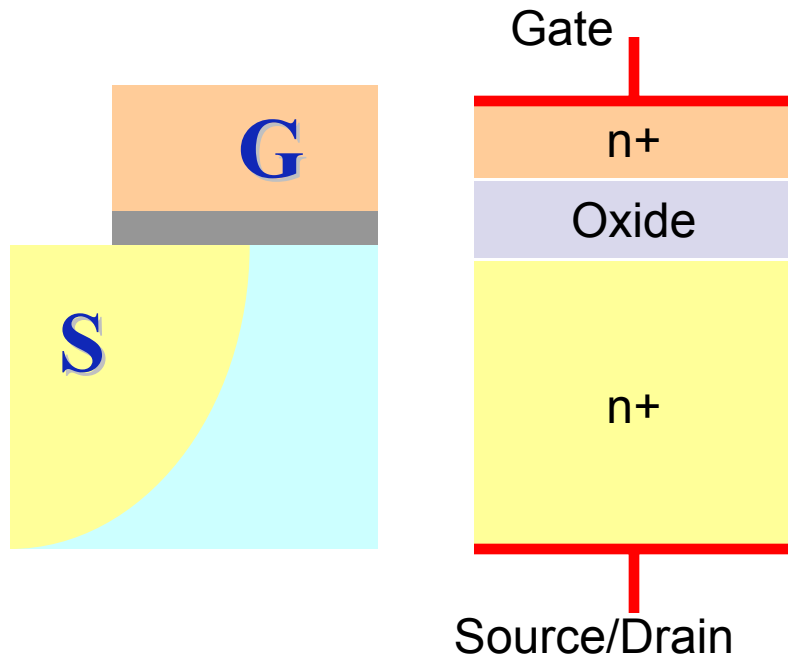


Streamlined Approximation of ϕ_s (III)



Overlap Capacitance (C_{ov}) Model

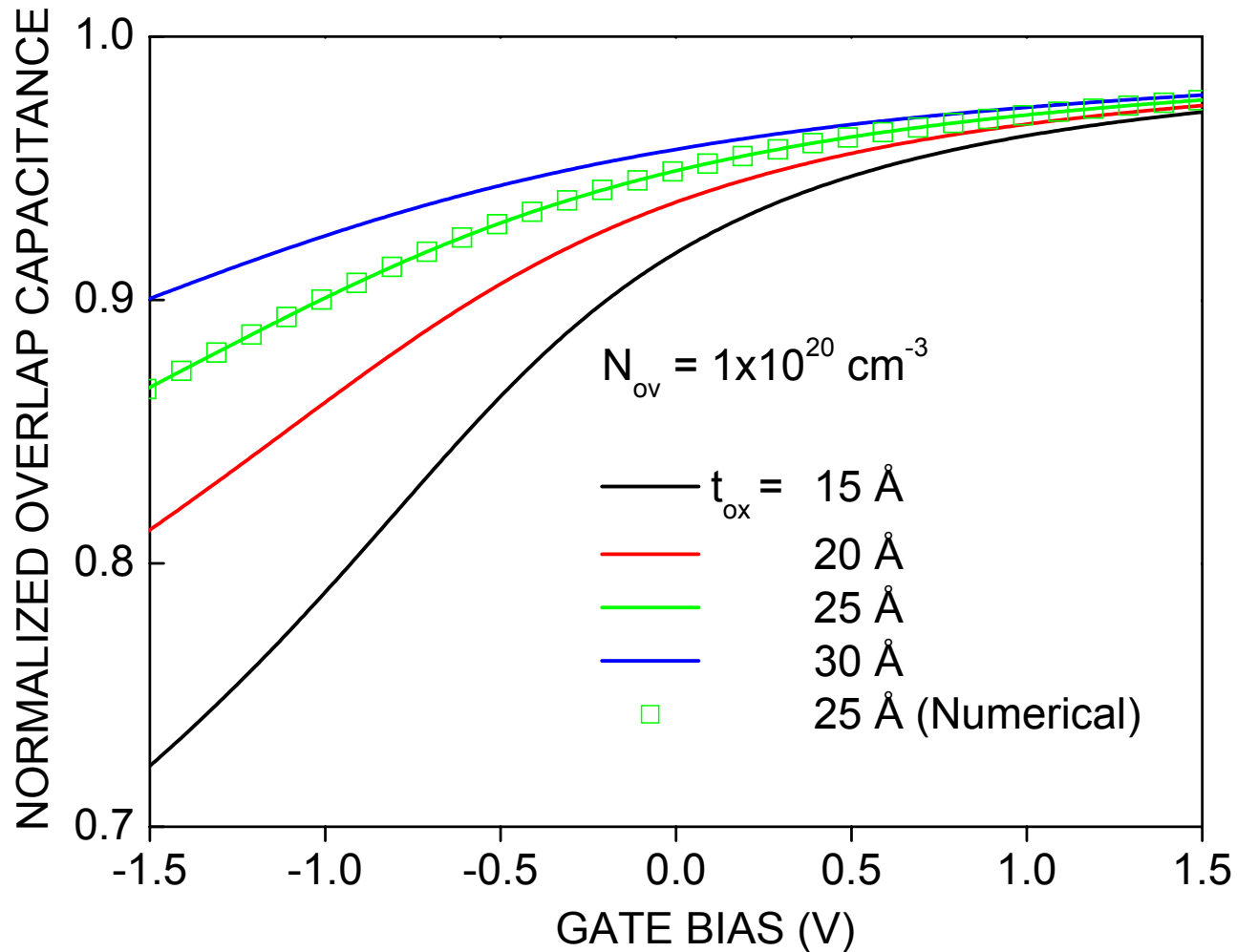
- $L_{ov}/L_g \uparrow$ requires physically-based modeling of the overlap regions for scaled devices
- Conventional models either neglect the bias dependence of C_{ov} or rely on the smoothing function to fit data
- **SP** models the overlap region as MOS capacitor



$$Q_{ov} = WL_{ov}C_{oxov}(V_g - \phi_{ov})$$

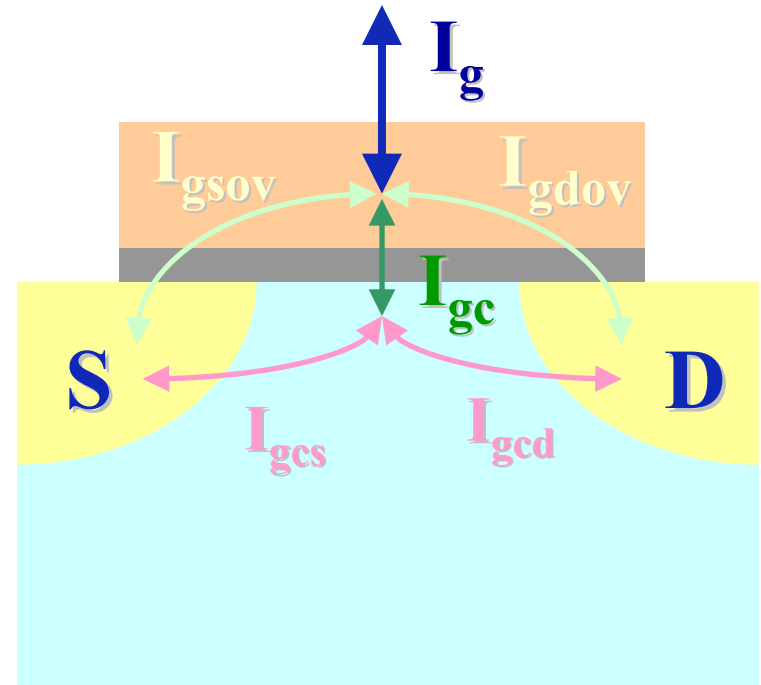
$$C_{ov} = dQ_{ov}/dV_g$$

Overlap Capacitance (C_{ov}) Model (II)



Gate Tunneling Current (I_g) Model

- Aggressive scaling of $t_{ox} \Rightarrow$ substantial I_g
- $I_g = I_{gc} + I_{gsov} + I_{gdov}$; the overlap component is modeled physically
- $I_{gc} = I_{gcs} + I_{gcd}$; partition is achieved using a physics-based approach
- The physically correct carrier statistics included in the Esaki-Tsu formula is implemented efficiently
- The same form of model and identical parameters are used in all the three components
- No scaling parameters are required to fit the data



Gate Tunneling Current Model (II)

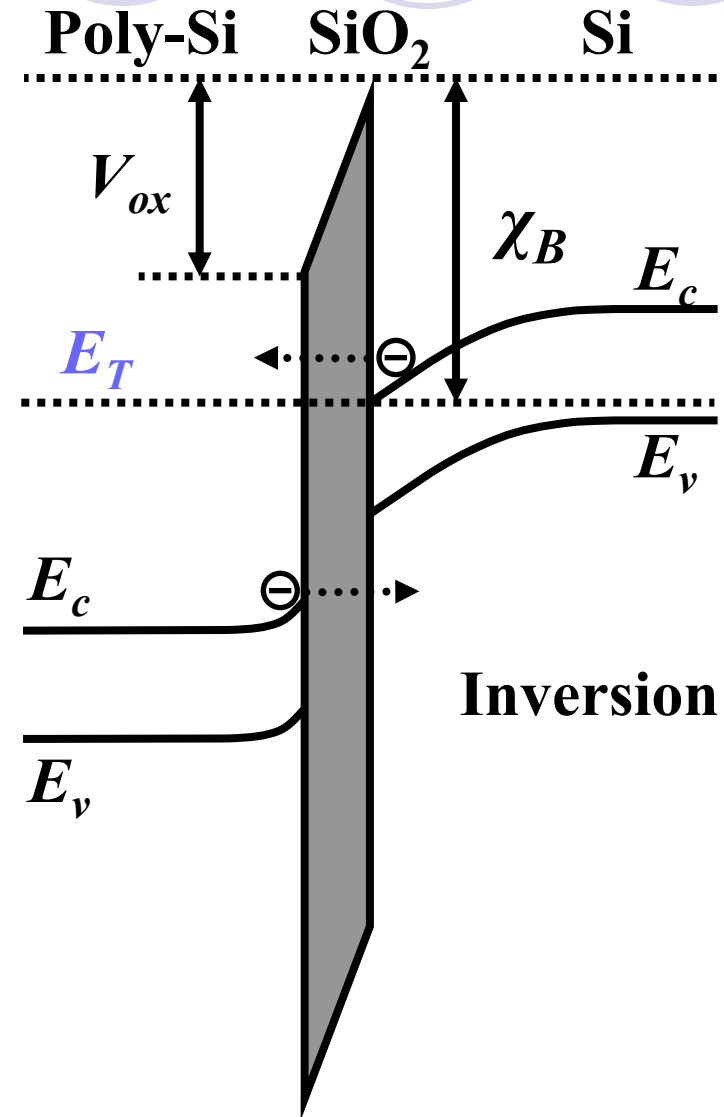
- For each component of I_g , the current density

$$J_g = J_0 \int D(E) F_s(E) dE$$

- In order to obviate the need to numerical integration, it is assumed that the tunneling only takes place at a constant energy – the conduction band edge

$$J_g = J_0 D(E_T) F_s(E_T)$$

- The numerical difference is absorbed by model parameters



Gate Tunneling Current Model (III)

Transmission Coefficient:

$$D(E_T) = \exp \left[B \frac{\left(1 - |V_{ox}|/\chi_B\right)^{3/2} - 1}{|V_{ox}|/\chi_B} \right]$$

$$\cong \exp \left\{ -B \left[G_1 + G_2 \frac{|V_{ox}|}{\chi_B} + G_3 \left(\frac{|V_{ox}|}{\chi_B} \right)^2 \right] \right\}$$

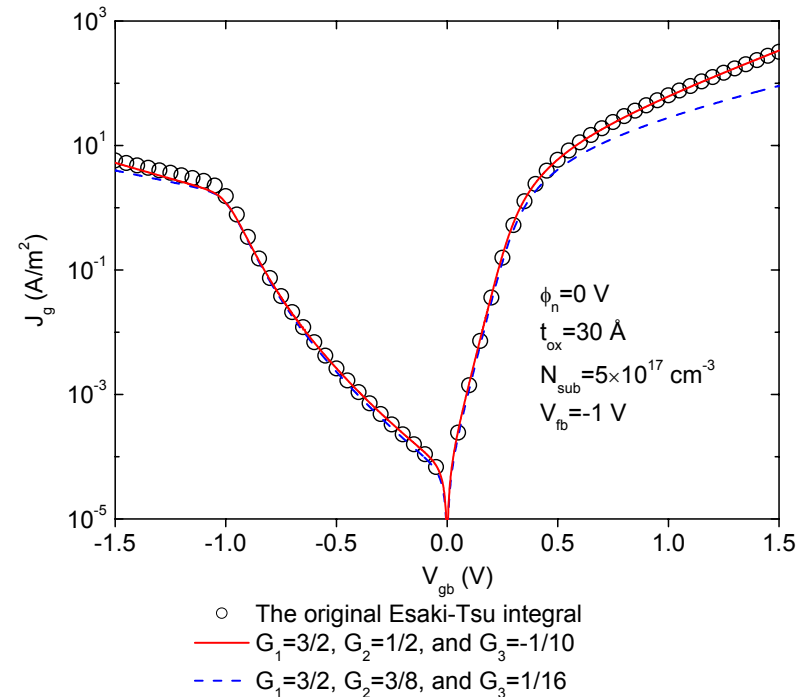
G_1 , G_2 , and G_3 are model parameters

Supply Function:

$$F_s = \ln \frac{1 + \Delta_{Si}}{1 + \Delta_{Si} \exp \left[(\phi_n - V_{gb})/\phi_t \right]}$$

$$\Delta_{Si} = \exp \left[(\phi_s - \phi_n - \alpha_b)/\phi_t \right]$$

$$\alpha_b = \frac{1}{q} (E_c - E_F)_{\text{bulk Si}}$$



At equilibrium:

$$E_f^{\text{Si}} = E_f^{\text{Poly}} \Rightarrow F_s = 0 \Rightarrow J_g = 0$$

Gate Tunneling Current Model (IV)

$$I_{gs\text{ov}} = WL_{\text{ov}}J_g(V_{gs})$$

- I_g in the overlap regions:

$$I_{gd\text{ov}} = WL_{\text{ov}}J_g(V_{gd})$$

- I_g in the channel region:

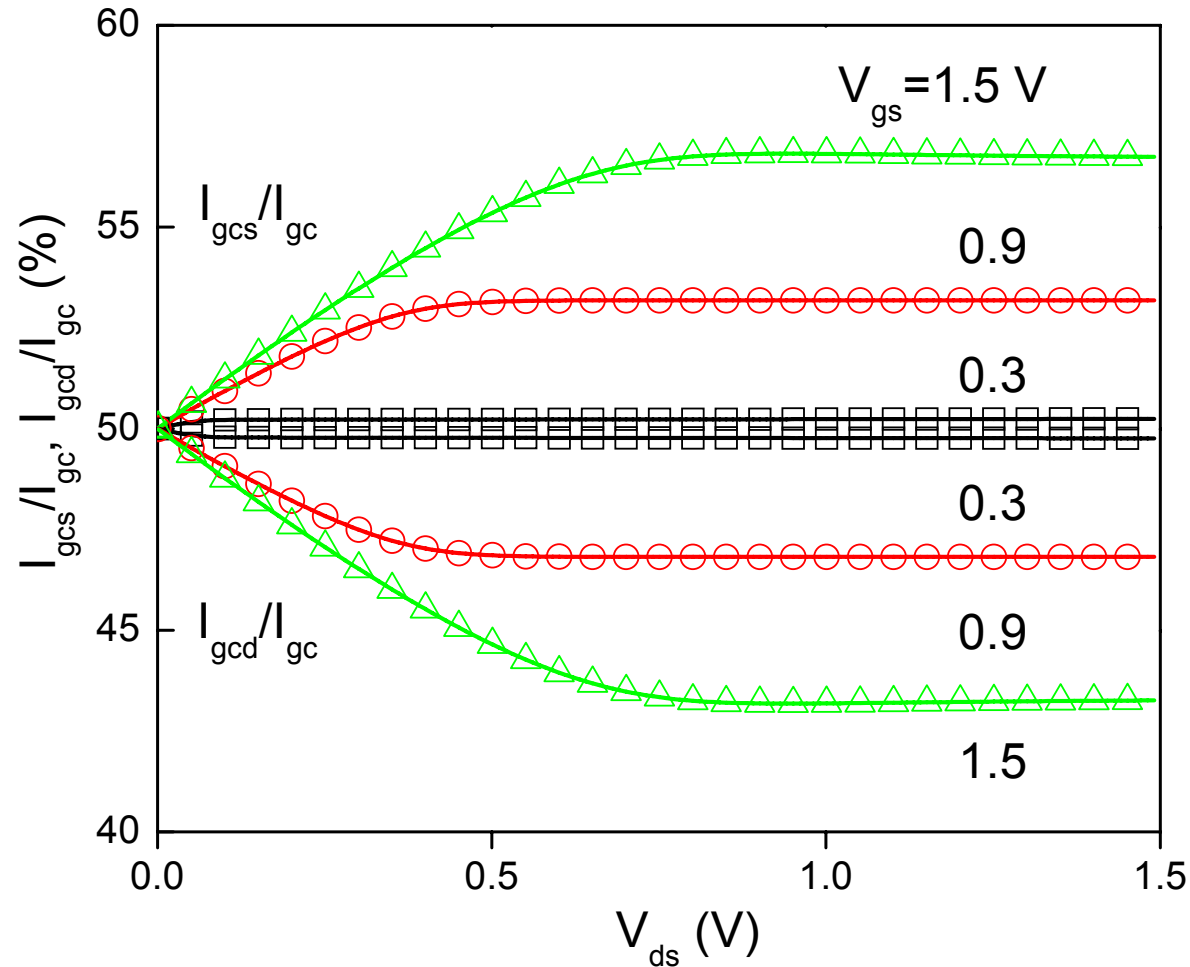
$$I_{gc} = W \int_0^L J_g(y) dy$$

- The partition of I_{gc} into the source and drain components (Shi *et al.* IEDM 2001 and van Langevelde *et al.* IEDM 2001):

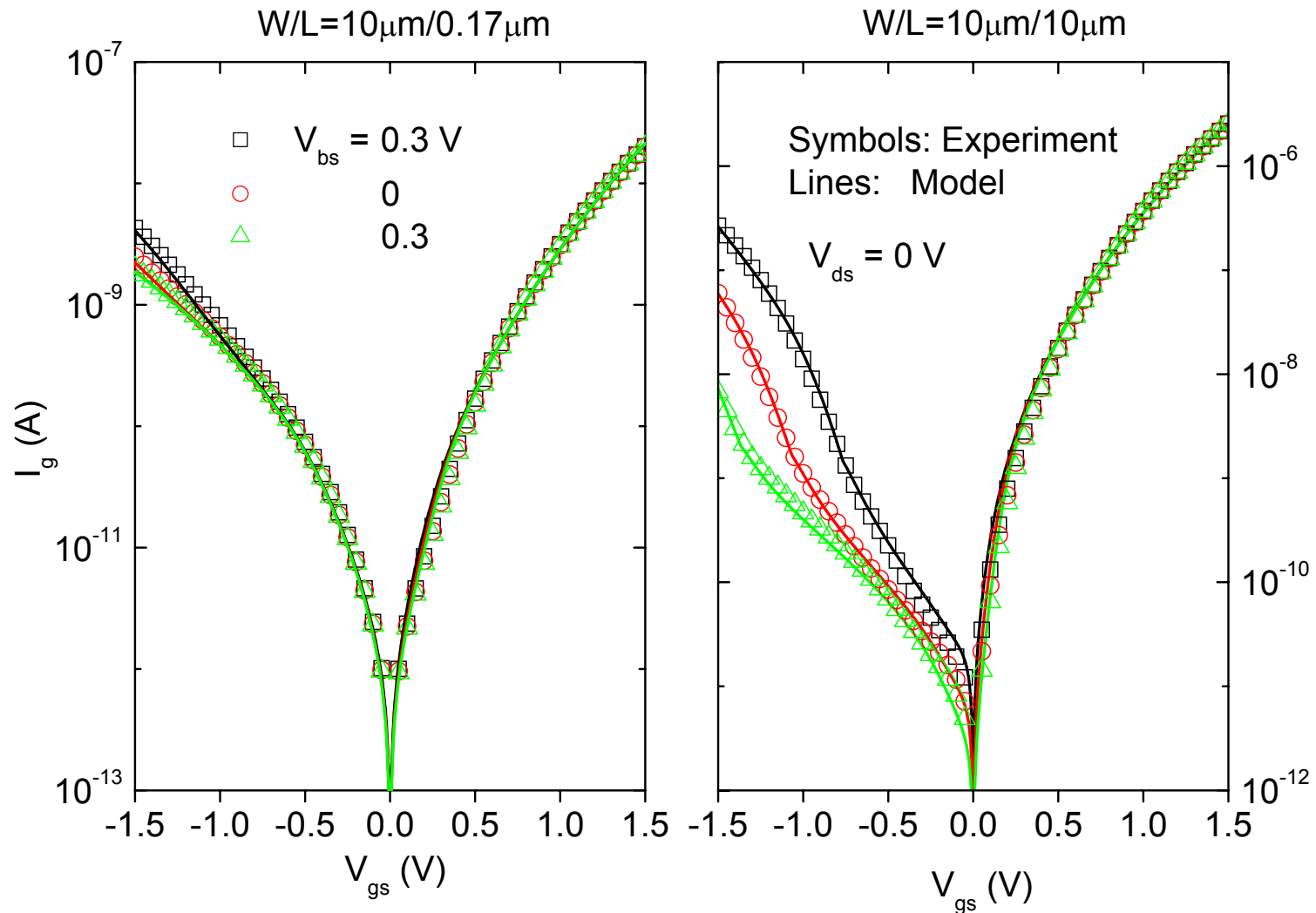
$$I_{gd} = W \int_0^L J_g(y) \frac{y}{L} dy; \quad I_{gcs} = I_{gc} - I_{gcd}$$

- The integrals are evaluated analytically using the symmetric linearization method (Gildenblat and Chen WCM2002)

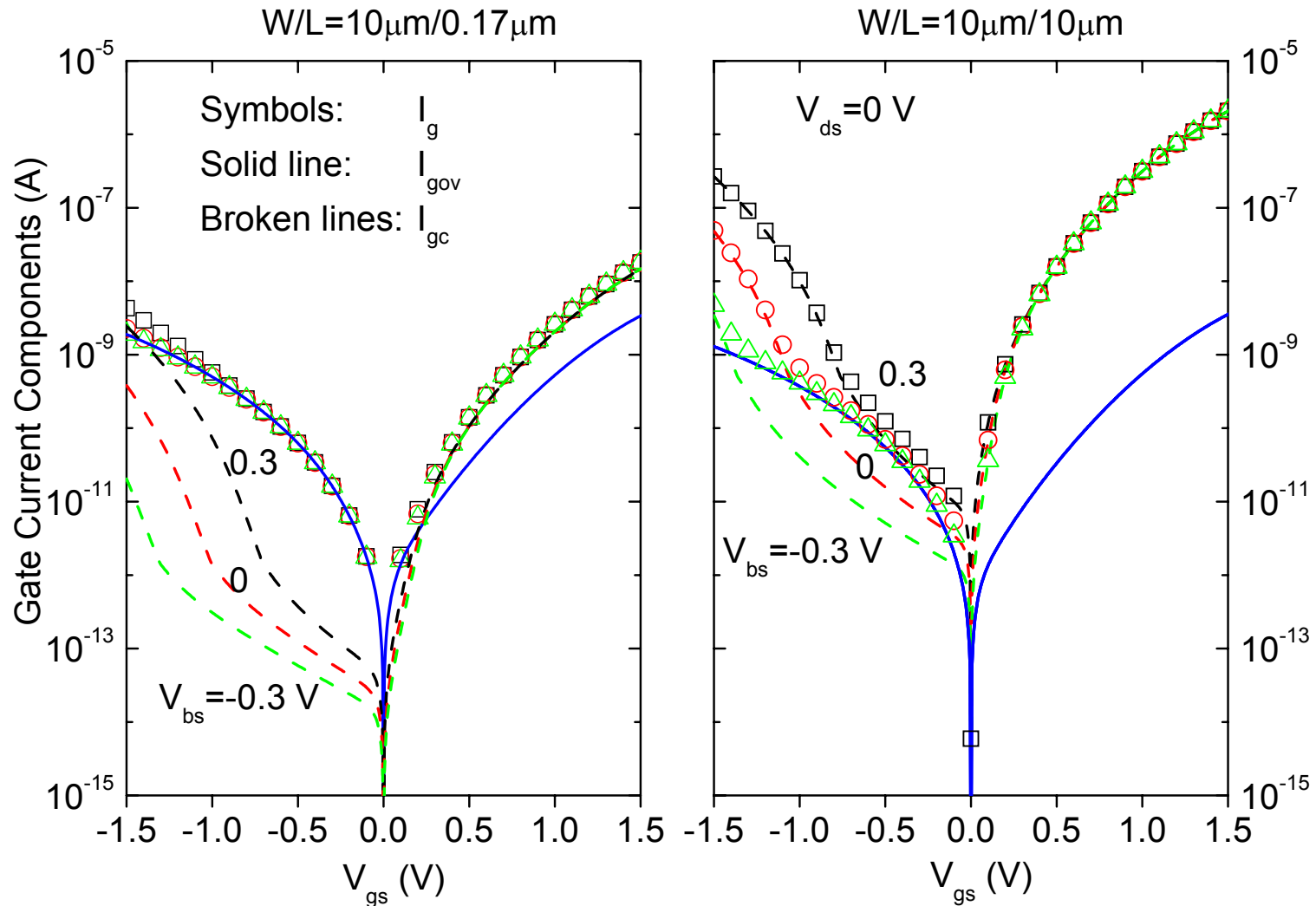
Gate Tunneling Current Model (V)



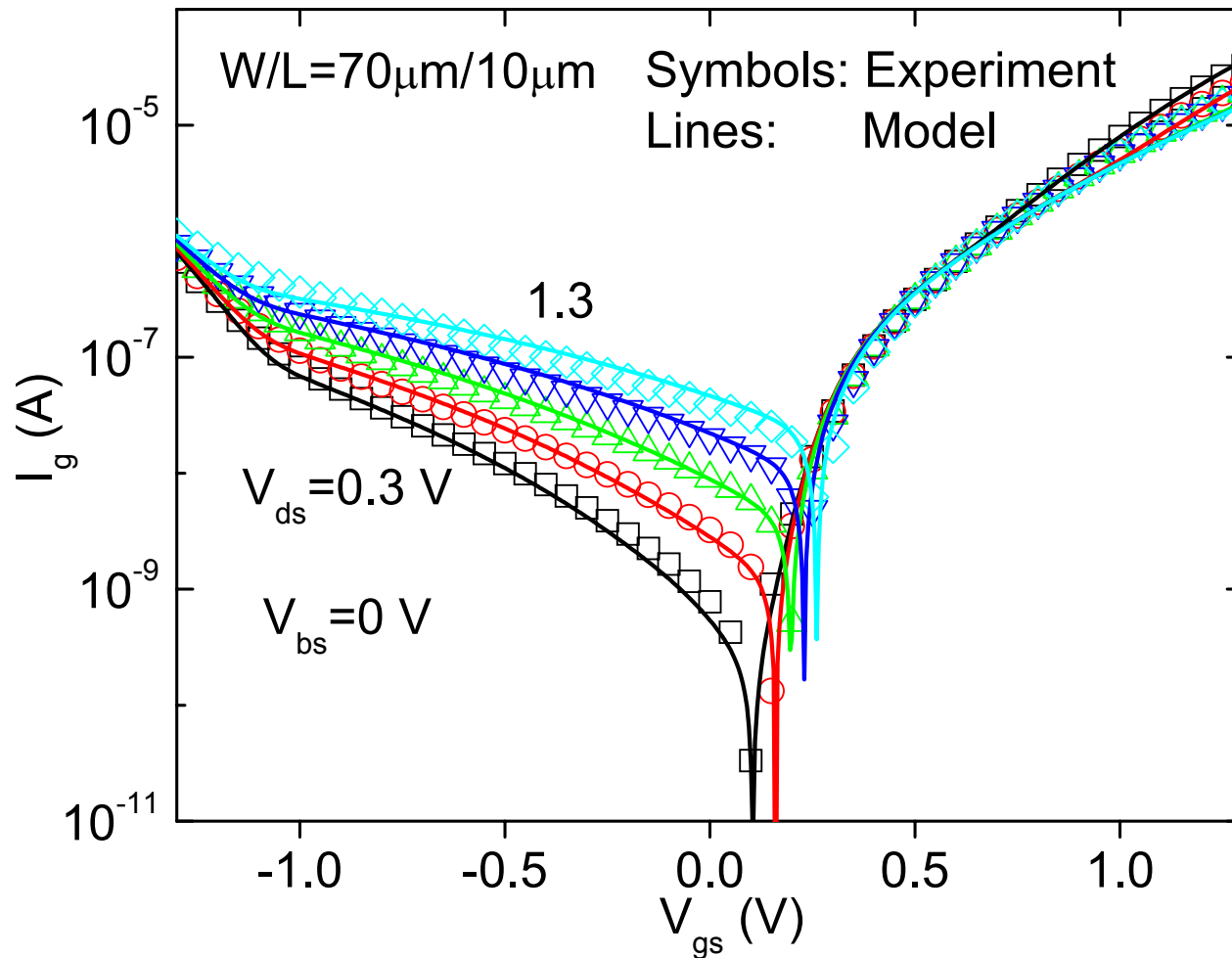
Gate Tunneling Current Model (VI)



Gate Tunneling Current Model (VII)



Gate Tunneling Current Model (VIII)



Substrate Current (I_b) Model

- The original expression based on the pseudo-2D analysis

$$I_b = \begin{cases} a_1 I_d \exp\left(\frac{a_2}{V_{ds} - a_3 V_{dsat}}\right) & V_{ds} > a_3 V_{dsat} & (1) \\ a_1 I_d \exp\left(\frac{a_2}{V_{ds}}\right) & \text{in subthreshold} & (2) \end{cases}$$

- $V_{ds} - a_3 V_{dsat}$ represents the potential drop across the velocity saturation region and a_2 models the characteristic length
- Conventional threshold-voltage-based models rely on the smoothing functions to achieve the transition between the two regions

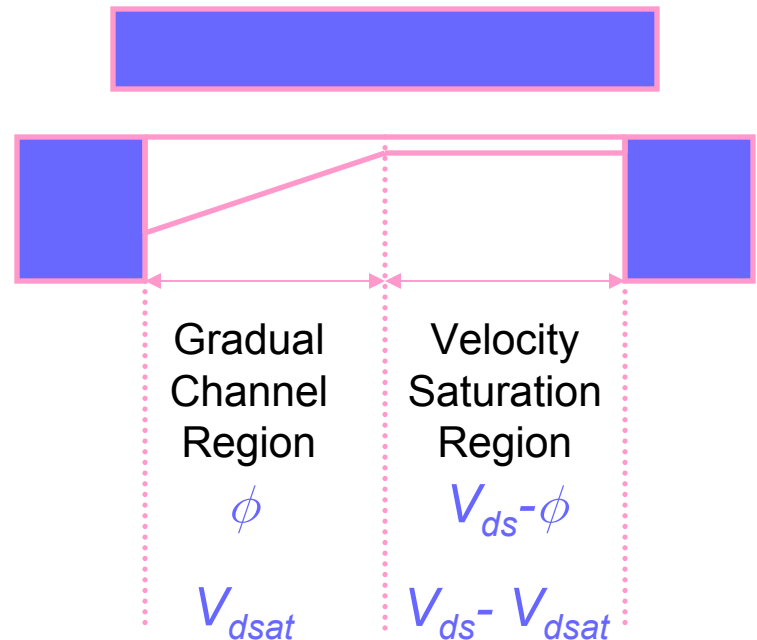
(1) C. HU *et al.* TED 1985

(2) B. INIGUEZ *et al.* SSE 1997

Substrate Current Model (II)

- Within the context of the SP model, the potential drop across the velocity saturation region is given by $V_{ds} - \phi$
- In the subthreshold region, $\phi \rightarrow 0$, the asymptotic behavior is achieved automatically
- In the subthreshold region, ϕ is obtained directly by manipulating the surface potential equations at the two ends of the gradual channel region, no numerical problem
- a_2 is made a function of V_{bs} to model the back-bias dependence of characteristic length
- In SP, a modified expression is used

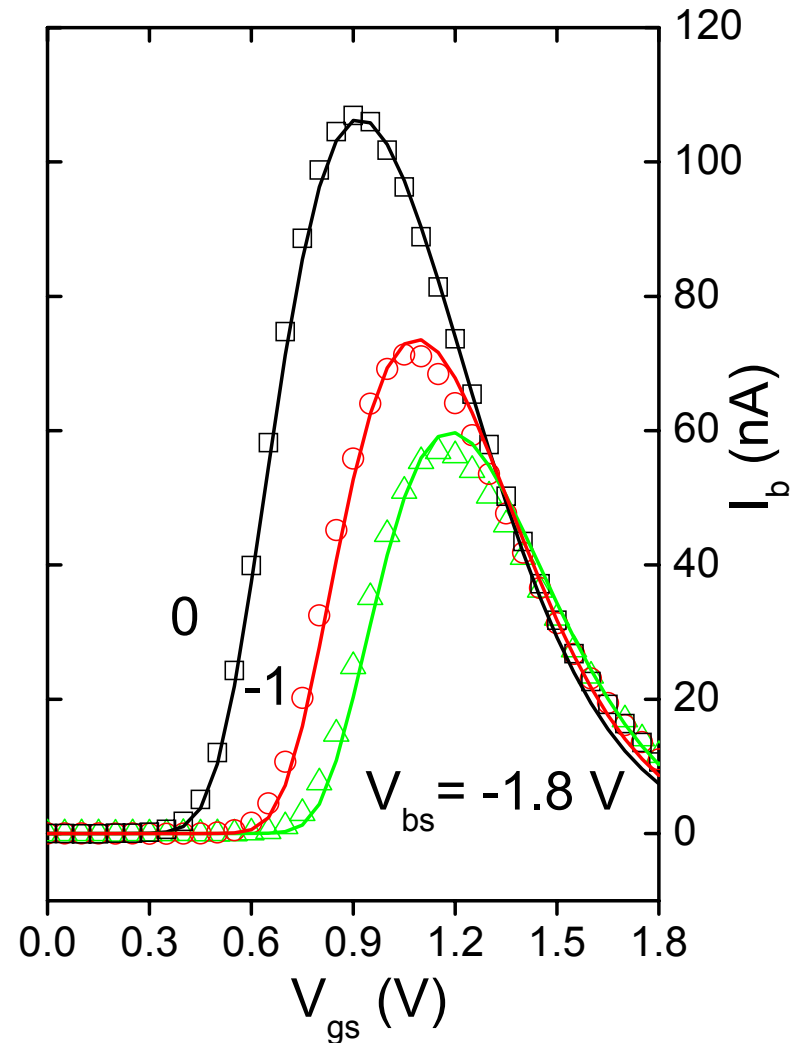
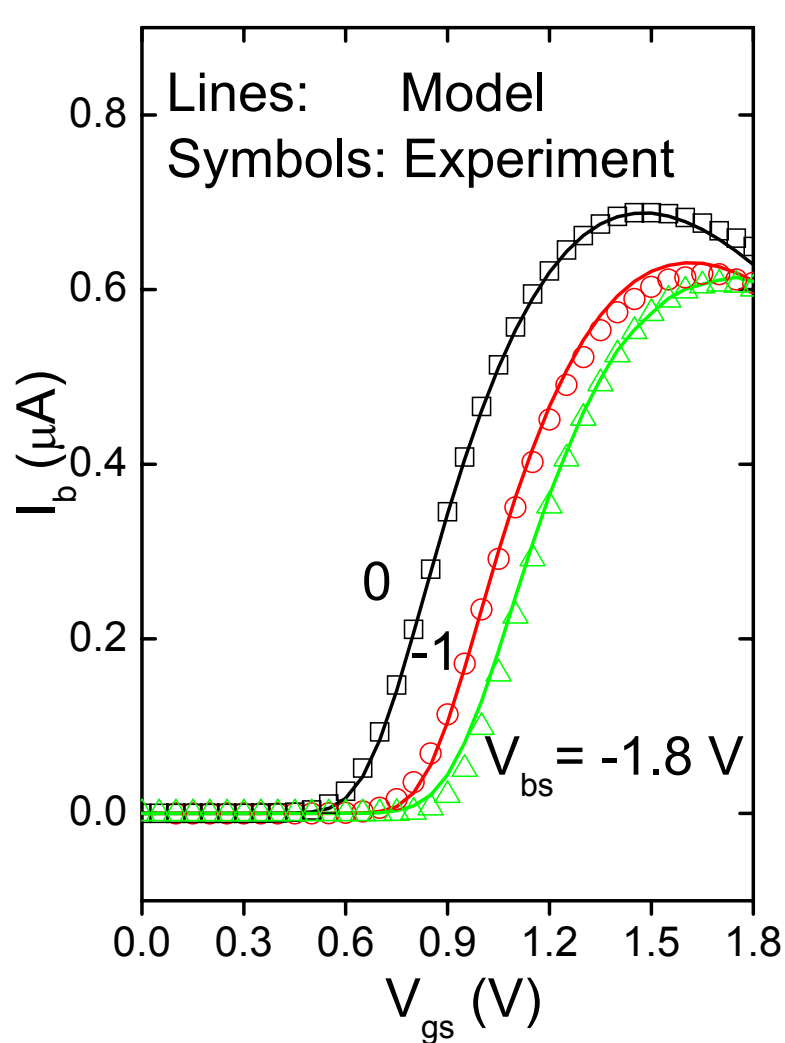
$$I_b = a_1 I_d \exp\left(\frac{a_2}{V_{ds} - a_3 \phi}\right)$$



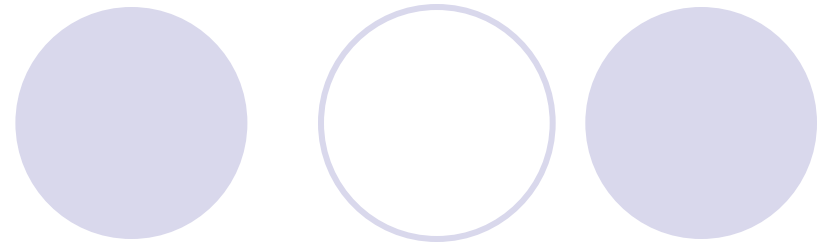
Substrate Current Model (III)

W/L=10 μ m/0.2 μ m

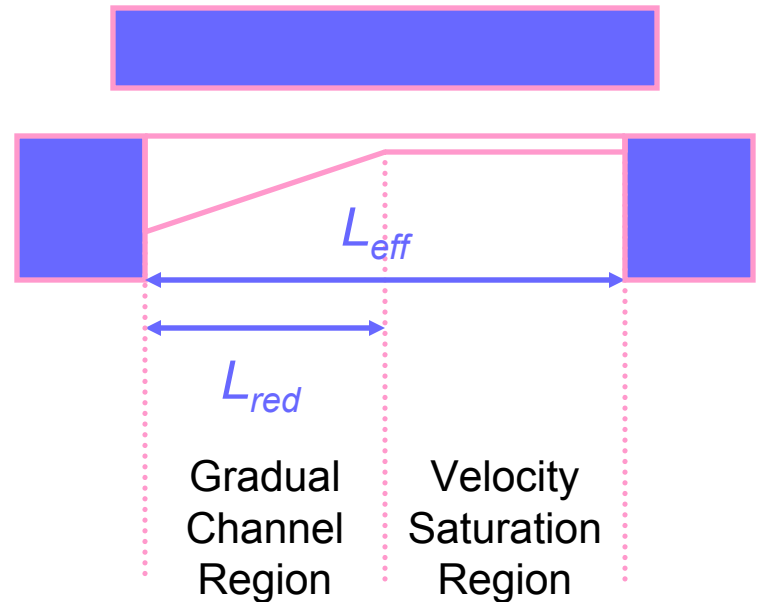
W/L=10 μ m/0.5 μ m



Noise Sources



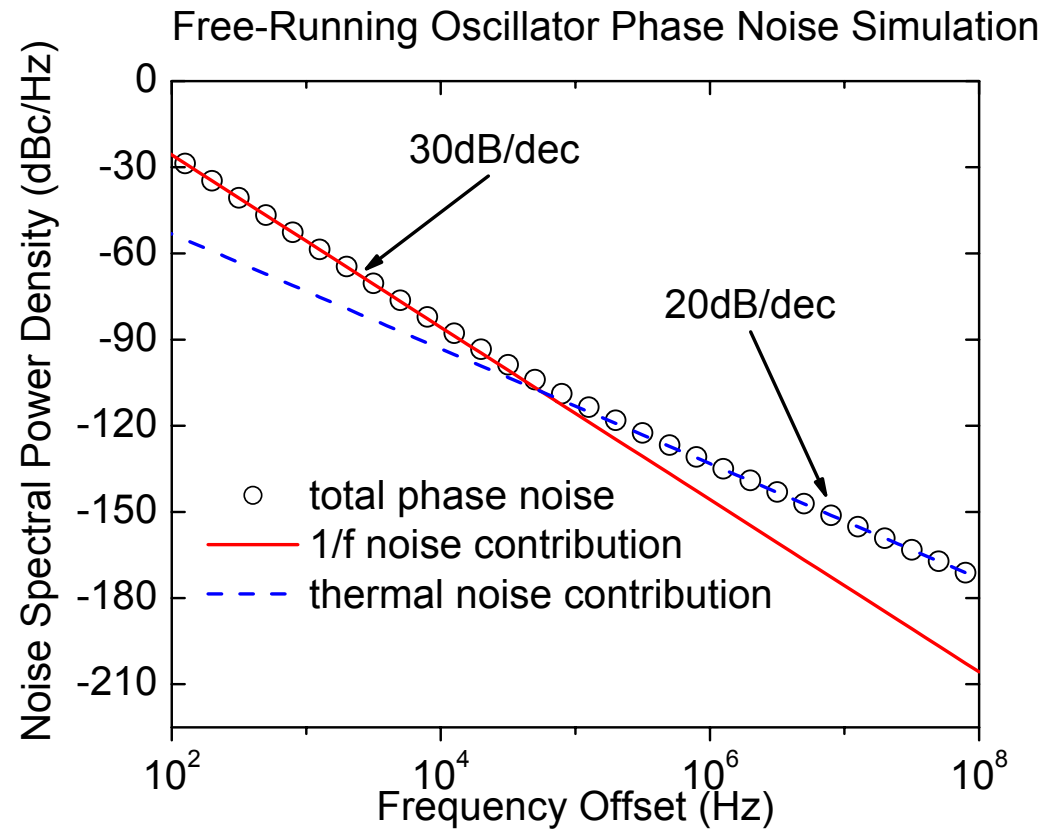
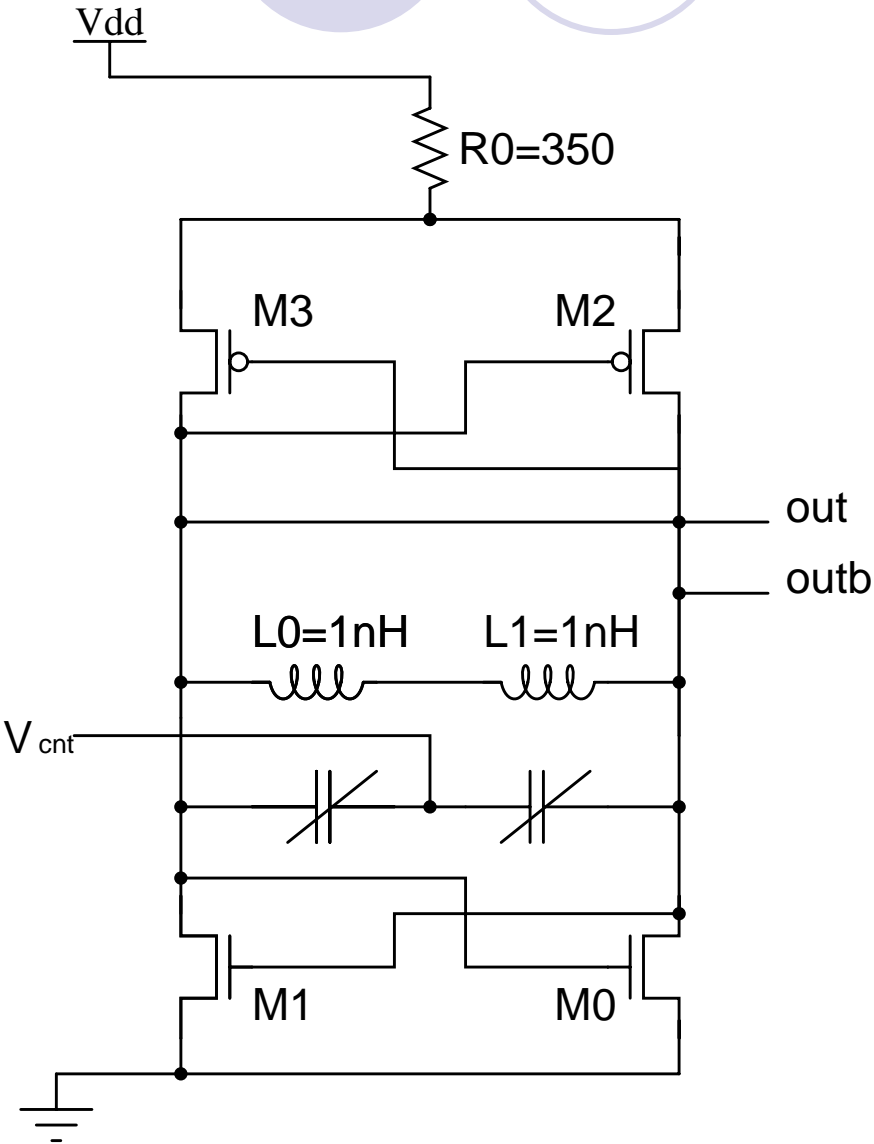
- Channel thermal noise model
“excess” thermal noise of the short-channel devices is included via CLM
- Improved flicker noise model
Conventional approach (Hung *et al.* TED 1993) in the context of the surface-based-model yields a single expression valid for all the regions of operation



$$S_{id} = \frac{4k_B T}{L_{red}^2} \int_0^{L_{red}} g^2(x) dx$$

Neglect the contribution from the velocity saturation region where $g(x) \approx 0$ (Deen *et al.* TED 2002)

Noise Sources – Circuit Simulation





Other Extrinsic Components

- Two approaches provided to model series resistance – absorbed and lumped
- Junction current and capacitance models are included
- Gate and substrate resistance are modeled by adding external elements to the core model
- Bias dependent inner-fringe capacitances
- Channel induced gate noise

Conclusions – SP Extrinsic Model

- Using surface-potential-based approach increases the physical content of the compact model
- Correct asymptotic behavior is automatically ensured, not by using smoothing functions
- Excellent reproduction of experimental data with small set of model parameters
- SP model is complete now, being transferred to industry

more information about SP – gildenblat@psu.edu