Gate Current Partitioning in MOSFET Models for Circuit Simulation

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Motivation

• Aggressive MOSFET scaling giving rise to non-negligible direct tunneling current
• Modeling of short-channel effects are imperative for IC design accuracy

Objectives

• Develop a surface-potential based compact gate-current model
• Accurately describe partitioning of gate-current between source and drain

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Modeling Approach

- Description of different gate-tunneling mechanisms
  - Gate-to-Channel Tunneling
  - Gate-to-SDE Tunneling

- Use of three core MOSFET concepts
  - Band-to-Band generation of carriers
  - Surface potential
  - Inversion charge

- Generate mathematical description of core concepts

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Summary of Core Model Equations

Source-Drain Partitioning

\[ I_{G,D} = W \int_{0}^{L} \frac{y}{L} J_G \, dy \]
\[ I_{G,S} = W \int_{0}^{L} (1 - \frac{y}{L}) J_G \, dy \]
\[ I_G = I_{G,S} + I_{G,D} \]

Gate Current Density and Average Inversion Layer Thickness

\[ J_G = q x_C A \frac{E_{ox}^2}{E_g^2} \exp(-B \frac{E_g^3}{E_{ox}}) \]
\[ x_C \equiv \sqrt[3]{\frac{Q_i'}{q N_{sub} L_D \sqrt{2}}} \]

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Results

Gate Current versus Gate Voltage

- $V_d = 0$, $T_{ox} = 2.48\text{nm}$
- $L = 5\mu\text{m}$

Gate Current versus Drain Voltage

- $W/L = 10\mu\text{m}/5\mu\text{m}$, $T_{ox} = 2.48\text{nm}$, $V_g = 1.2\text{V}$

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Conclusion

- A new gate-current partitioning model suitable for circuit simulation has been developed
- Gate-current model has been validated with measurements
- Partitioning method has been validated by using 2-D device simulation