

# Gate Current Partitioning in MOSFET Models for Circuit Simulation



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## Motivation

- Aggressive MOSFET scaling giving rise to non-negligible direct tunneling current
- Modeling of short-channel effects are imperative for IC design accuracy

## Objectives

- Develop a surface-potential based compact gate-current model
- Accurately describe partitioning of gate-current between source and drain



## Modeling Approach

- Description of different gate-tunneling mechanisms
  - Gate-to-Channel Tunneling
  - Gate-to-SDE Tunneling
- Use of three core MOSFET concepts
  - Band-to-Band generation of carriers
  - Surface potential
  - Inversion charge
- Generate mathematical description of core concepts



# Summary of Core Model Equations

## Source-Drain Partitioning

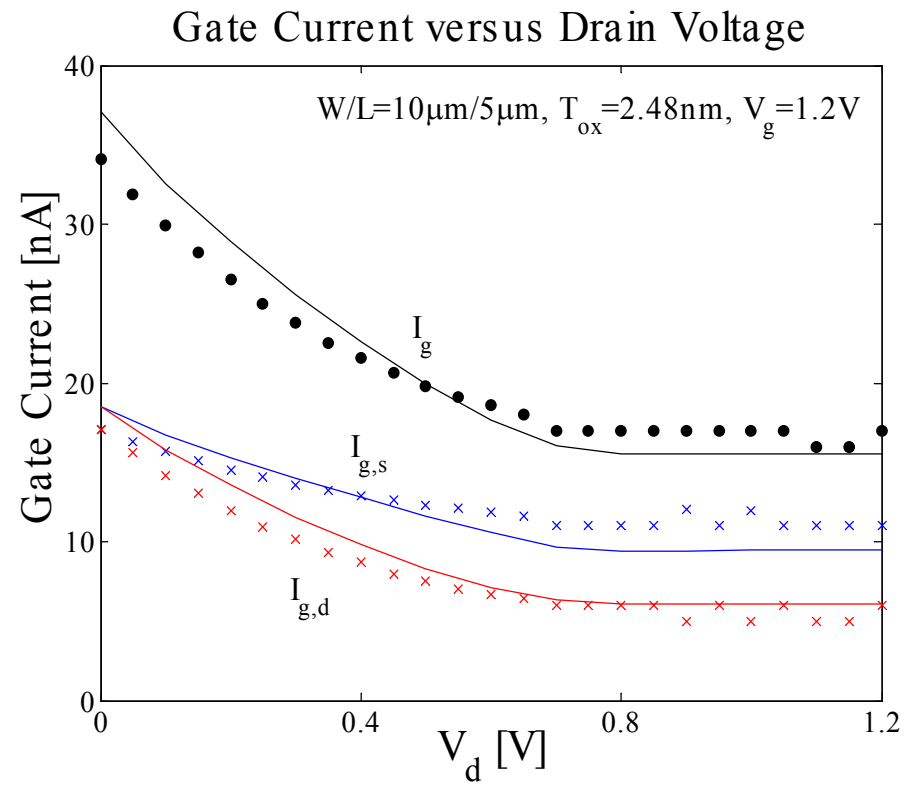
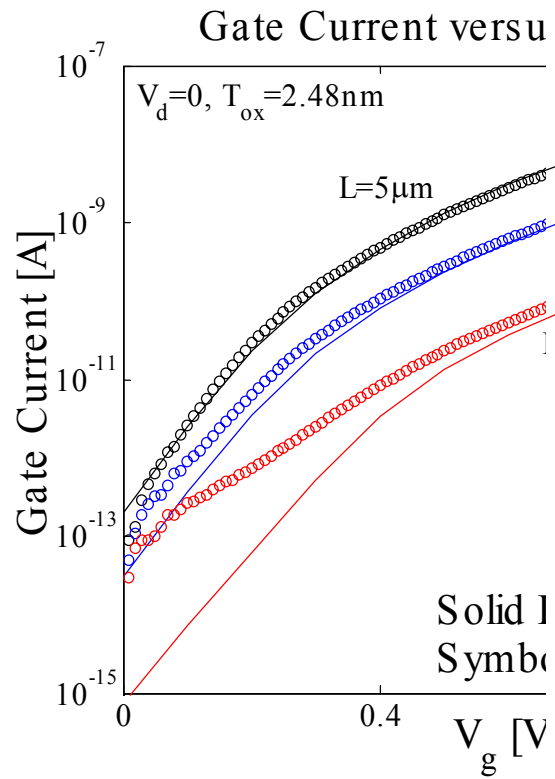
$$\begin{aligned} I_{G,D} &= W \int_0^L \frac{y}{L} J_G dy \\ I_{G,S} &= W \int_0^L \left(1 - \frac{y}{L}\right) J_G dy \end{aligned} \quad \Bigg\} \quad I_G = I_{G,S} + I_{G,D}$$

## Gate Current Density and Average Inversion Layer Thickness

$$J_G = q \bar{x}_C A \frac{E_{ox}^2}{E_g^{\frac{1}{2}}} \exp\left(-B \frac{E_g^{\frac{3}{2}}}{E_{ox}}\right) \quad \bar{x}_C \equiv \sqrt{\frac{Q_i'}{q N_{sub} L_D \sqrt{2}}}$$



# Results





## Conclusion

- A new gate-current partitioning model suitable for circuit simulation has been developed
- Gate-current model has been validated with measurements
- Partitioning method has been validated by using 2-D device simulation