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Modeling and Characterization of Copper Interconnects

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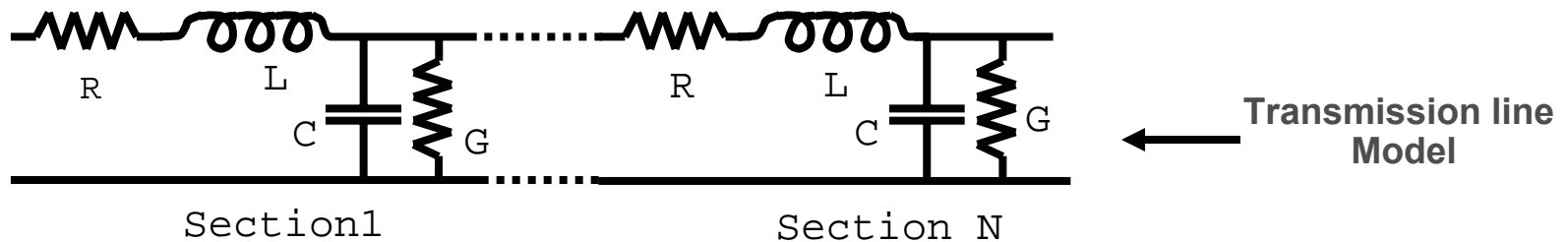
February 2003

Outline

- Interconnect – an overview
 - Why copper ?
- What is different in modeling Cu wires
 - Resistance modeling
 - Inductance modeling
 - Capacitance modeling
- Full-chip approach
- Silicon Validation
- Model order reduction
- Conclusion

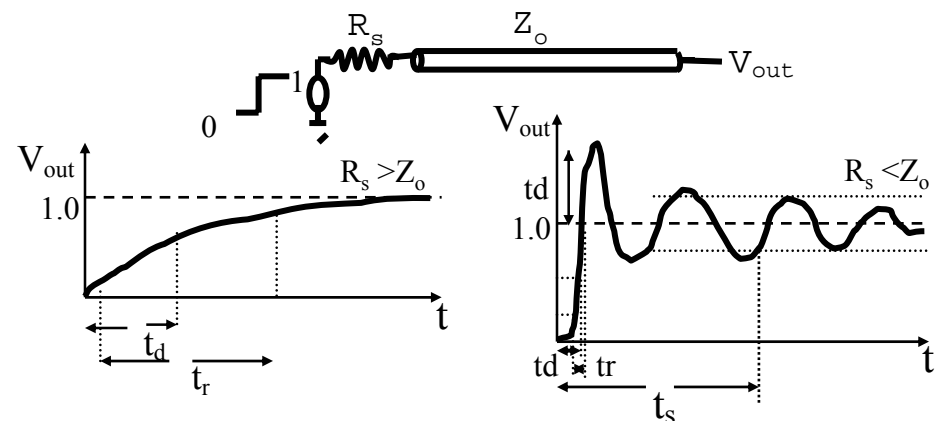
An Overview

- An interconnect is characterized by three elements **Resistance R**, **Capacitance C**, **Inductance L**, known as interconnect *parasitic elements*, that are distributed in nature, just like a Transmission lines



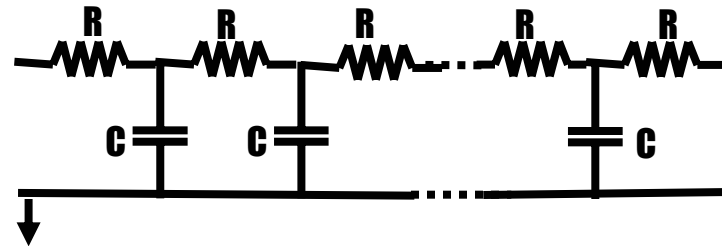
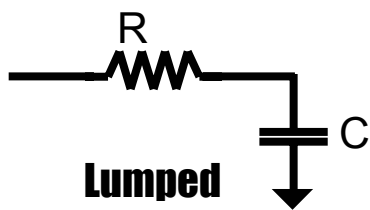
- The three parameters R, C, L, are not equally important, depends upon
 - Length of the line,
 - Signal rise time t_r ,
 - driver impedance Z_s , and
 - line impedance Z_0 .

$$Z_0 = \sqrt{\frac{R + j\omega L}{G + j\omega C}} \approx \sqrt{\frac{R + j\omega L}{j\omega C}}$$



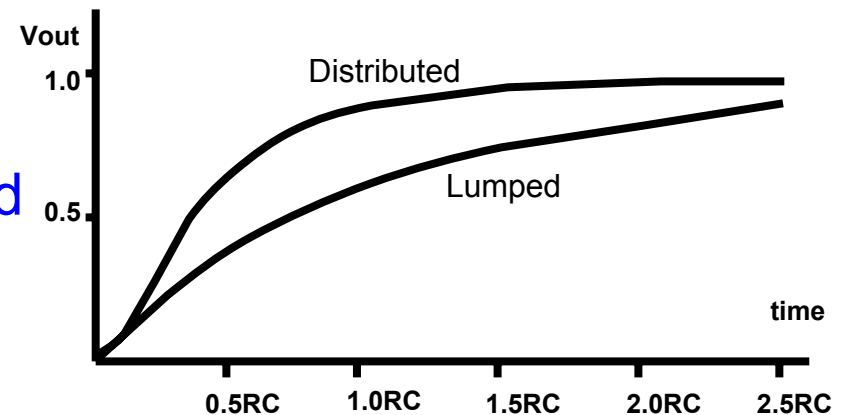
Distributed RC

- For circuit modeling we replace these distributed elements into series of lumped elements.

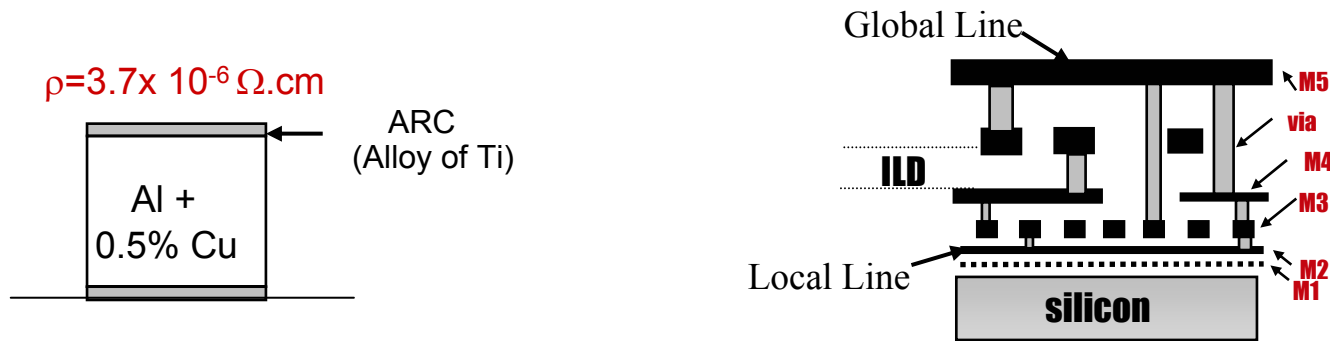


- Lumping of the elements depends upon signal frequencies of interest.

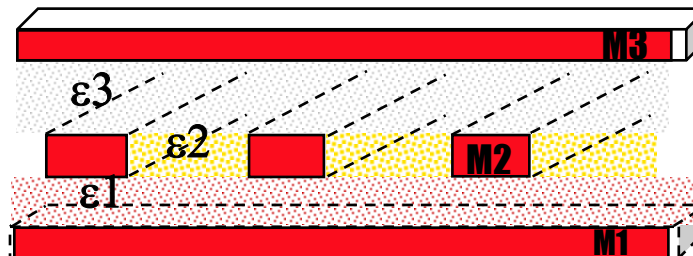
Response of distributed vs lumped



- Past 30 years Al has been *de facto* industry standard as a material for interconnections.
 - Over the years Al evolved from single layer to multiple levels of sandwiched Ti/Al-Cu/TiN

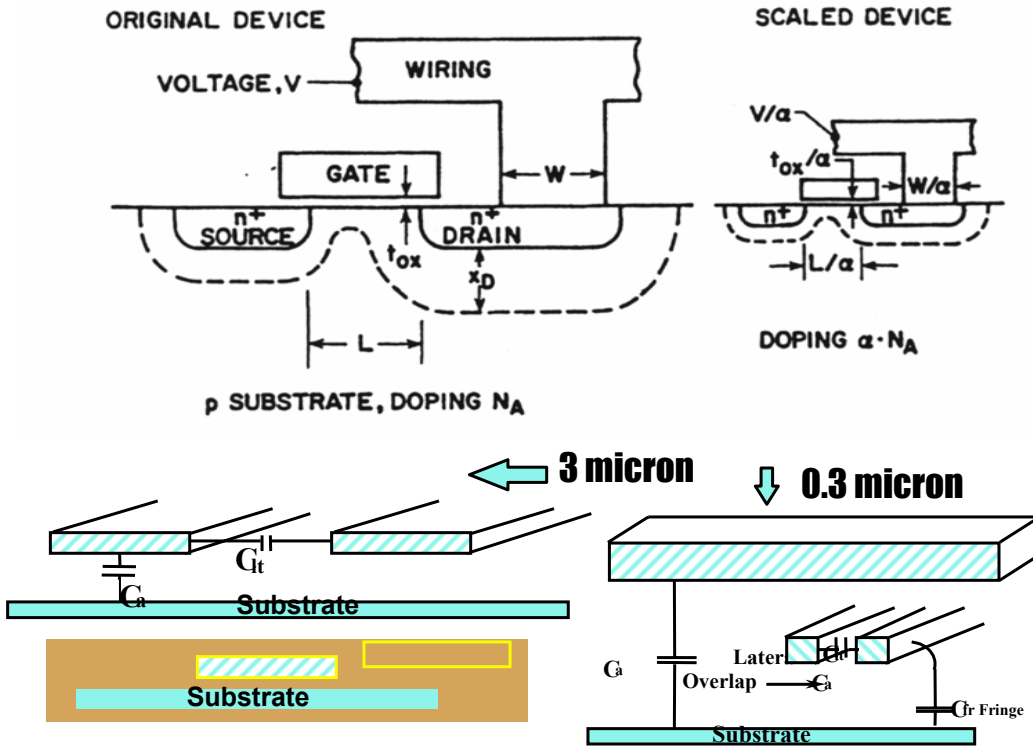


- Single layer of dielectric material to multiple dielectrics



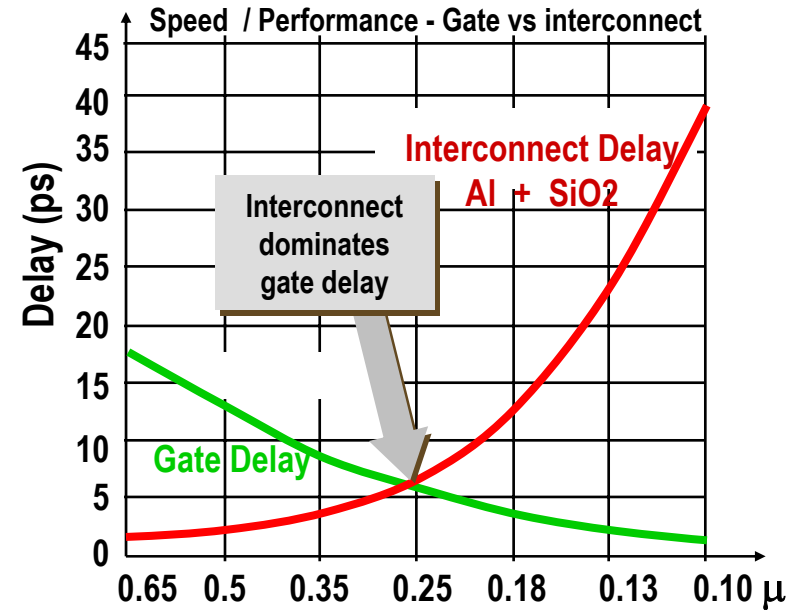
Technology Trends

- With ever increasing demand for **faster**, **reliable** and **higher functionality** chips, transistors have been systematically scaled down in dimensions and so has the interconnects



Total Capacitance

$$C_t = C_g + C_{ov} + C_{fr}$$

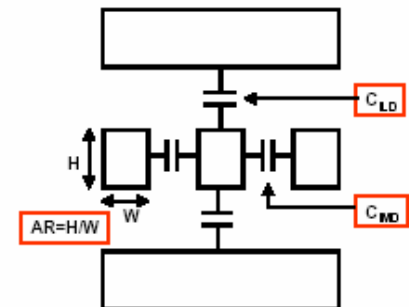
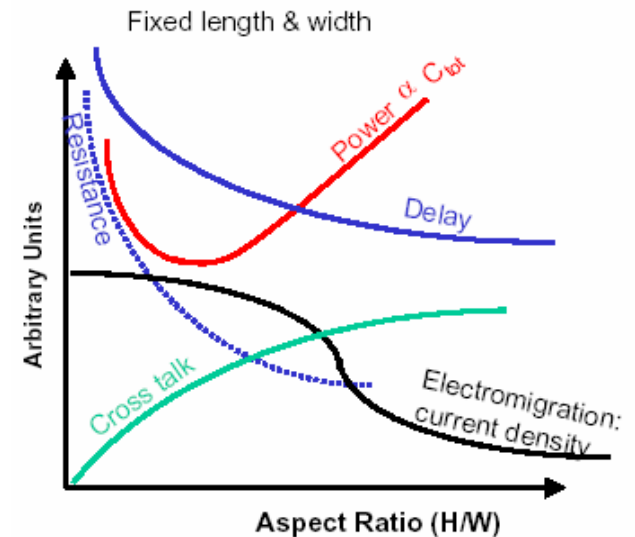


Source: SIA Roadmap 1997

Interconnect Scaling - 1

- Scaling dimensions though resulted in many advantages it also resulted in significant *degradation in interconnect related circuit parameters*

- Propagation delays (Timing)
 - wire R, C and L
- Cross-talk effects (Signal Integrity)
 - False switching due to C_c , L
- Clock skew (Signal Integrity)
 - wire R, C and L
- Electromigration effect (Reliability)
 - wire R, C
- IR Voltage Drop (Reliability)
 - wire R, C
- Power Consumption (Reliability)
 - wire C

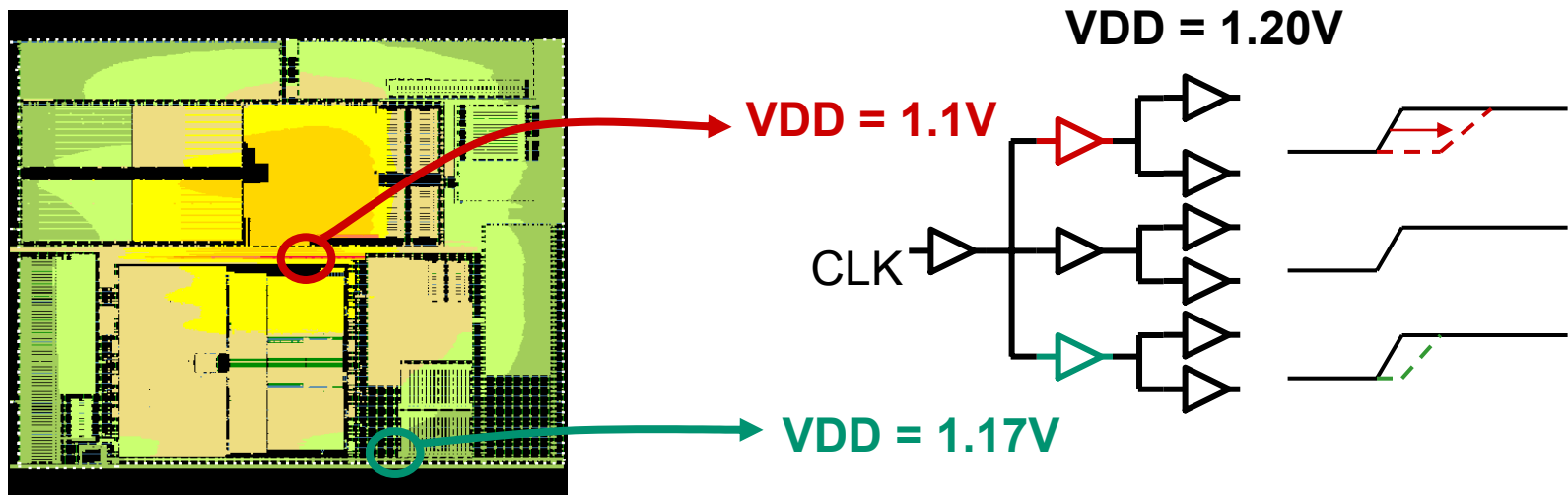


K. Saraswat et al. TFUG 3/20/02

Which in fact are chip design issues.

IR Drop & Ground Bounce

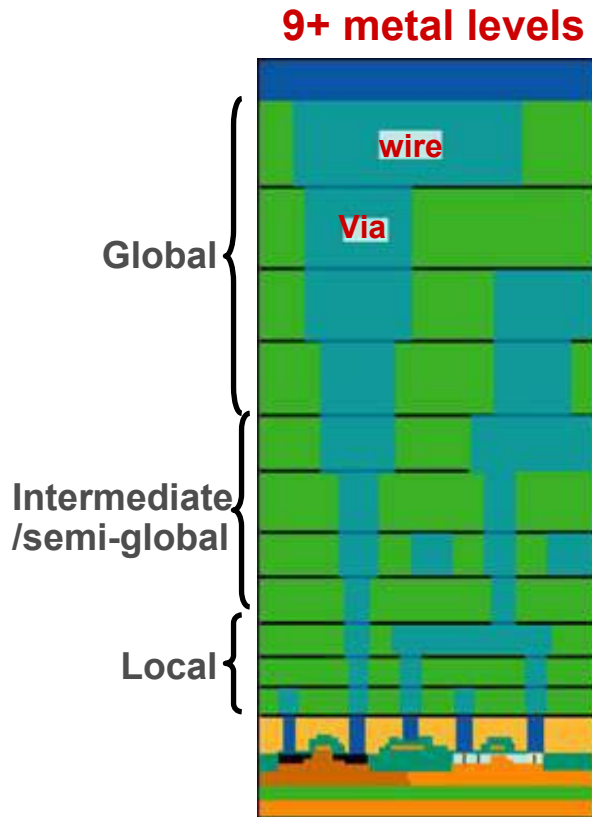
- IR Drop (ground bounce) increases clock skew
 - Hold time violations
- IR Drop (ground bounce) increases signal skew
 - Setup time violations



Impacts timing and leads to failed silicon

Wiring is central to nanometer SoC design

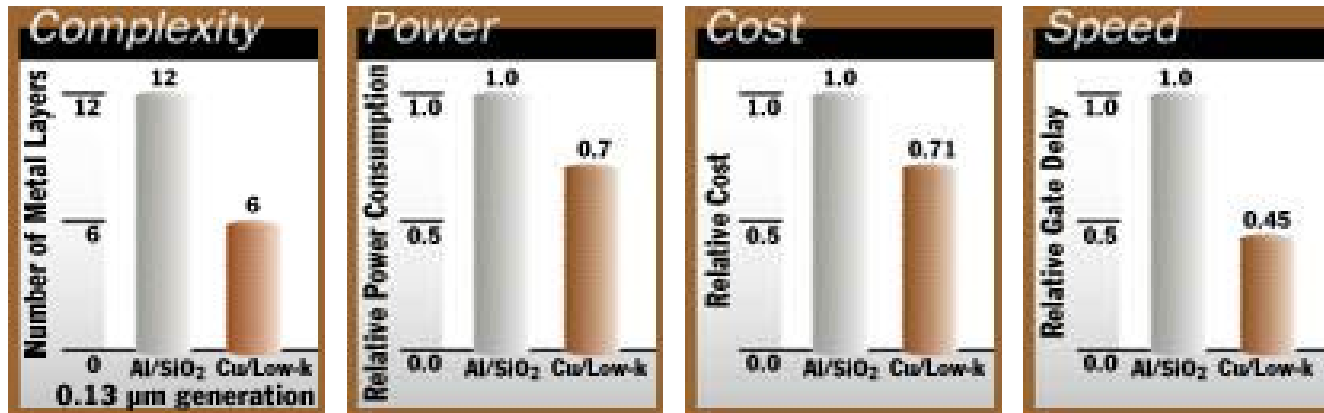
- Wires dominate manufacturability
 - RLC variation
- Wiring interacts
 - Timing,
 - Clocking,
 - Cross-talk,
 - Signal integrity,
 - Power inter-related
- “R” dependence is common



Source: ITRS Roadmap 1999

Cu as Interconnect lines

- Cu has $\frac{1}{2}$ the resistance of Al.
- An order of magnitude higher electromigration resistance
- It has many advantages:



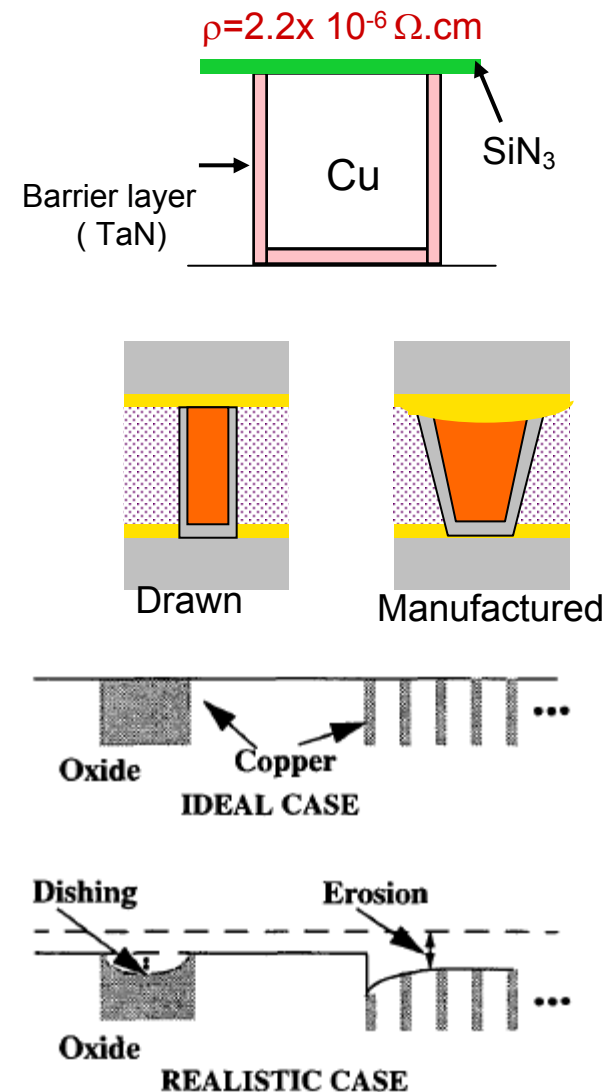
www.Novellus.com

Major process change moving from 180nm technology node to 130nm node was the use of

Cu interconnects and low K dielectrics

Copper Process

- Dual Damascene -- Trench etch profile, Barrier/Seed layer
- Lithography -- Cu wire dimensions are not as drawn
- CMP -- **dishing, erosion**
 ↓
 line thickness variation
- **Result:** Cu wire width and thickness becomes function of
 - Wire width and spacing
 - Wire pattern density
 - Wire topography



Impact of Dishing and Erosion

Dishing and Erosion
Layout dependent



Wire Width and
Thickness



Resistance



ILD Thickness



Wire Capacitance

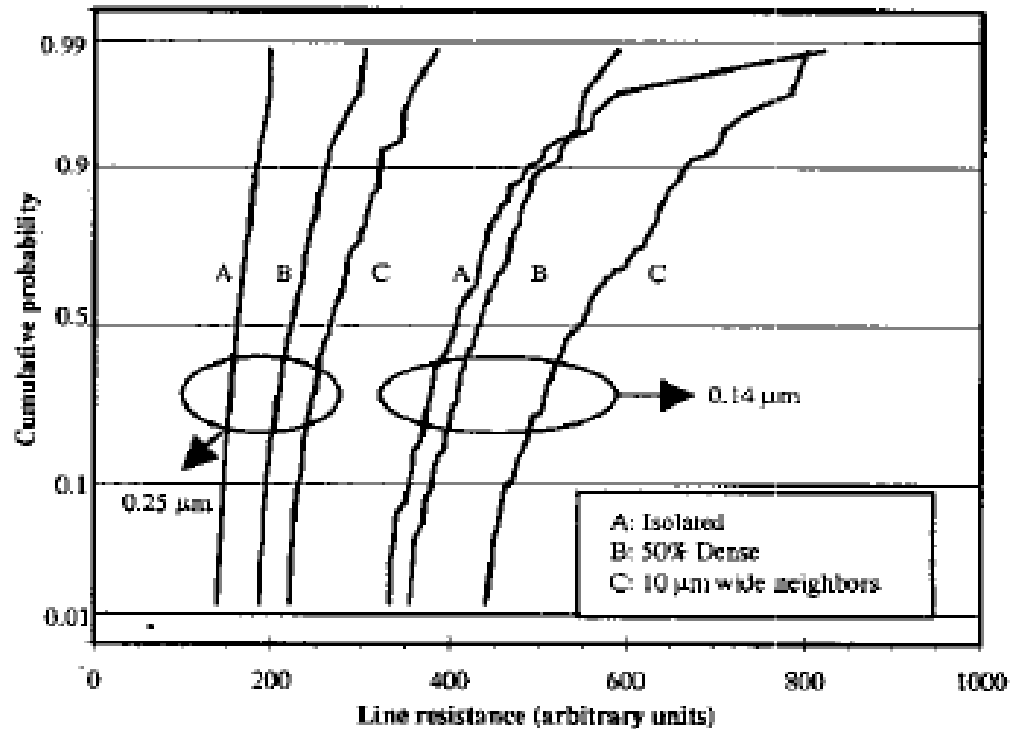


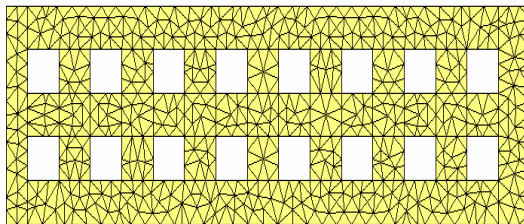
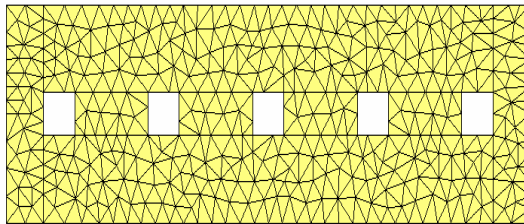
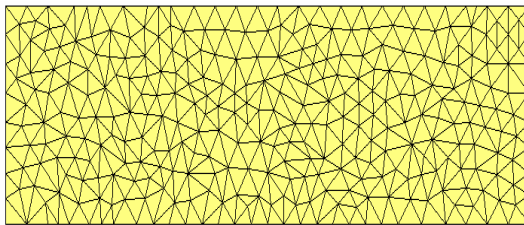
Fig. 1: Resistance of narrow lines for three layout configurations, namely isolated, 50% dense and 10 μm wide neighbors at minimum space.

Lakshminarayan et al. IITS 2001

Metal Density

Slotting

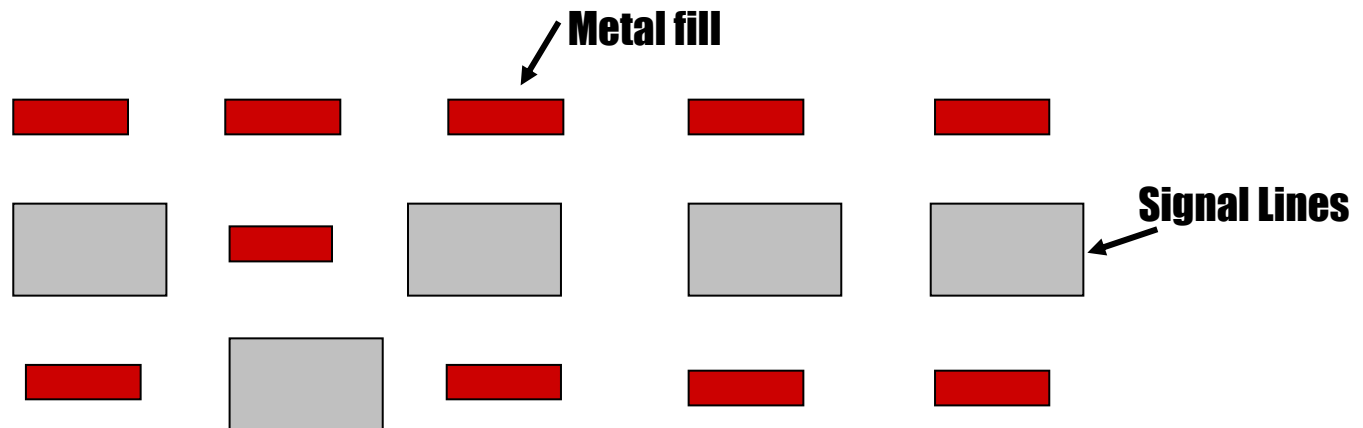
Reduce dishing in wide lines $> 2 \mu\text{m}$



Resistance w/ no slots (Ω)	Results with slots (Ω)	Difference No Slots vs Slots (%)
0.1569	0.1569	0
	0.1781	13.51
	0.2340	49.14

Metal Fills

- To reduce dishing and erosion of the inter-level dielectrics, CMP requires metal lines to be at a certain minimum distance from each other (metal density). This leads to the so called **metal fills** (dummy metal) - floating metal lines



- Dummy metals are of different shape and size.
- **Impact of metal fills is to increase line capacitance by 3-5% depending upon shape, size and proximity of the fills to the line.**

Impact of Grounding Fills

Adjacent Line Floating

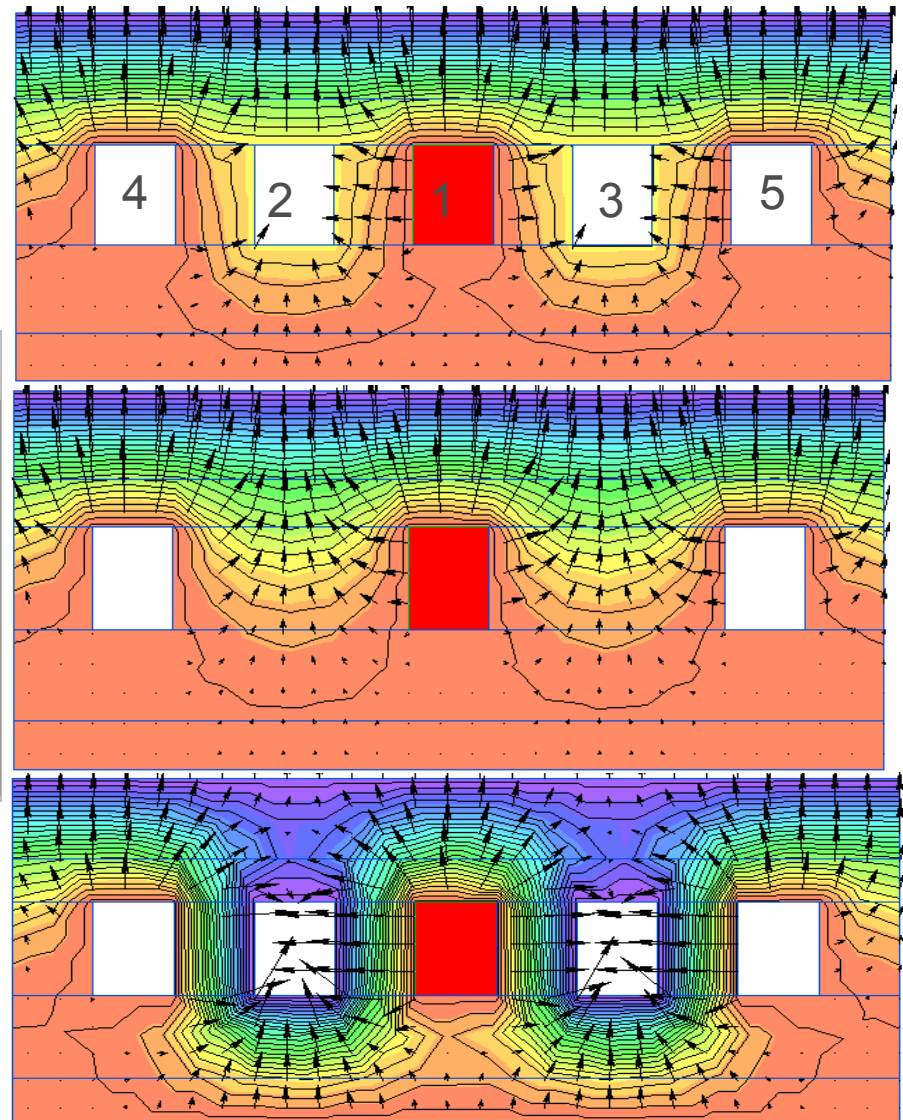
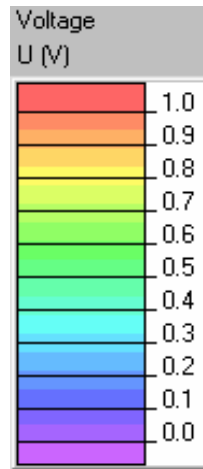
$$C_{\text{total}} = 56.24 \text{ fF/m}$$

Adjacent Line
Removed

$$C_{\text{total}} = 54.61 \text{ fF/m}$$

Adjacent Line Grounded

$$C_{\text{total}} = 155.5 \text{ fF/m}$$



Impact of Cu and low K

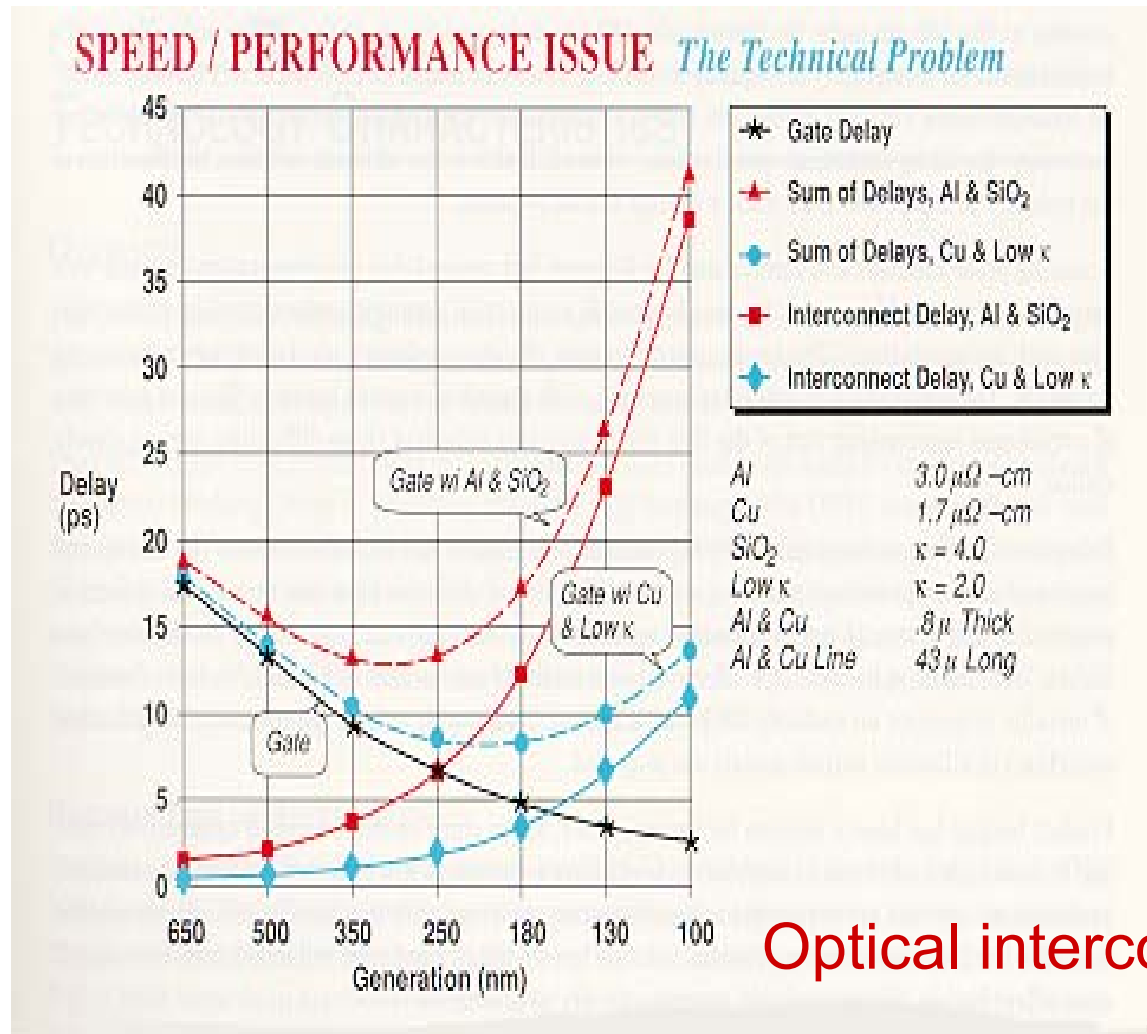
- It is this **proximity effect** that is challenging and necessitated retooling of the design tools.
- Since Cu has $\frac{1}{2}$ of the Al resistance for the same wire dimensions, wire **inductance** effect becomes more dominant

$$\begin{array}{c} \downarrow \quad \uparrow \\ Z = R + j\omega L \end{array}$$

- Ringing and overshoot - problematic for **clocks** since glitches can be observed as transitions leading to faulty switching
- Reflections of signals due to impedance mismatch
- Switching noise due to $L \frac{di}{dt}$ voltage drops - problematic for **power distribution network**.
- The **intra-die variation** of the interconnects becomes more pronounced in Cu wires.

Future of Cu

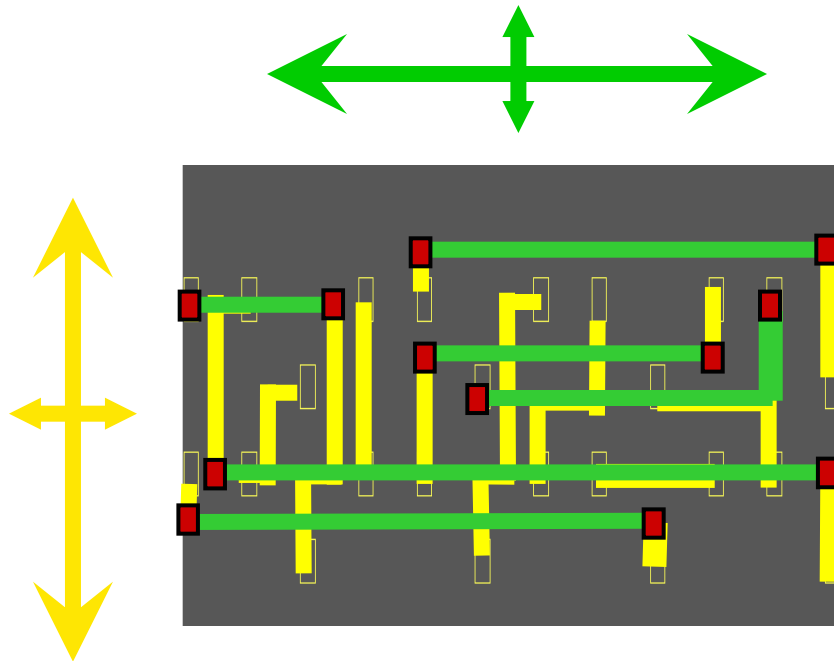
- Use of Cu shifts the delay transition point



Optical interconnects ??

Optimized Manhattan Routing

Preferred direction with optimization



Manhattan X-Architecture

Metal 5



Metal 4



45°

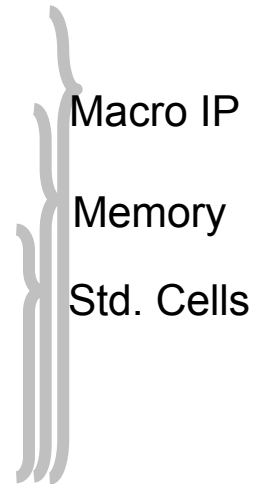
Metal 3



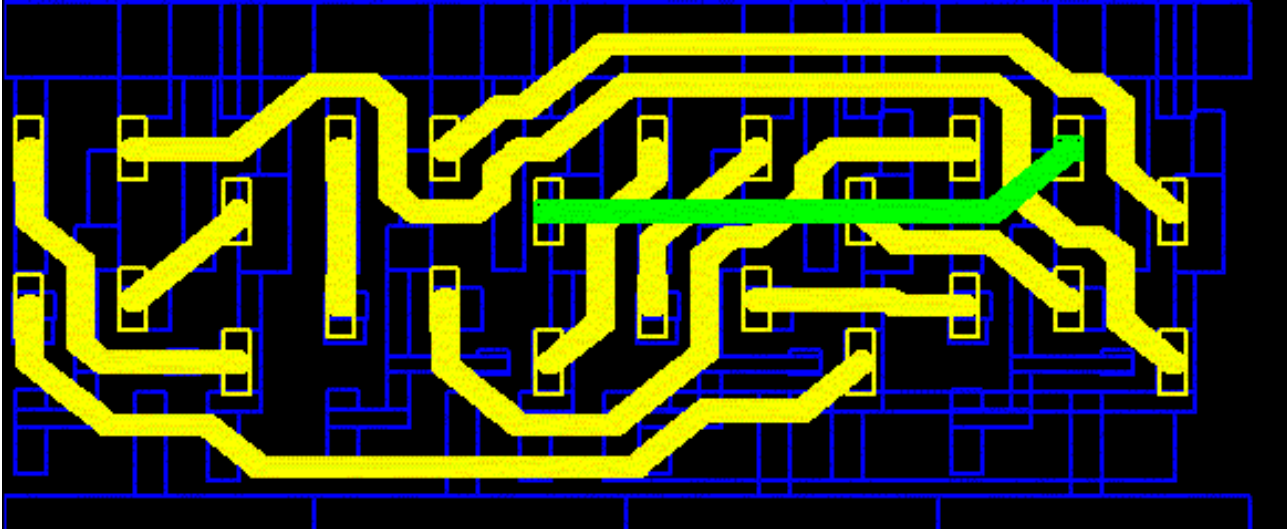
Metal 2



Metal 1



Benefits From X-Architecture



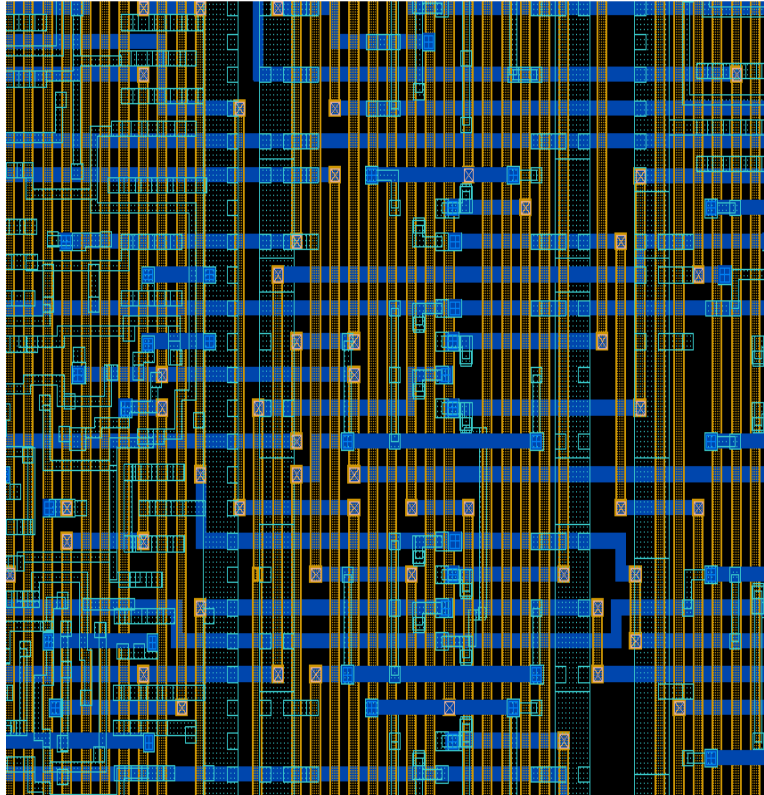
20+% less interconnect
30+% less vias



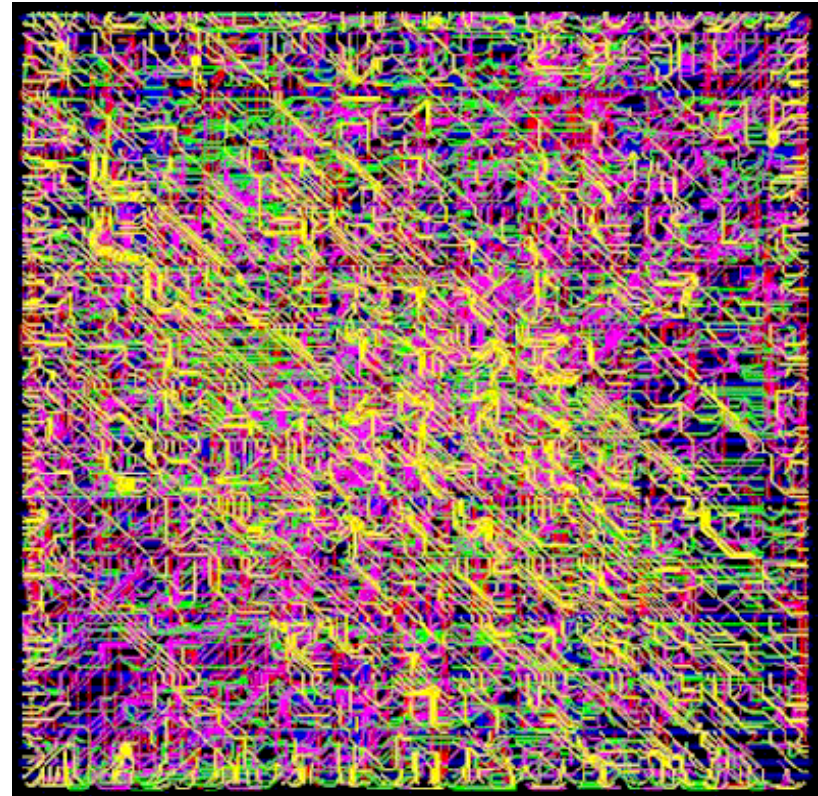
10% performance gain AND
20% power reduction AND
30% cost savings

Manhattan Vs X Architecture:

RISC chip - Manhattan



Toshiba First X-architecture design



Presented at ISSCC 2002

Modeling and Characterization of Interconnects

- The software tool that computes the R,C, L of a chip interconnections is called **Parasitic Extractor**, also known as **circuit level extractor, LPE**, etc.
- **Modeling:**
 - *Numerical methods*, the so called **Field Solvers**:
 - provides accurate em field solutions for complex geometry.
 - allows the modeling of non-linear, inhomogeneous and anisotropic material
 - *Analytical / Empirical models*
- **Characterization:**
 - Low Frequency Measurement
 - Frequency domain S parameter (inductance)
 - Test structure verification

Methods of modeling R, L, C

- Numerical or Field solver approach uses **Maxwell's** Electromagnetic field equations

Ampere's theorem

$$\text{curl} \mathbf{H} = \mathbf{J} + \frac{\partial \mathbf{D}}{\partial t}$$

$$\text{div} \mathbf{D} = \rho$$

Faraday's law

$$\text{curl} \mathbf{E} = -\frac{\partial \mathbf{B}}{\partial t}$$

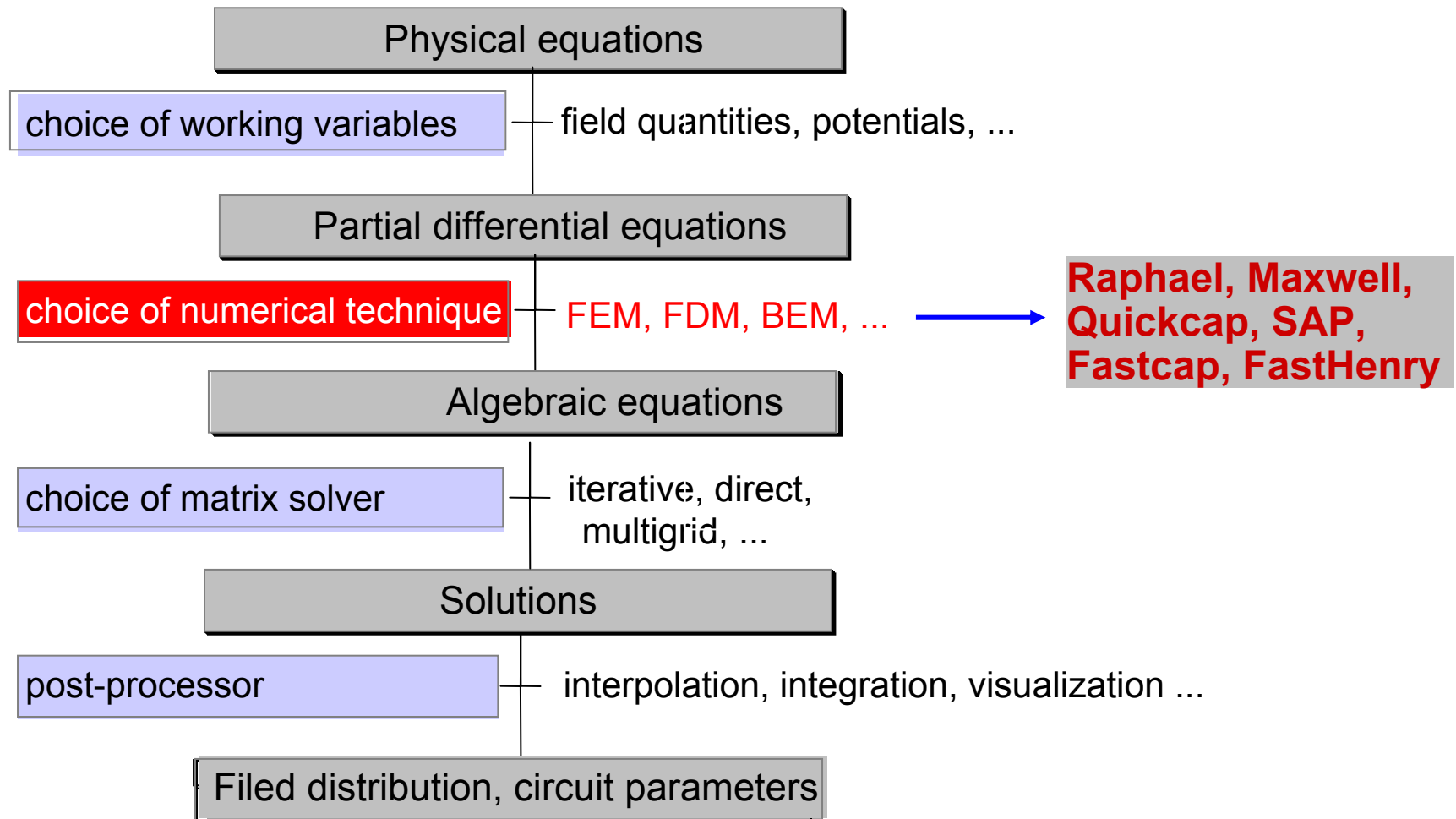
$$\text{div} \mathbf{B} = 0$$

Constitutive equations

$$\mathbf{B} = \mu \mathbf{H}, \quad \mathbf{D} = \varepsilon \mathbf{E}, \quad \mathbf{J} = \sigma \mathbf{E}$$

To be solved with initial and boundary conditions

Numerical computation of EM field

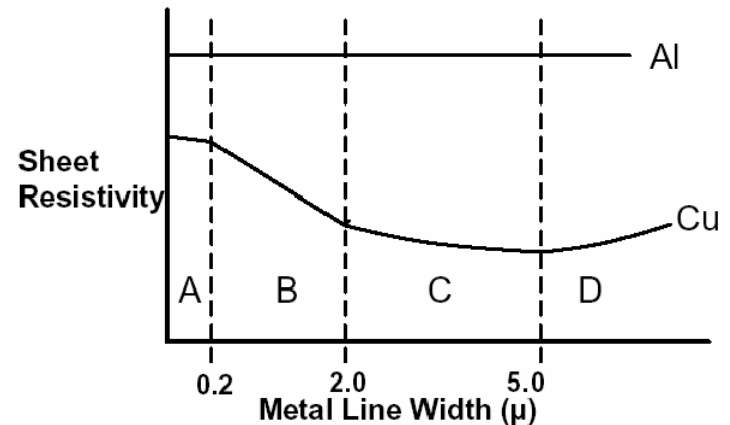
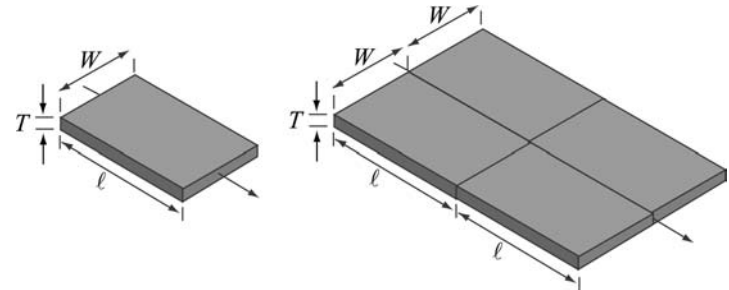


Interconnect Resistance (R) - 1

- Resistance of a rectangular conductor is given by:

$$R = \rho_s \cdot \frac{\ell}{W}$$

- To obtain resistance R of a wire, simply multiply ρ_s , by the ratio of length-to-width of the wire.
- Remember, **resistance is a function of conductor geometry and conductivity only.**
- Sheet resistance of Cu wire is function of line width and pattern density.**



Section A: Barrier Sidewall Thinning
 Section B: Cu Grain Size Reduction
 Section C: Increasing Effect of Sidewall
 Section D: CMP Dishing

Resistance (R) - Skin Effect

- As signal frequency increases, penetration depth (skin depth, δ) of the em field into the conductor decreases

$$\delta = \frac{1}{\sqrt{\pi f \mu \sigma}}$$

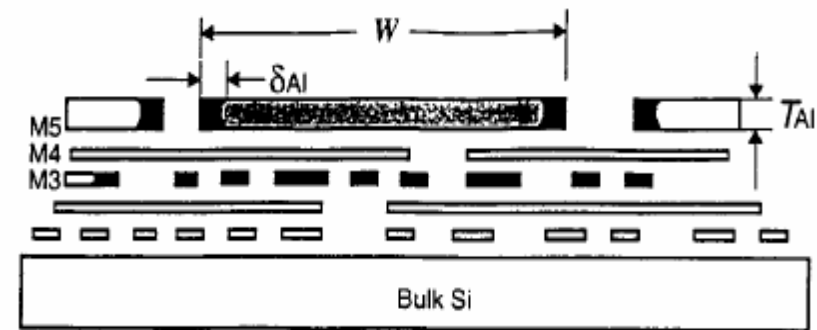
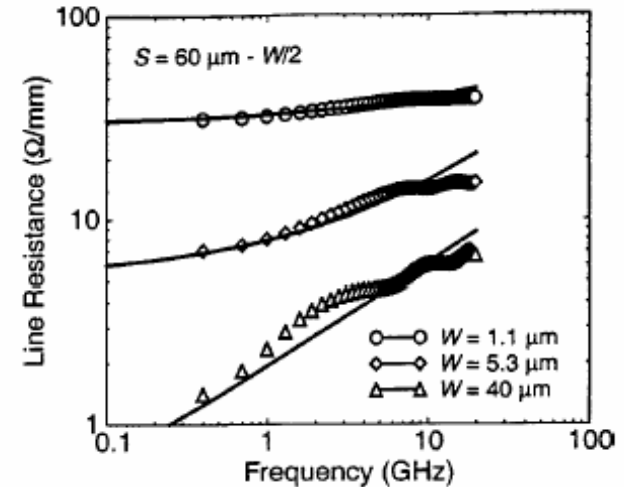
thereby increasing conductor R.

- Simple line

$$R = \frac{\rho \cdot l}{W \cdot \delta_{Al} \cdot (1 - e^{-T_{Al}/\delta_{Al}})}$$

- Line mimic real structure

$$R = \frac{\rho \cdot l}{T_{Al} \cdot 2 \cdot \delta_{Al} \cdot \left(1 + \frac{W}{20}\right) \cdot (1 - e^{-W/(2 \cdot \delta_{Al})})}$$



Cross section illustration of lateral skin effect for wide lines.
 Cleveland et al. IEEE Solid State Circuits
 Vol. 37, No. 6, 2002

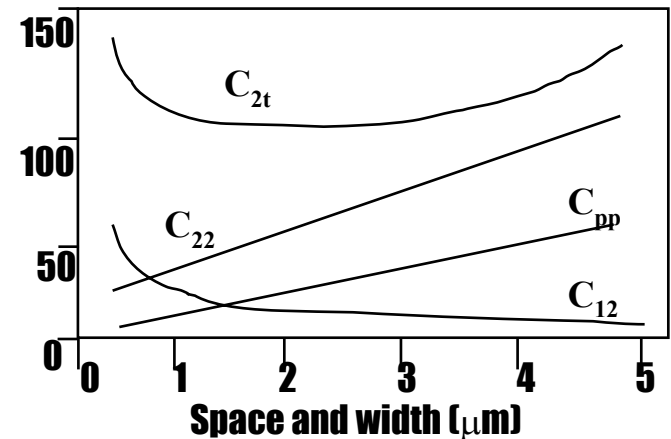
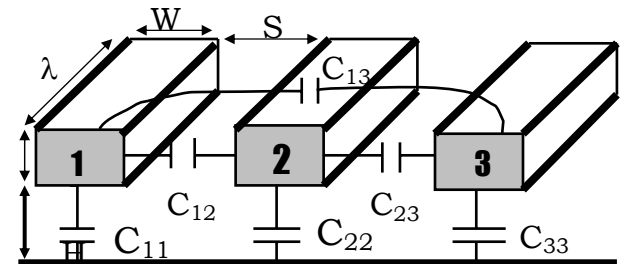
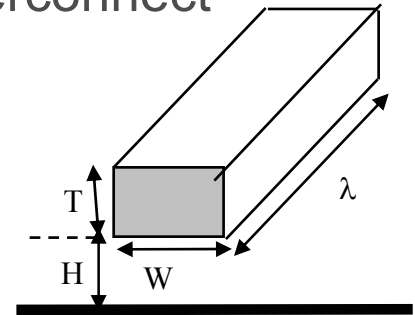
Interconnect Capacitance (C) - 1

- Fundamental expression for the computation of interconnect capacitance is the **parallel plate formula**

$$C = \epsilon \cdot W \lambda / H \quad (1)$$

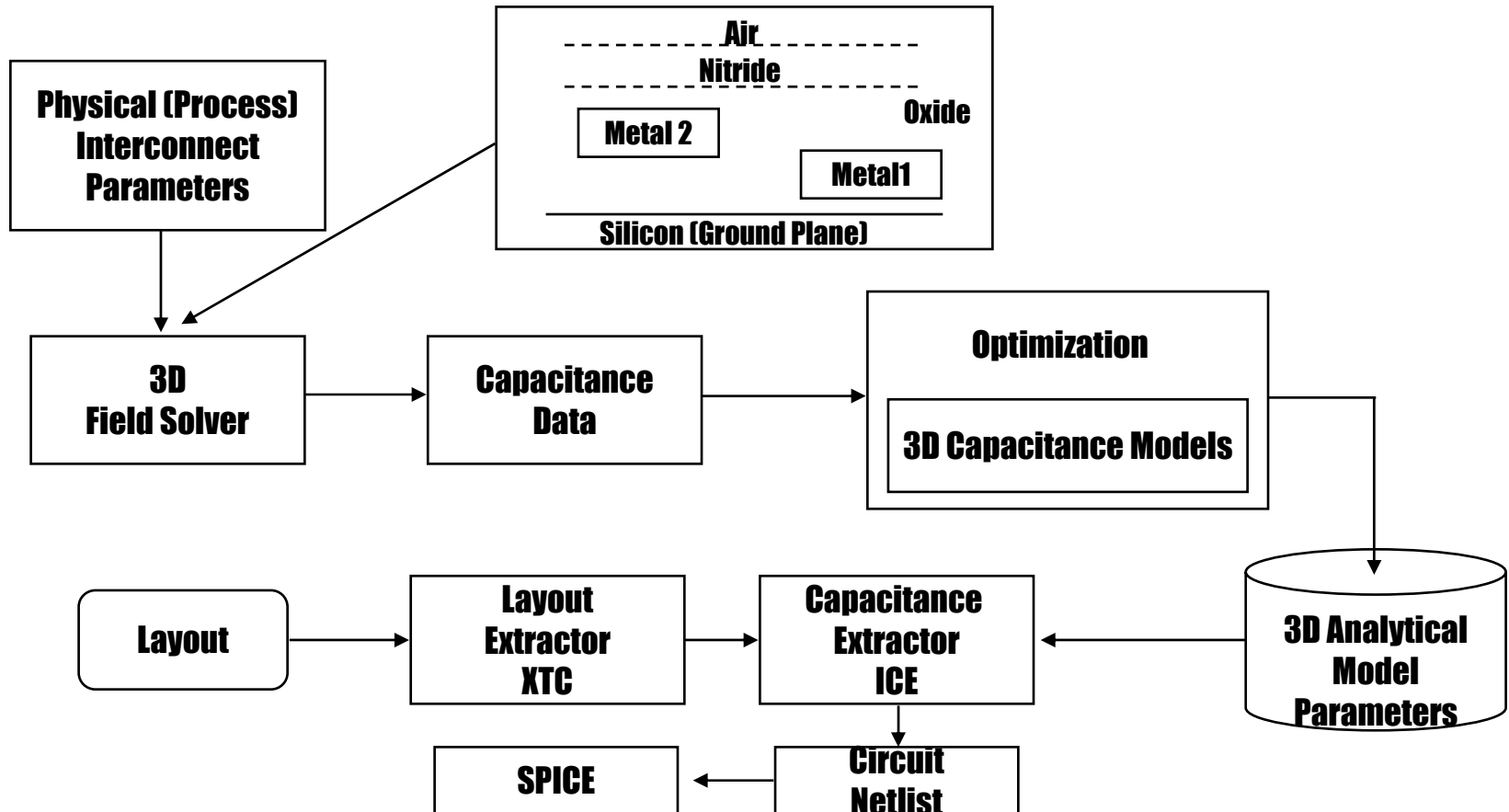
Assumptions - T negligible and $W \gg H$.

- Due to finite T and W of the line, with dimensions comparable to ILD, fringe capacitance is significant.
- It is customary to define 3 different components:
 (1) overlap, (2) lateral, and (3) fringe, though such distinctions are artificial.
- Physically speaking capacitance is a 3D **electromagnetic** problem.
- Total capacitance of conductor 2
 $C_{2t} = C_{12} + C_{23} + C_{22}$



Chip Level R, C Extraction

- Procedure for chip level RC extraction: [Ref. Arora et al., IEEE CAD-15, p58 (1996)]



Interconnect Inductance -1

- Inductance, by definition, is for a loop of a wire (wider the current loop, higher the inductance).
- Inductance of a wire in an IC requires knowledge of return path(s)
 - the V_{ss} or V_{dd} closes loop for each piece of interconnection.
- Often return path is not easily identified, particularly at layout stage as it is not necessarily through the silicon substrate. Concept of partial inductance (PI) is introduced which allows algebra to take care of determining the loops (A.E. Ruehli. IBM J. Res. Dev. 16, pp 470-481, 1972)
- Each partial inductance assumes current return at infinity.
- Based on PI approach,

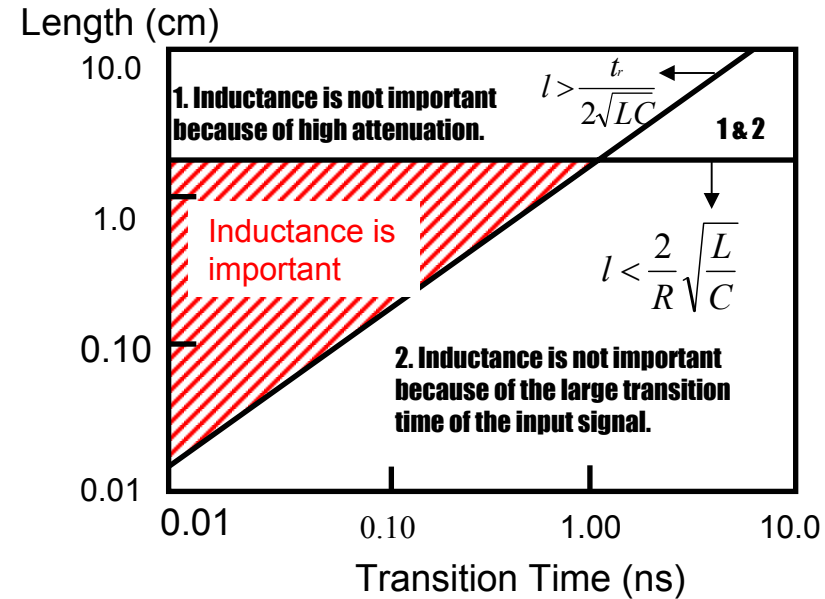
$$L_{self} = \frac{\mu_0}{2\pi} \left[l \cdot \ln \left(\frac{2l}{w+t} \right) + \frac{l}{2} + 0.2235l(w+t) \right]$$

$$M = \frac{\mu_0 l}{2\pi} \left[\ln \left(\frac{2l}{d} \right) - 1 + \left(\frac{d}{l} \right) \right]$$



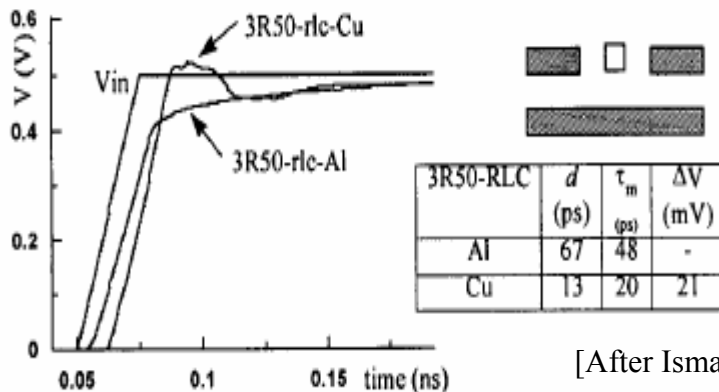
Comparison of L, C

- Unlike capacitive coupling, inductive coupling is much stronger (has long range effects). As such localized **windowing** is not easy. **Challenge is how far to go ?**
- Wire capacitance is important for any length, while **wire inductance is significant only for certain range of wire length.**
- **Inductance for Cu is higher**



[After Ismail et al. DAC 1998 p. 560]

Inductance is reduced by design using metal plane or interdigitated shield



[After Ismail et al. IITC 2000 p. 560]

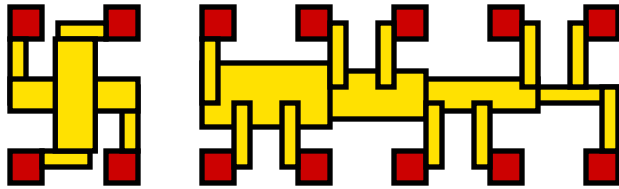
Interconnect Characterization

- Two ways of characterizing interconnects are :
 1. Use the **Field Solvers** that are based on Maxwell's equations (**soft validation**).

Inherent assumption is that process parameters that are input to the solver are correct (from silicon prospective).

2. **Test chips** fabricated on Silicon Wafers for a given technology, measuring the capacitance of those structures (**Silicon validation**).
Though expensive and time consuming, it is the only way to do correct model validation.

Test Structure For Resistance Extraction

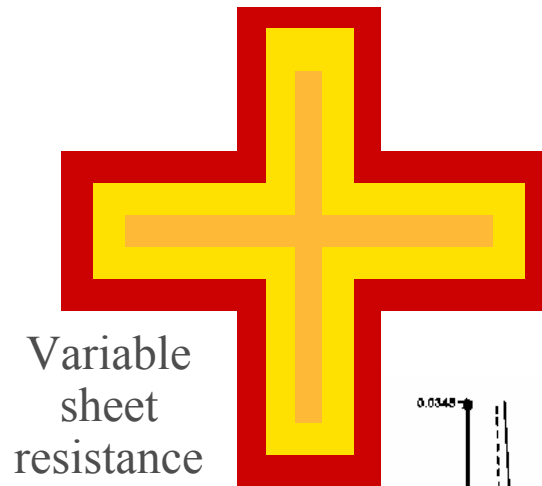


- Cross Bridge

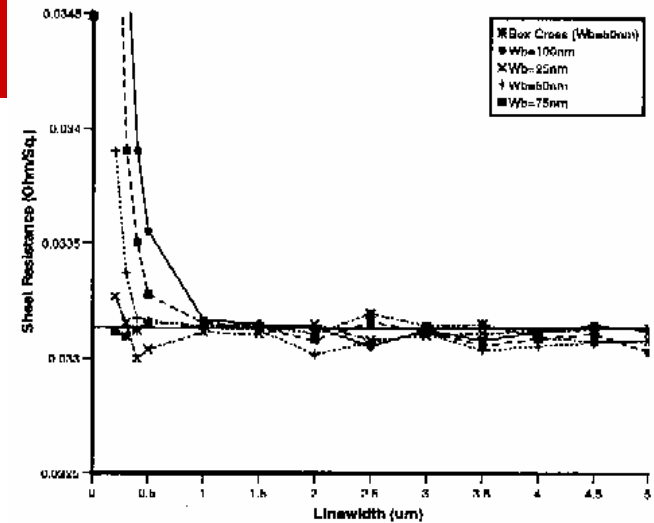
- Sheet Resistance
- Line CD W and δW
- Barrier Layer resistivity
- Thickness Measurement
- CMP Dishing

- $R = V/I$

- $R_s = \pi R / \ln 2$



Dishing

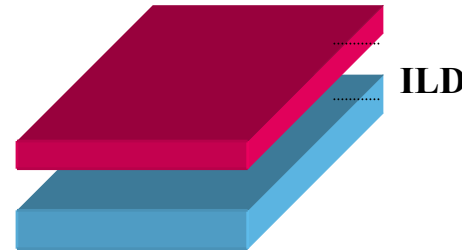


Extracted sheet resistance versus copper linewidth for simulated Greek cross structures with barrier layers.

Smith et al. ICMTS, 2001

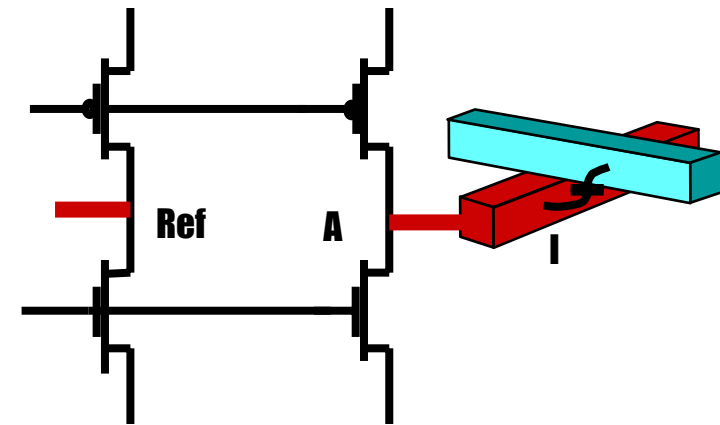
Test Structure For Capacitance Extraction

- Most commonly used test structures for characterizing interconnects, are the so called, **passive structures**, of the following type
 - parallel plate over a parallel plate
 - parallel plate over fingers
 - fingers over a parallel plate
 - interdigitated fingers
 - interdigitated fingers over a plate



Active Approach:

C , of the interconnect I is determined by measuring the difference in the dc drain currents, I_{avg} , of the two “pseudo inverters” Ref and A such that [Chen et al. Proc. IEDM, December 1996]

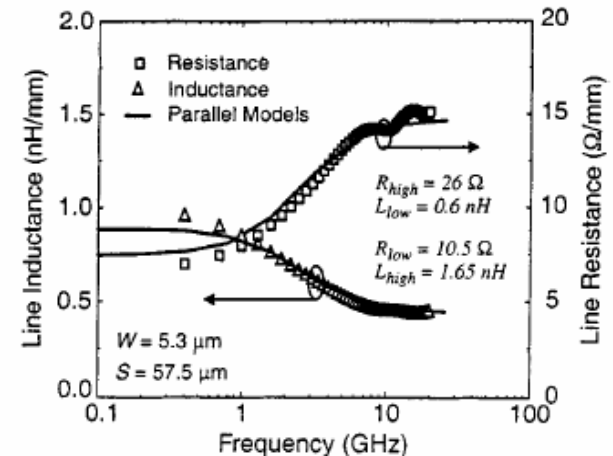
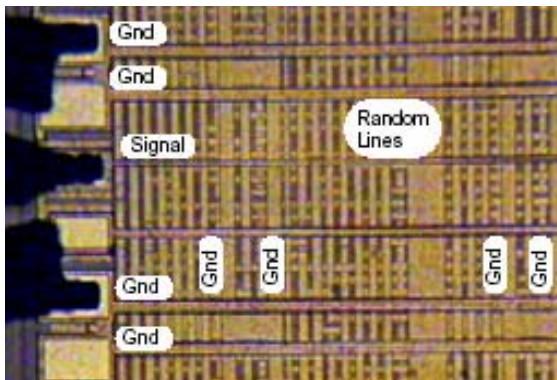


CBCM Method

$$C = V_{dd} \cdot f / (I_A - I_{ref}) = V_{dd} \cdot f / I_{avg}$$

Inductance Characterization – S Parameters

- S parameters are measured on Test structures that mimic a real chip layout
- These parameters are then converted into Y parameters and models are developed from which we extract resistance and inductance.



Kleveland et al. IEEE
Solid State Circuits
Vol. 37, No. 6, 2002

Process variations

- Due to manufacturing tolerances, interconnect related process variations
 - **Interlevel dielectric thickness (H)**
 - **Metal width (W) and thickness (T)**
 - **Dielectric uniformity**
 - **Line sheet resistance**
- In addition these parameters are also dependent on
 - Layout
 - Local pattern density
- Parameters change from die-to-die, wafer-to-wafer, lot-to-lot resulting in R, and C which could be 20% of the typical value.
- Geometry specific variations
- In circuit design one normally should use worst case value (maximum W and thinnest H) for *delay* and dynamic *power* calculations, while for *race* calculations minimum W and maximum H be used.

Statistical Analysis

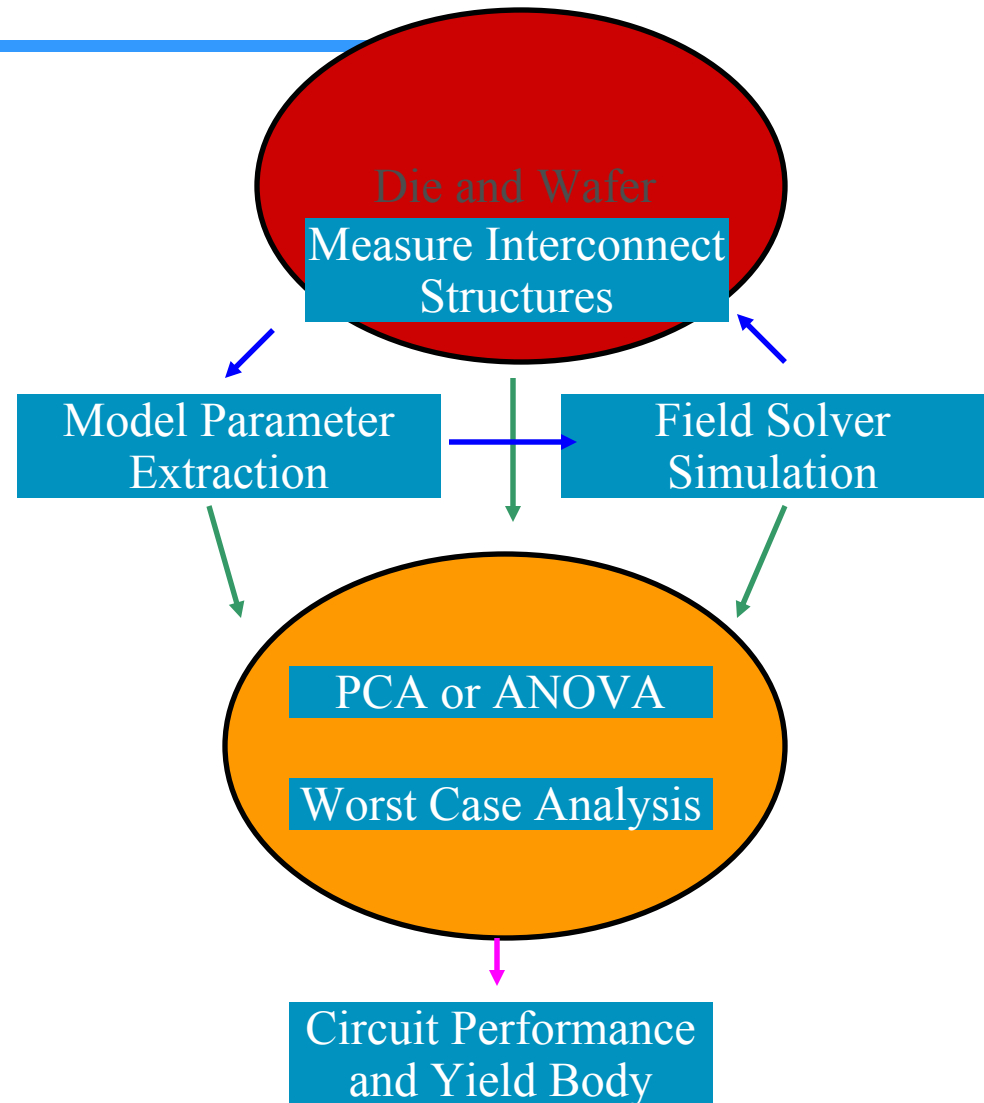
- Variation Analysis

- Principle Component Analysis (PCA)
- Analysis of Variance (ANOVA)

- Worst Case Analysis

$$\delta e_i = \sum_k \frac{\partial e_i}{\partial p_k} \delta p_k$$

$$\sigma^2_{\delta e_i} = \sum_k \left(\frac{\partial e_i}{\partial p_k} \right)^2 \sigma^2_{\delta p_k}$$



- Accurate characterization and modeling of VLSI interconnects is important because it affects chip design through, timing, signal integrity and reliability of the chip.

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