A Physics-Based Compact Model for Nano-Scale DG and FD/SOI MOSFETs

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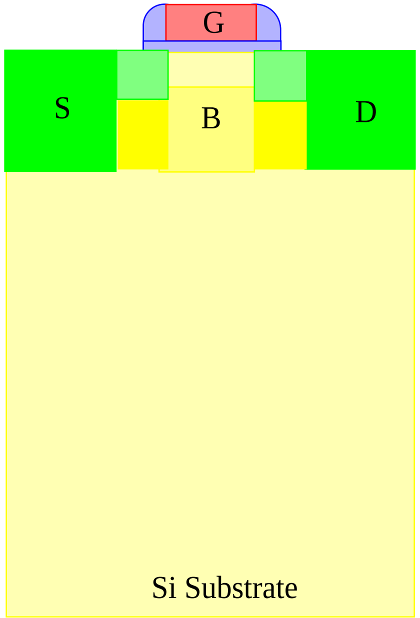
Outline

- Introduction
- UFDG Overview/Verification
- UFDG Applications
- Summary

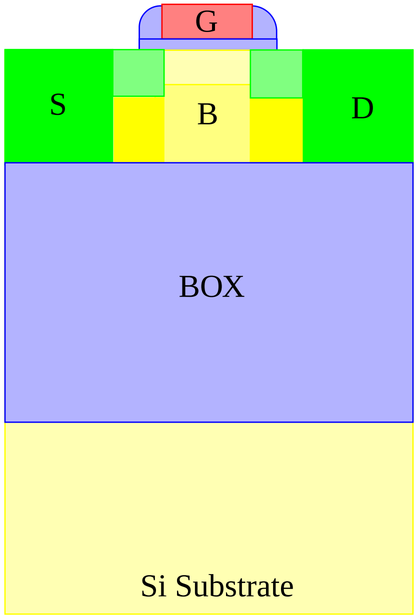
CMOS Scalability to $L_{gate} < 50nm$?

Bulk Si



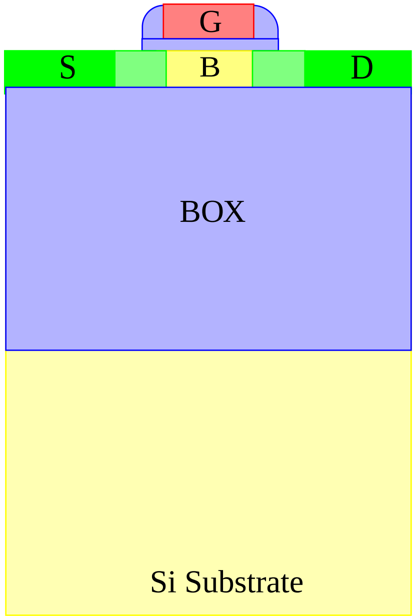
No.

PD/SOI



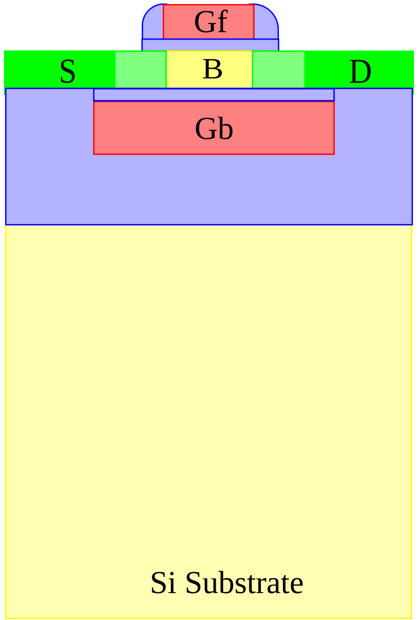
No,
but with performance advantage over bulk Si to the scaling limit, which can be enhanced in strained Si/SiGe technologies .

FD/SOI



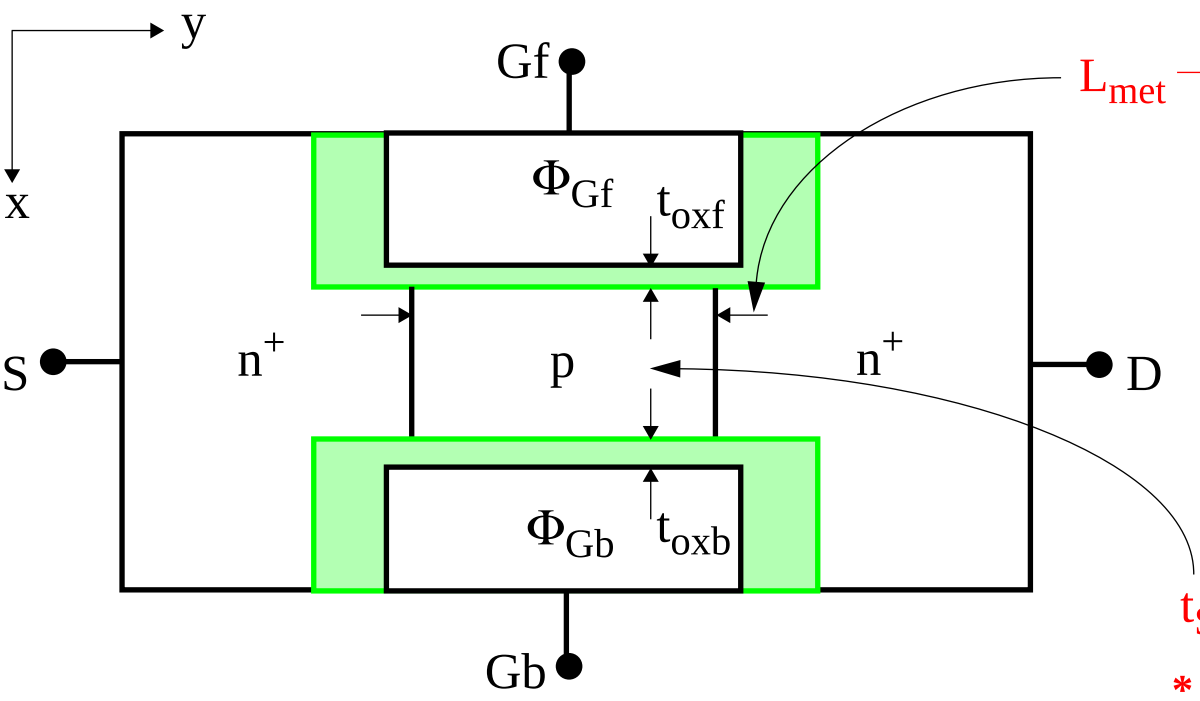
Maybe,
but how far depends on how thin the Si-film body can be made; $t_{Si} < 10nm$ will be needed.

DG



Yes;
thin Si is needed, but optimal structure is not yet known. Thicker oxides and longer channels could yield superior performance relative to anything else.

DG MOSFET: Challenging Technology, Complex Physics, Superior Features



$L_{met} \rightarrow 10\text{nm} \Rightarrow$

- short-channel effects (SCEs)
- quasi-ballistic/ballistic transport
- thermal injection velocity (v_{inj})
- quantum transport (S-D tunneling)

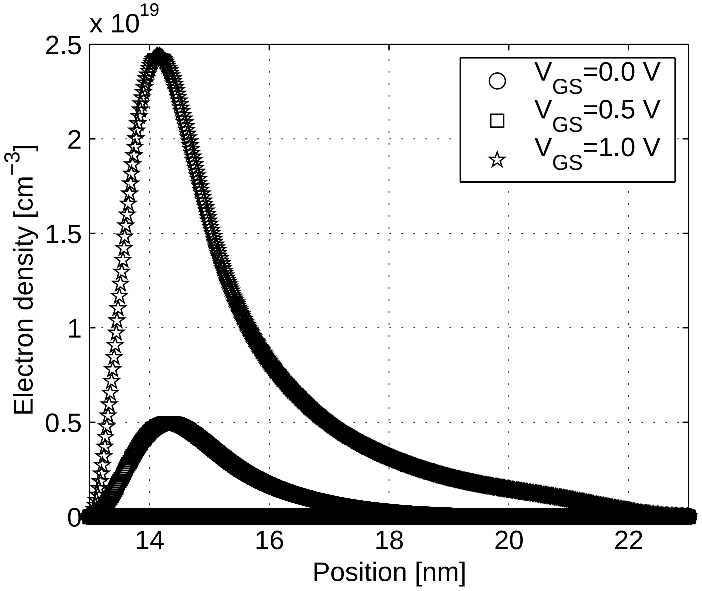
$t_{Si} < 10\text{nm} \Rightarrow$

- Gf-Gb charge coupling
- t_{Si}-dependent quantization (QM)
- 2D DOS with Fermi-Dirac statistics
- volume inversion
- QM-defined μ_n and v_{inj}

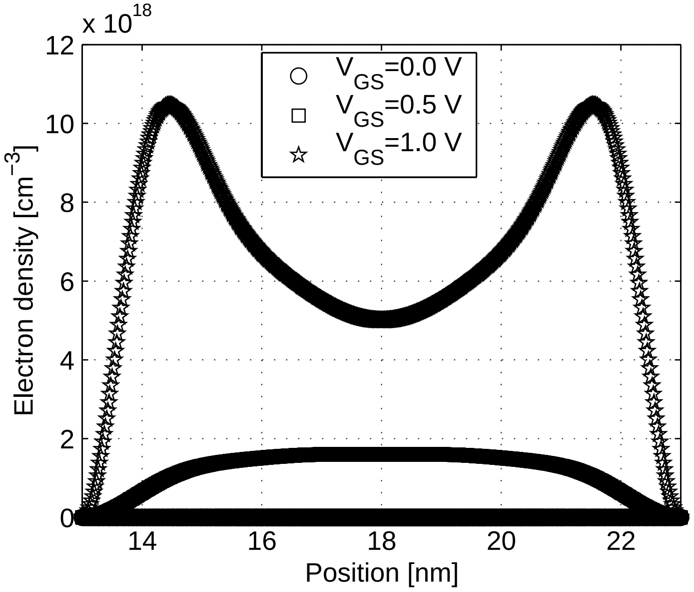
The gate charge coupling underlies several unique, advantageous features of the intrinsic DG MOSFET.

SCHRED-2*: n(x)

Asymmetrical DG nMOSFET



Symmetrical DG nMOSFET



Notes: Carrier degeneracy for high V_{GS}.

Different inversion-layer centroids, or average depths (t_i).

Asymmetrical device: one predominant channel (for moderate V_{GS}).

Symmetrical device: two channels for high V_{GS}; *volume inversion* for low V_{GS}.

*D. Vasileska and Z. Ren, Purdue Univ. , W. Lafayette, IN, Feb. 2000.

Process-Based Compact Device Modeling

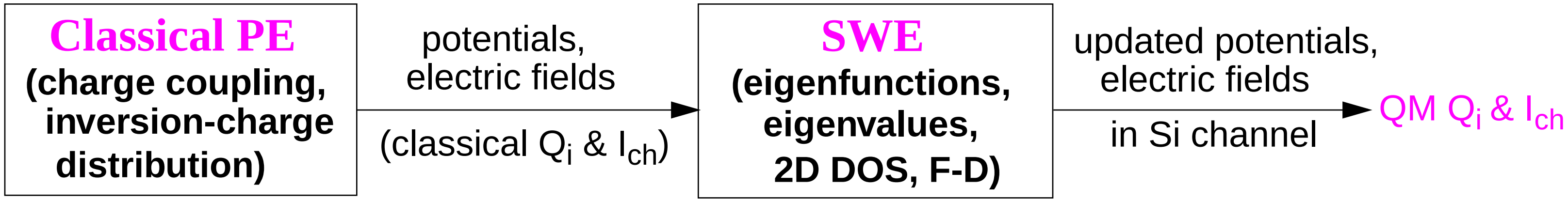
- Truly physics-based, with key simplifying approximations.
- Device structure-dependent, with relatively small number of parameters that relate directly to processing and physics.
- Straightforward parameter evaluation, with minimal measurement-based tuning of key parameters (like that needed for numerical device simulation).
- Predictive, enabling reliable IC TCAD, sensitivity analysis, next-generation performance projection, efficient mixed-mode device/ circuit simulation, as well as reliable circuit design and analysis with strong link to technology. Can aid advanced device design and technology development.
- UFPDB for bulk-Si and PD/SOI MOSFETs; now UFDG .....

UFDG: Generic Process-Based Compact Model for DG MOSFETs

- Is being developed to project performance of DG CMOS, accounting for parasitics as well as the intrinsic features of DG MOSFETs, and to thereby aid its design optimization.
- Weak-inversion formalism based on approximate 2D Poisson solution (with SCEs), with QM-defined shifts of surface potentials ($\Delta\phi_{w(QM)}(E_0)$) and predominant diffusion current.
- For strong inversion, solve classical 1D Poisson: $\frac{d^2\phi}{dx^2} \cong \frac{q}{\varepsilon_{Si}} n(x)$ (nMOSFET); then link, via derived $\phi(V_{GfS}, V_{GbS})$, to iterative solution of Schrödinger (ψ_j, E_j), via variational approach with 2D DOS and Fermi-Dirac statistics, for updated $Q_i(E_j)$, $\phi(x)$: compact self-consistent Poisson-Schrödinger solver.
- Model quasi-ballistic transport via $\mu_n(E_x, t_{Si})$ (based on QM modeling) and $v_{sat(eff)}$ (> v_{sat} for carrier velocity overshoot) with v_{inj} (ballistic) limit.
- Integrate $I_{ch} = -WQ_i(y)v(y) + WD_n\frac{dQ_i(y)}{dy}$ from S to D to get $I_{DS}(V_{GfS}, V_{GbS}, V_{DS}, V_{BS})$, modeling v(y) in terms of E_y, μ_n, and (bias-dependent) $v_{sat(eff)}$, and including t_{Si} dependences.
- Define correlated terminal charges: $Q_j(V_{GfS}, V_{GbS}, V_{DS}, V_{BS})$, j = G_f, G_b, D, S, B.
- Use spline interpolation of I_{ch} and Q_j for moderate inversion, defined by bias-dependent V_{GfS} boundaries (V_{TW} and V_{TS}). Truly physics-based modeling is thereby facilitated.

UFDG:

A Generic Compact Poisson-Schrödinger Solver for FD/SOI as well as DG MOSFETs



Classical PE
(charge coupling, inversion-charge distribution)

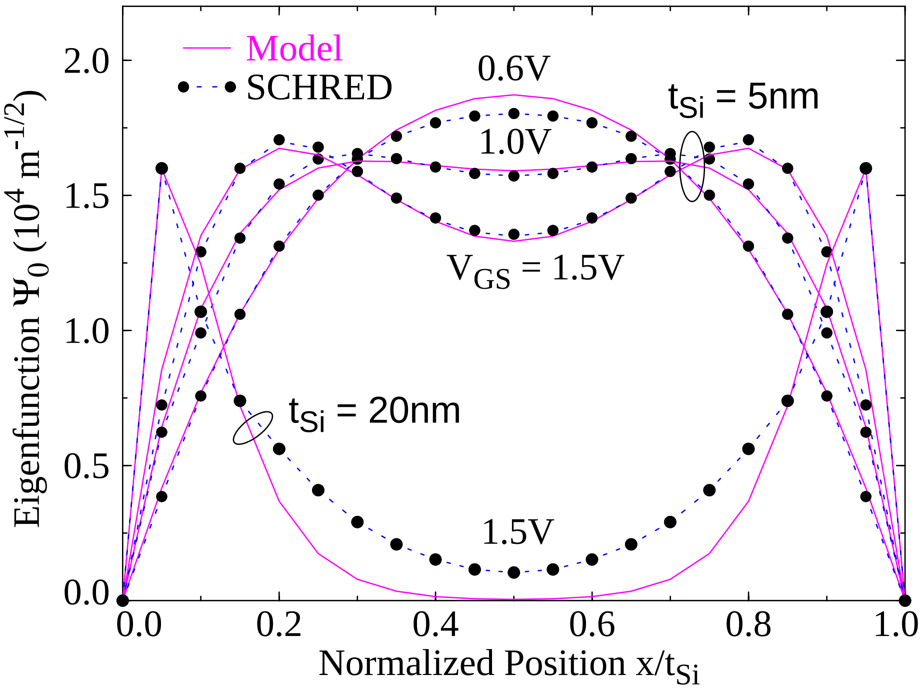
potentials, electric fields
(classical Q_i & I_{ch})

SWE
(eigenfunctions, eigenvalues, 2D DOS, F-D)

updated potentials, electric fields
in Si channel

QM Q_i & I_{ch}

SWE analytical solution is derived using a variational approach, then coupled to PE and $Q_i(V_{GfS}, V_{GbS})$ via Newton-Raphson iteration.



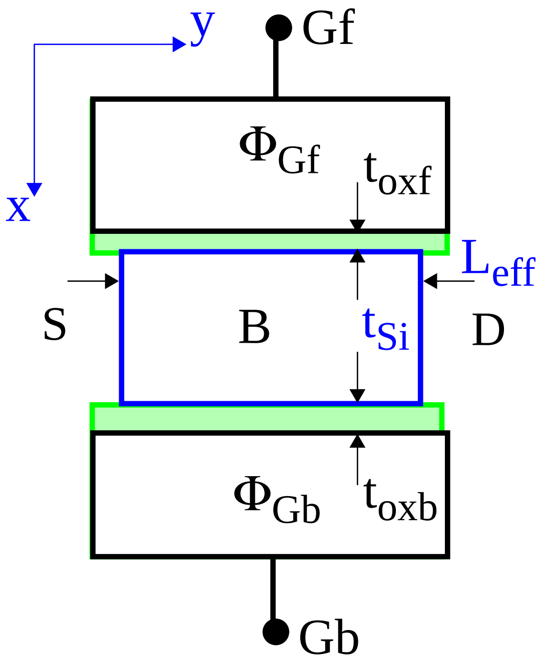
Sym. DG nMOSFETs:
n^+ gates
t_{ox}=1.5nm
N_A=$10^{17}$$cm^{-3}$

The QM solution is also the basis for the $\mu_n(E_x, t_{Si})$ modeling, accounting for volume-inversion effects.

Short-Channel Effects (SCEs)

2D Poisson equation (for weak inversion),

$$\frac{\partial^2\psi}{\partial x^2} + \frac{\partial^2\psi}{\partial y} \cong \frac{qN_{CH}}{\varepsilon_{Si}} ,$$



is solved in (rectangular) body/channel (B) region by assuming

$$\phi(x, y) \cong \alpha_0(y) + \alpha_1(y)x + \alpha_2(y)x^2$$

in Poisson, and applying the (four) boundary conditions (including surface-state charge at the gate-channel interfaces). The derived potential defines the (classical) integrated (over x) inversion charge (Q_i) and an effective channel length ($L_e < L_{eff}$) for predominant diffusion current (in y), and thus accounts for:

- S/D charge (impurity and/or carrier) sharing [$V_t(L_{eff})$ & $S(L_{eff})$] ,

- DIBL (front and back interfaces) [$\Delta V_t(V_{DS})$] .

QM Modeling (e.g., for nMOSFET)

- Trial Eigenfunction for Asymmetrical (Generic) DG Device:

$$\psi_j(x) = \frac{a_j}{2}\sqrt{\frac{2}{t_{Si}}}\sin\left(\frac{(j+1)\pi x}{t_{Si}}\right)\left(e^{-b_j x/t_{Si}} + \eta e^{-b_j (t_{Si}-x)/t_{Si}}\right), \quad j = 0, 1, 2, \ldots ;$$

a_j are normalization constants, and η is a charge-partition parameter.

- Solve Poisson equation for the electric potential $\phi(x)$ in the Si-film:

$$\frac{d^2}{dx^2}\phi(x) = \frac{q}{\varepsilon_{Si}}(N_A + n(x)) = \frac{q}{\varepsilon_{Si}}(N_A + N_{inv}|\psi(x)|^2) \Rightarrow \phi(x) .$$

- Use Schrödinger equation to get subband energies:

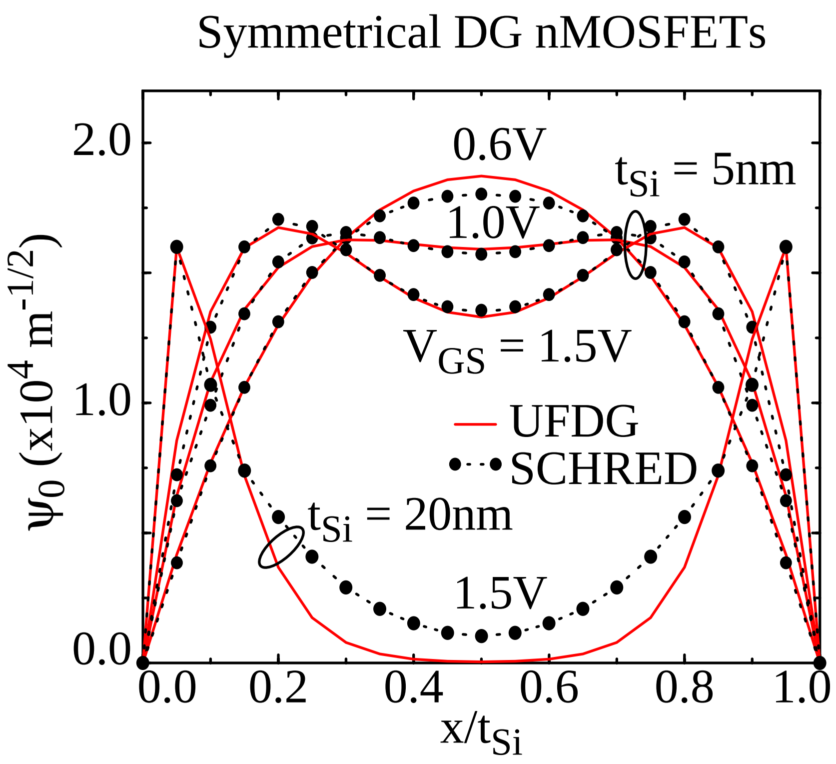
$$-\frac{h^2}{8\pi^2 m_x}\frac{d^2}{dx^2}\psi_j(x) + (-q)\phi(x)\psi_j(x) = E_j\psi_j(x) \Rightarrow E_j(b_j) .$$

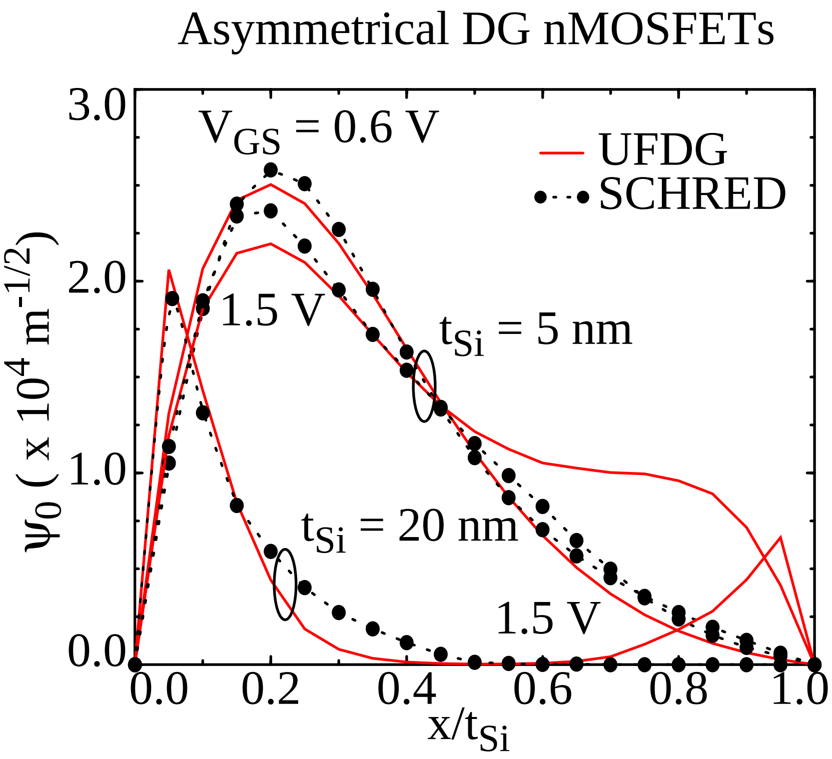
- Apply QM variational approach:

$$\frac{dE_j}{db_j} = 0 \Rightarrow b_j \cong t_{Si}\left(\frac{q m_x \pi^2\left(Q_{d(eff)} + \frac{5}{6}Q_i\right)}{(j+1)\varepsilon_{Si} h^2}\right)^{1/3}, \quad j = 0, 1, 2, \ldots$$

QM Model Verification via SCHRED (which defines Q_i here)

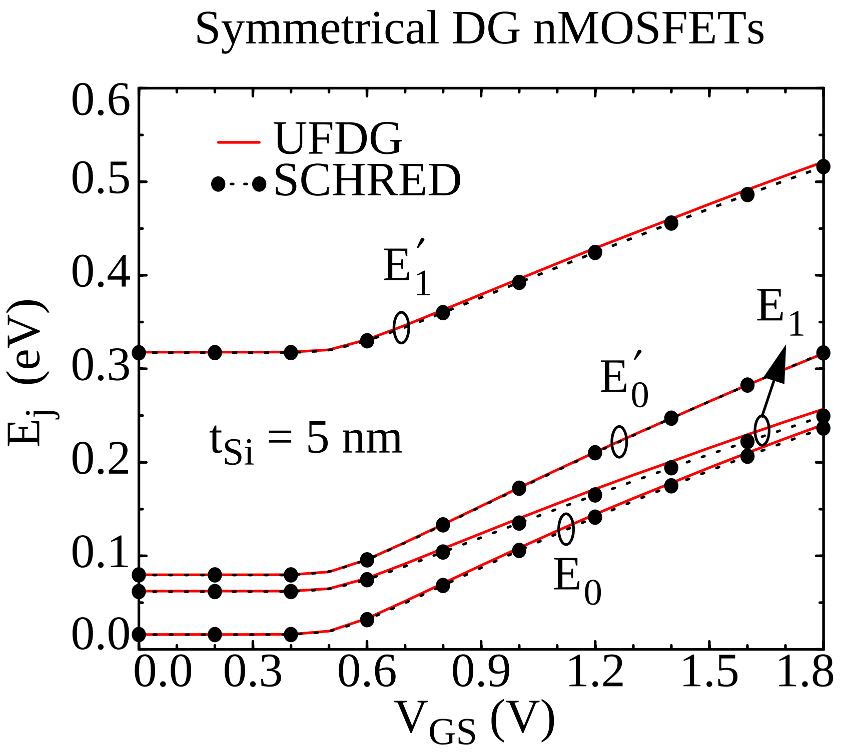
- Eigenfunctions

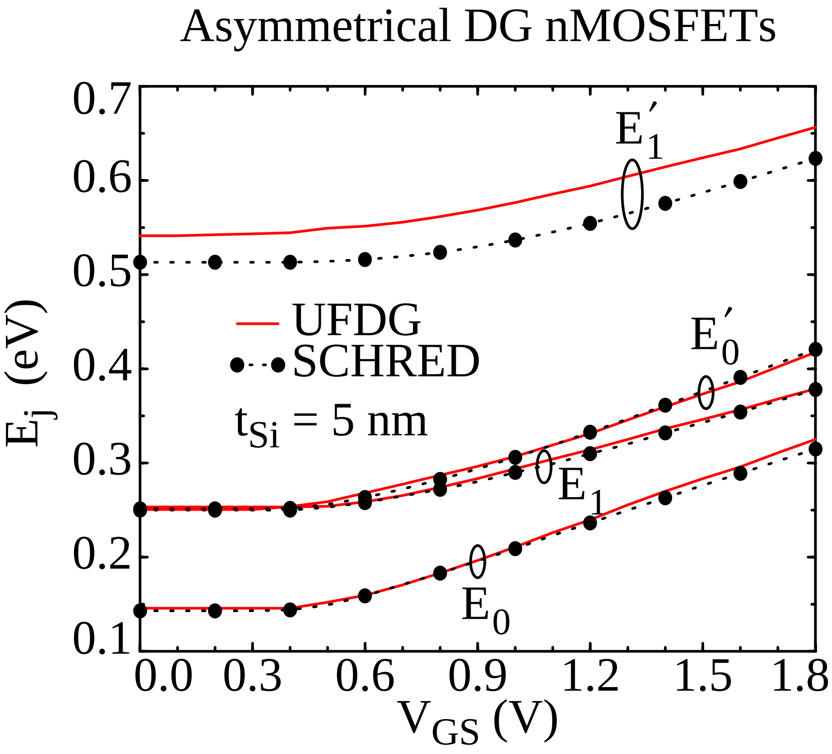




- For thin-t_{Si} symmetrical DG MOSFET, $V_{GS}\downarrow \Rightarrow$ volume inversion.

- Subband Energies

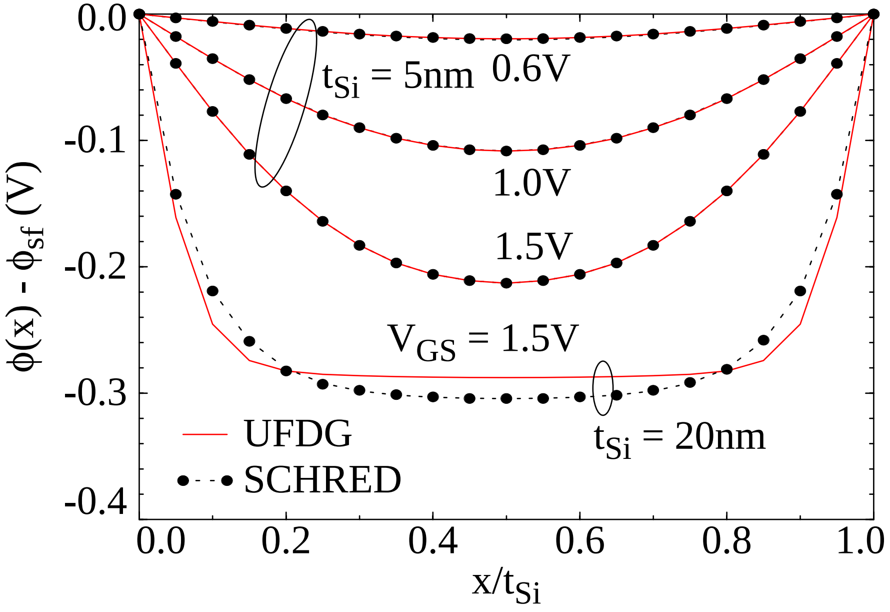




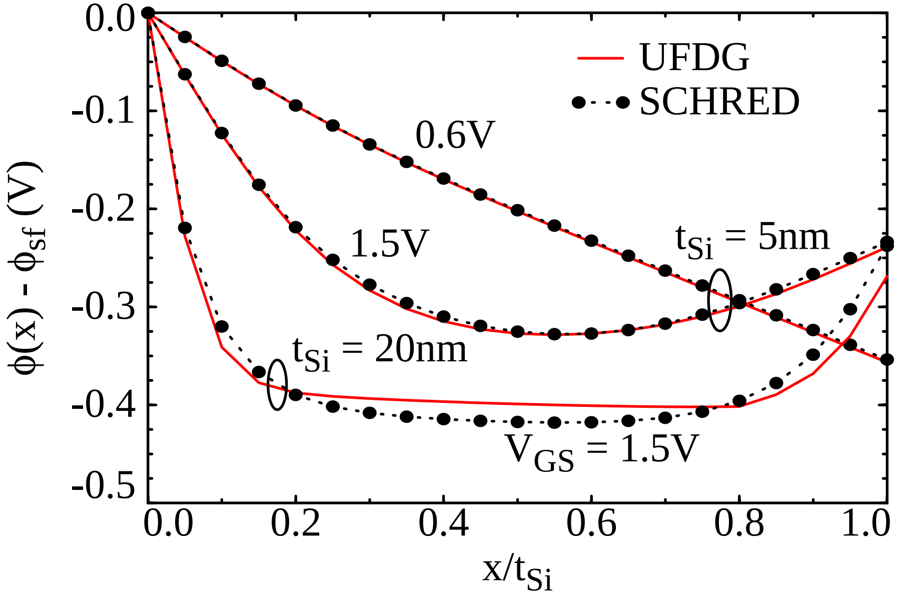
- QM effects are more significant in asymmetrical DG MOSFET.

- <u>Electric Potential</u>

Symmetrical DG nMOSFETs



Asymmetrical DG nMOSFETs



- Note that $n(x)$ does not correlate directly with $\phi(x)$ due to the quantization.

QM Model Implementation in UFDG (to get Q_i)

Weak Inversion: $\phi_{sf,b} = \phi_{sf,b(CL)} - \Delta\phi_{(QM)}[E_0(V_{GfS}, V_{GbS}, t_{Si})]$.

- Diffusion current follows from integration along channel ($0 < y < L_e$).
- 2D Poisson solution defines SCEs and effective channel length (L_e).

Strong Inversion: Inversion charge via Newton-Raphson Iteration:

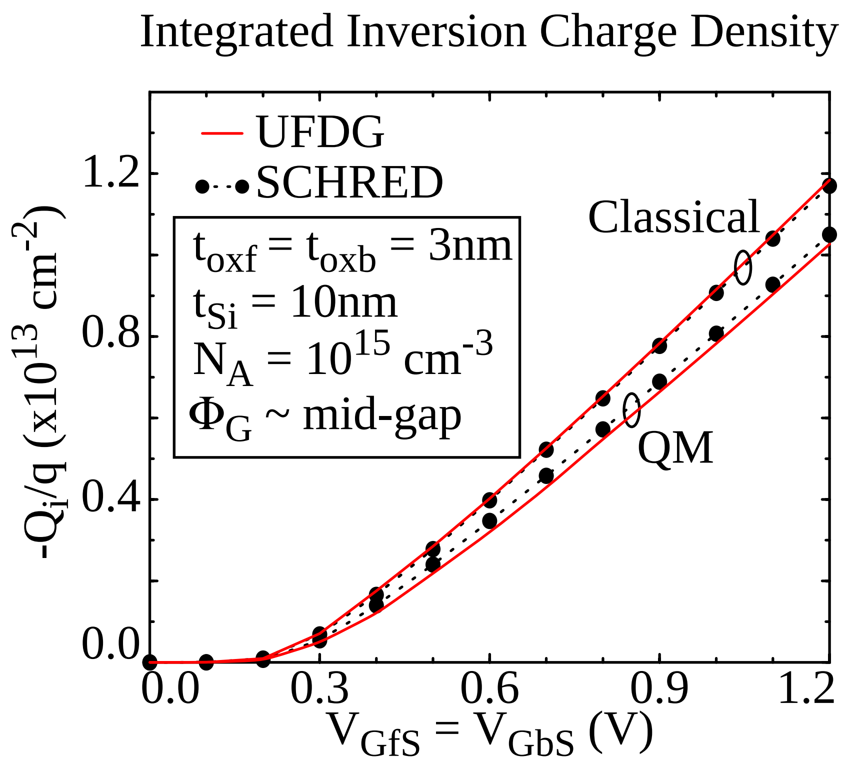
$$-Q_i = \frac{4\pi q k_B T}{h^2}\left(g m_d \sum_j \ln\left(1 + \frac{n_i^2}{N_c N_A}\exp\left(\frac{q\phi_{sf} - E_j}{k_B T}\right)\right)\right.$$
$$\left. + g' m'_d \sum_j \ln\left(1 + \frac{n_i^2}{N_c N_A}\exp\left(\frac{q\phi_{sf} - E'_j}{k_B T}\right)\right)\right) = \frac{C_{oxf}(V_{GfS} - V_{FB}^{f} - \phi_{sf})}{\gamma} \quad j = 0, 1 .$$

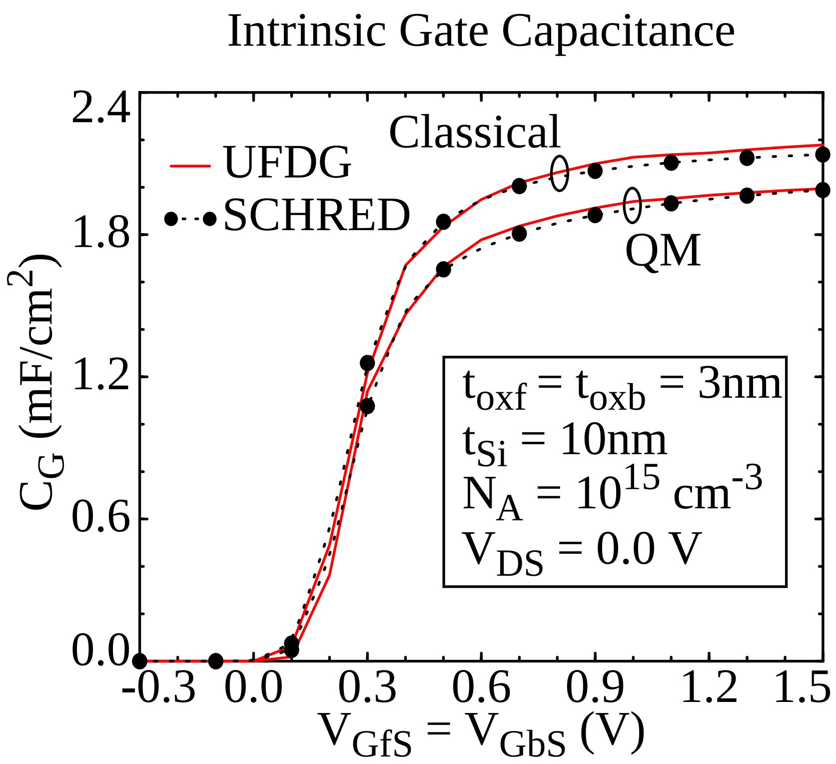
- Uncertainty in the effective mass m_x (m_x') and the 2-D density-of-states effective mass m_d (m_d') suggests two tuning parameters, QMX and QMD, which are generally unity: $m_x = m_x/$QMX and $m_d = m_d/$QMD.
- QMX is also used as a flag: QMX = 0 gives classical solution.
- Drift/diffusion current follows from integration along channel ($0 < y < L_e$).
- 2D Gauss solution near drain defines channel-length modulation ($L_{eff} - L_e$).

Moderate Inversion: V_{TW} and V_{TS} are increased via $\Delta\phi_{(QM)}[E_0(V_{TW,TS}, V_{GbS})]$.

More UFDG Verification via SCHRED

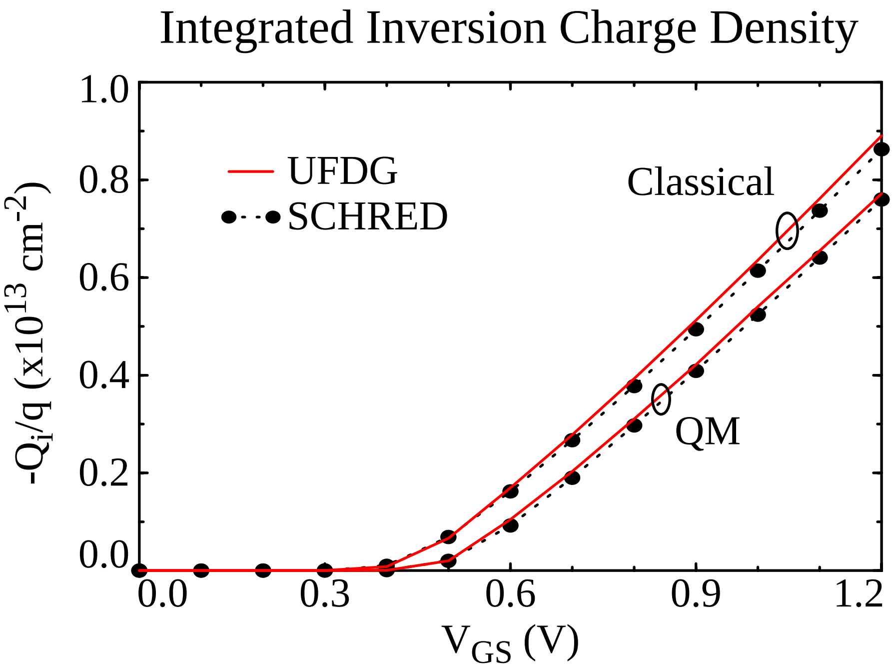
- Electrical Properties (Symmetrical DG nMOSFETs)

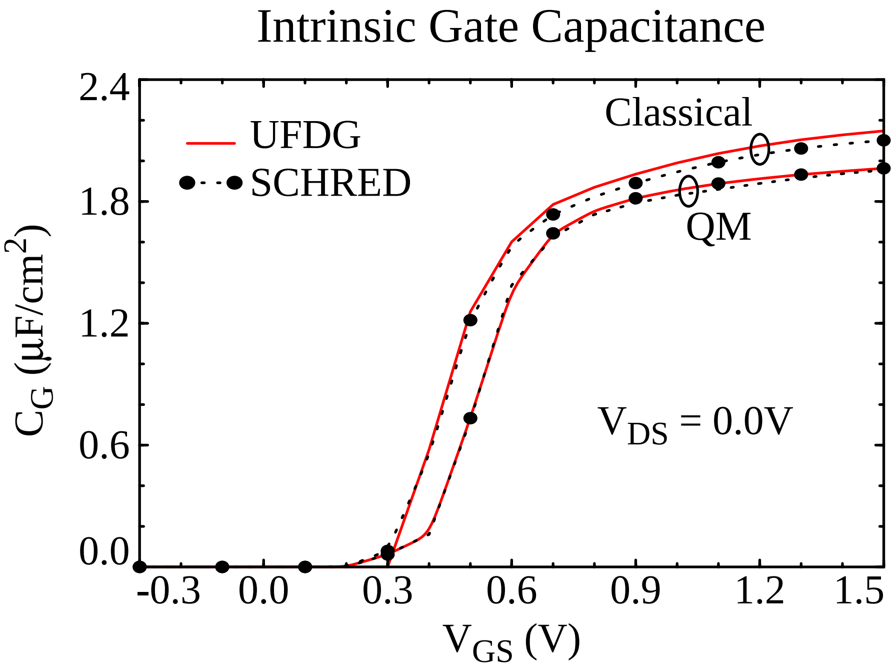




- UFDG has classical option; QM doubles run-time.

•Electrical Properties (Asymmetrical DG nMOSFETs)





- Note QM effects; no UFDG parameter tuning!

Physical (QM-Based) Mobility Modeling

Matthiessen Approximation:

$$\frac{1}{\mu_{eff}} = \frac{1}{\mu_{0(bulk)}} + \frac{1}{\mu_{co}} + \frac{1}{\mu_{sr}} + \frac{1}{\mu_{ph}} \Rightarrow \frac{1}{\mu_{eff}} = \frac{1}{\mu_{0}} + \frac{1}{\mu_{sr}} + \frac{1}{\mu_{ph}}$$

where $\mu_{0(bulk)}$ is the mobility in the bulk silicon defined by the doping density, μ_{co} is the carrier mobility limited by Coulomb scattering due to surface states, μ_{sr} is surface roughness-limited mobility, and μ_{ph} is phonon-limited mobility; μ_{co} is assumed constant, leading to μ_0.

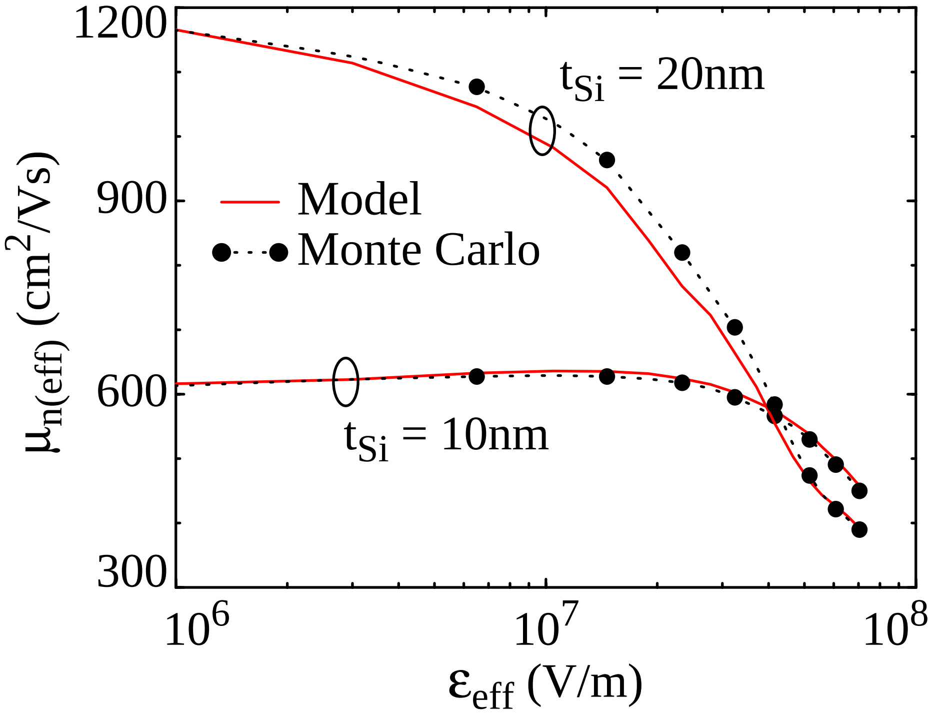
Both μ_{sr} and μ_{ph} are dependent on electric field as well as Si-film thickness, characterized via the Boltzmann transport equation and quantum-mechanical perturbation theory, and on the noted QM modeling, which defines the form factor for the phonon scattering and the matrix element for the surface-roughness scattering:

$$\mu_{eff} = \mu_{eff}[\psi_j(V_{GfS}, V_{GbS}, t_{Si})]$$

with only three parameters (μ_0, and θ_{ph} and θ_{sr} which are generally unity).

Mobility Model Verification via Monte Carlo*

Composite Mobility: Surface-Roughness + Phonon Scattering



SDG nMOSFET

$t_{oxf} = t_{oxb} = 3$nm

$N_A = 10^{15}$ cm^{-3}

Φ_G ~ mid-gap

- Note the strong ε_{eff} and t_{Si} dependences.

*F. Gámiz, et al., Proc. 10th Internat. Symp. SOI Tech. and Devices, May 2001.

More Physical UFDG Modeling

Physical accountings for impact ionization and quasi-ballistic transport (with velocity overshoot) are based on a simplified form of the energy-balance equation (i.e., the 2nd-order moment of the Boltzmann transport equation (BTE)):

$$\frac{d}{dy}(T_c(y) - T) + \frac{(T_c(y) - T)}{(5v\tau_w/3)} = \frac{2qE_y(y)}{5k_B}$$

where T_c is the carrier temperature [defined by the kinetic energy, which defines the impact-ionization rate (α) and the carrier mobility (μ)], E_y is the electric field along the channel, and τ_w is the energy-relaxation time. With $E_y(y)$ and the parasitic BJT modeled in UFDG, the impact-ionization current is then characterized as

$$I_{Gi}(T_c) = \int \alpha(T_c)dy\Big|_{high - E_y \ \ regions}(I_{CH} + I_{BJT})$$

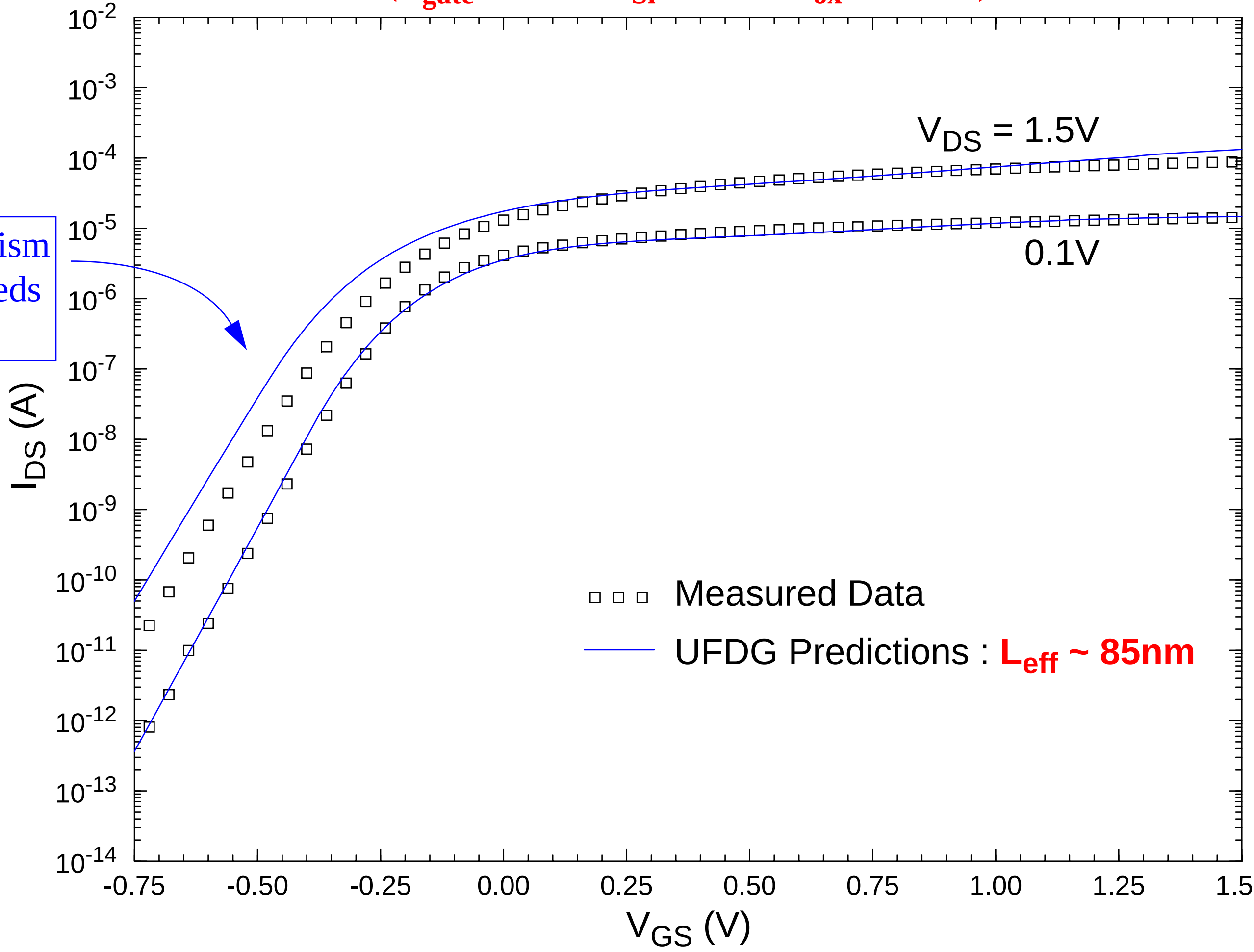
and, with the 1st-order moment of the BTE incorporated, an effective saturated drift velocity, reflecting overshoot, is defined as

$$v_{sat(eff)}(T_c) = \mu(T_c)E_y(y)\big|_{y = L_{met}} > v_{sat} \ .$$

UFDG Calibrations/Verification (just beginning)

DG nFinFET*

(L_{gate} = 65nm, t_{Si} = 45nm, t_{ox} = 3.3nm)



Self-heating?
(Turned off
in UFDG.)

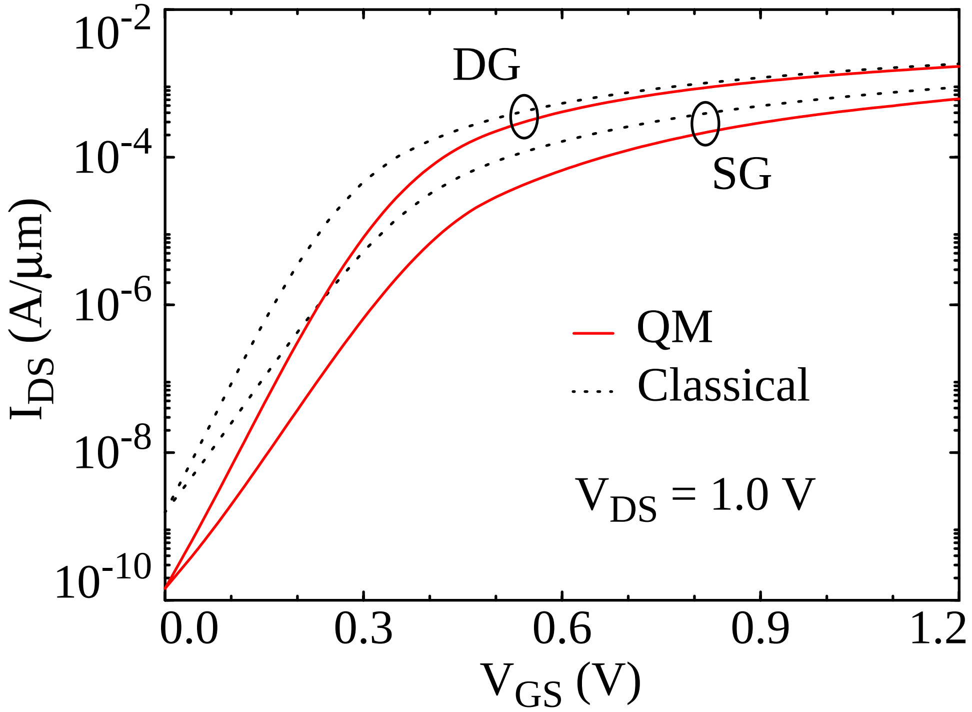
UFDG SCE formalism
(e.g., for DIBL) needs
to be refined.

Note that t_{Si} ~ $L_{eff}/2$ can yield well-controlled SCEs.

***Devices fabricated and characterized at Motorola, Austin, TX.**

UFDG Application: SG vs. DG CMOS

UFDG-Predicted Asymmetrical DG vs. SG nMOSFET Characteristics:



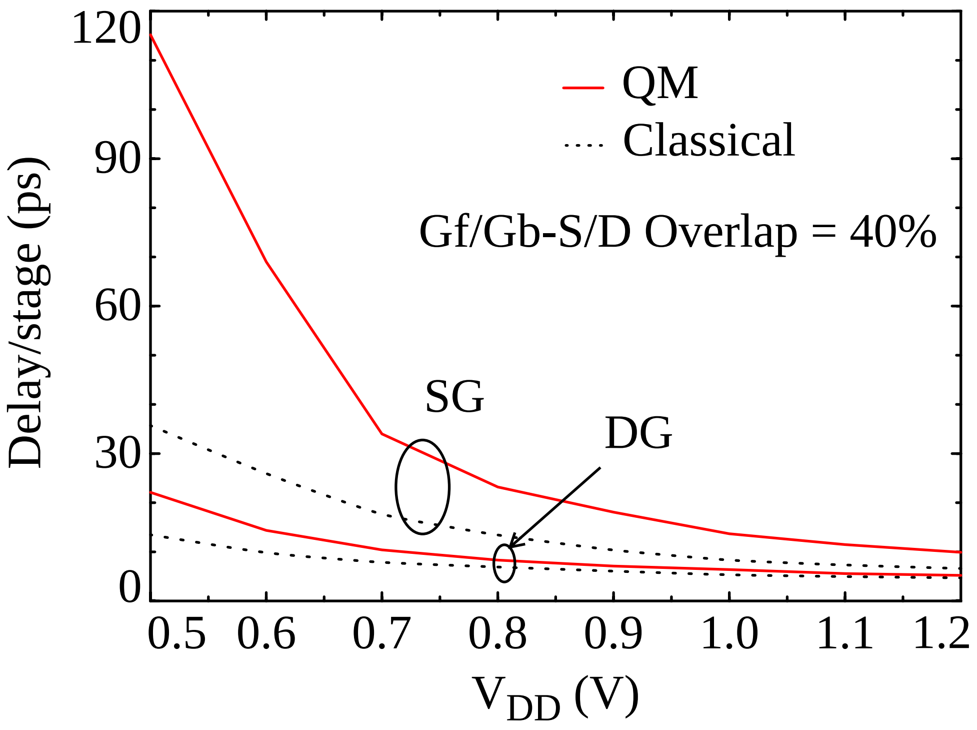
For UFDG simulations:

- $L_{eff} = 50$nm.
- $t_{oxf} = t_{oxb} = 3.0$nm.
- $t_{Si} = 10$nm.
- $N_A = 1\text{x}10^{15}$ cm^{-3}.
- n^+/p^+ polysilicon gates ($\Phi_{mf} = 4.05$V and $\Phi_{mb} = 5.13$V) for asymmetrical DG devices.
- SG is ADG device with back gate grounded.

- Both devices have the same I_{off}.
- SG is representative of bulk-Si devices. Note larger QM effect due to higher E_x.
- Note that polysilicon gates, with the QM effects, will not suffice for scaled DG.

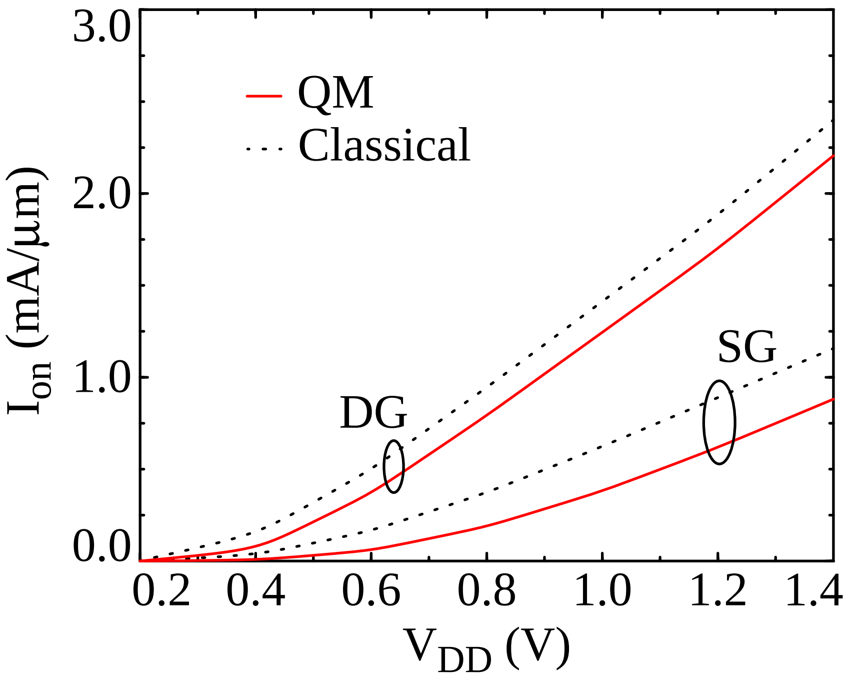
UFDG/Spice3 Speed-Performance Projections

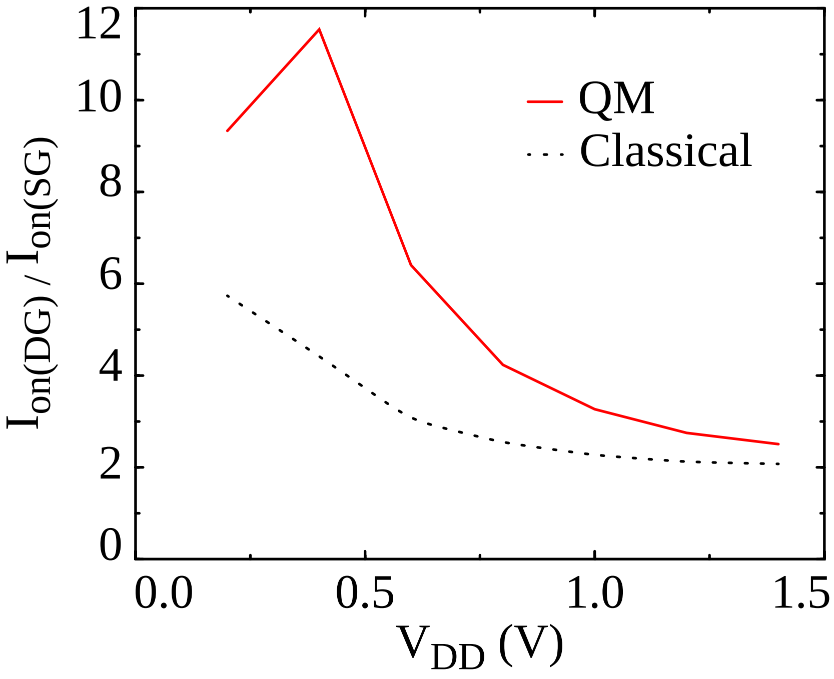
Intrinsic Propagation Delay from a 9-Stage CMOS-Inverter Ring Oscillator:



- DG CMOS is much faster; e.g., 41% faster than SG at V_{DD}=1.0V.
- The speed superiority is due to much higher I_{on} and not so much higher C_G.
- It is enhanced by QM effects (which are worse in SG devices).

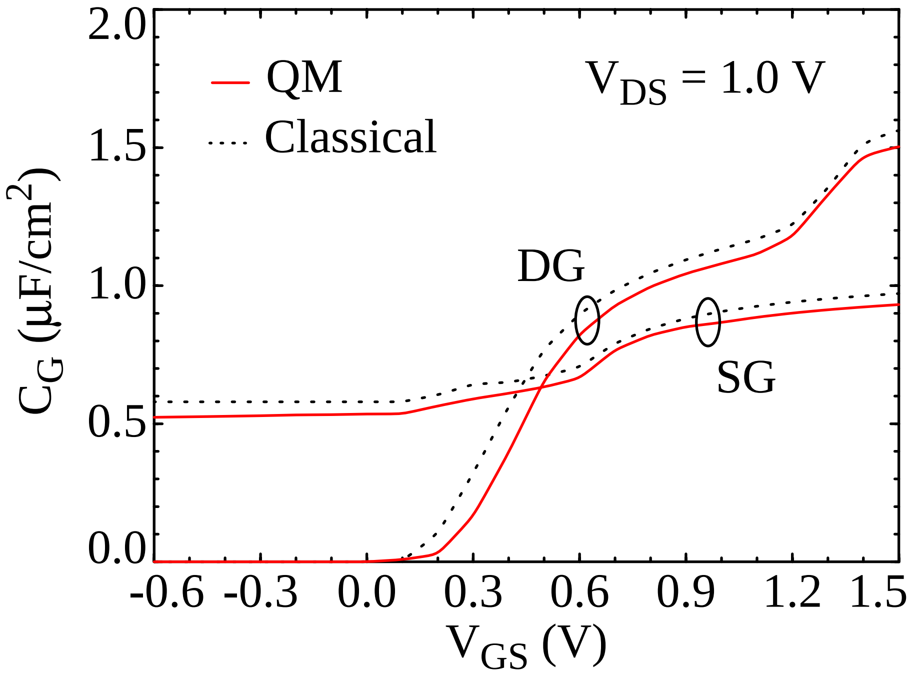
On-State Current (nMOSFETs):





- The DG-device I_{on} is greater than twice that of the SG counterpart at relatively low V_{DD}, due mainly to the near-ideal gate swing S and enhanced by QM.
  - Significant velocity overshoot, due to higher DG mobility, is also beneficial.

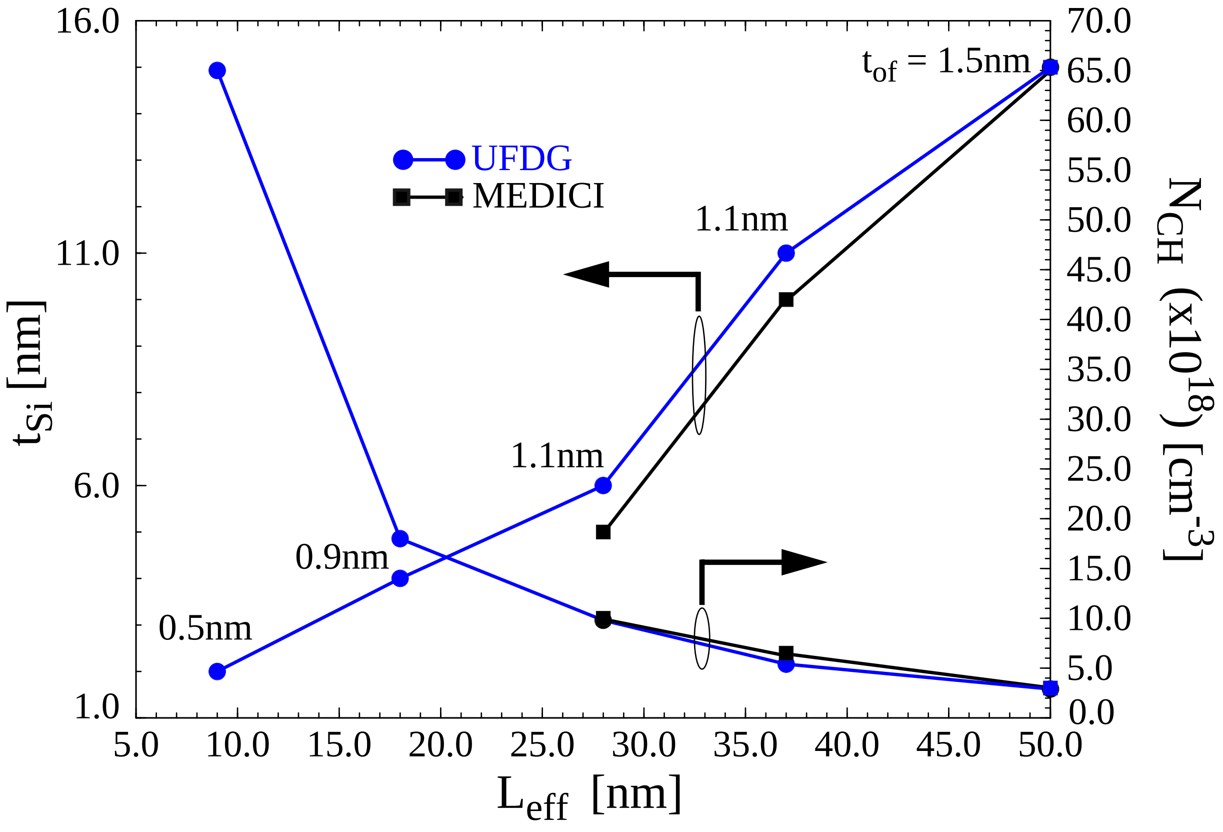
Intrinsic Gate Capacitance (nMOSFETs):



- The DG MOSFET C_G is near-zero in weak inversion.
- It is less than twice that of the SG counterpart in moderate inversion.

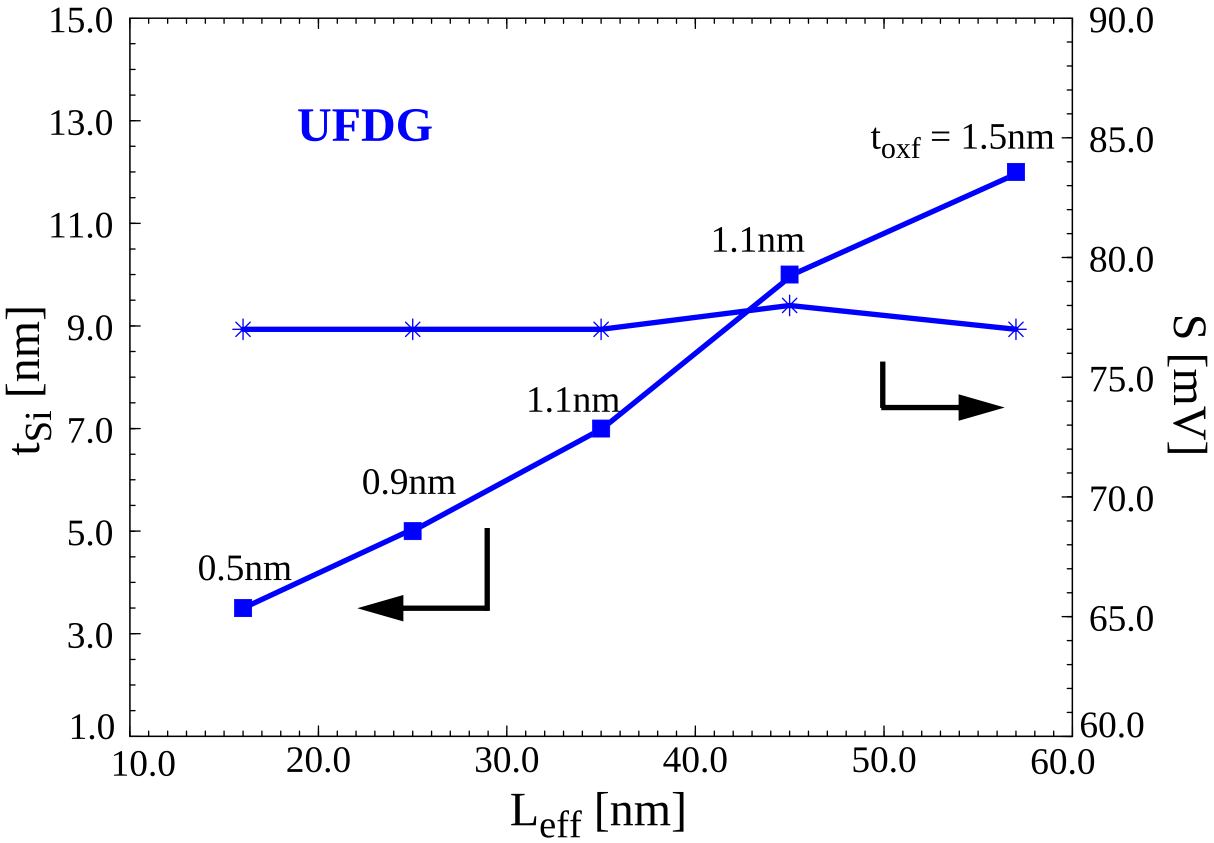
UFDG Application: Scaled FD/SOI MOSFET Design

Needed thin t_{Si} for DIBL < 100mV/V, high N_{CH} for V_t ~ 0.25V with poly gates:



- High SOI-channel doping density for V_t control is not viable!

Needed thin t_{Si} for DIBL < 100mV/V, with low N_{CH} and midgap gate:



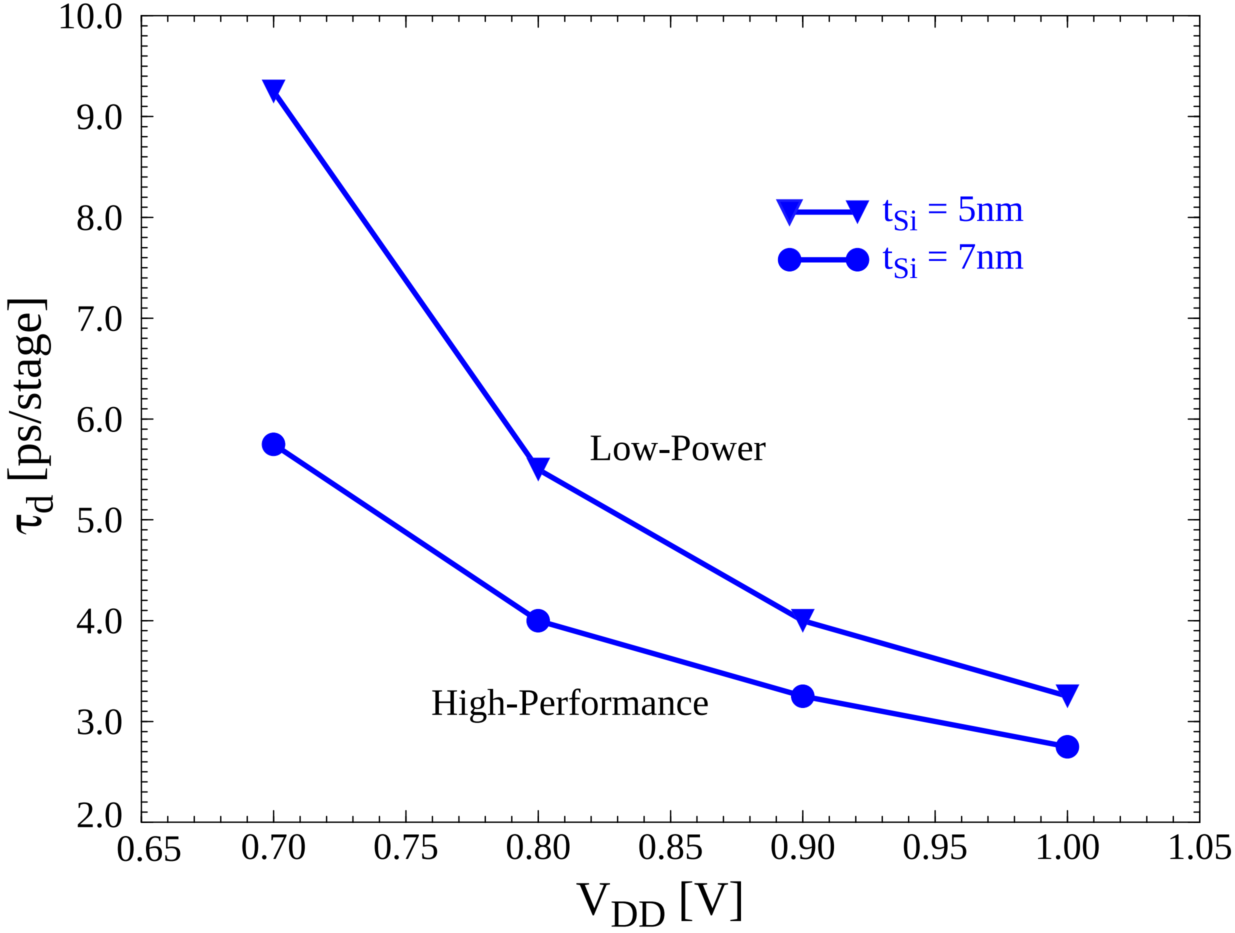
- Ultra-thin SOI is needed, but moderate Δt_{Si} can be tolerated.

UFDG/Spice3: Performance of L_{gate} = 28nm FD/SOI CMOS*

(9-stage Unloaded Ring-Oscillator Simulations)

Propagation Delay vs. Supply Voltage

(20% of L_{gate} overlaps S/D; $R_{S/D}$ assumed comparable to bulk-CMOS values)



*L_{eff} = 35nm, low N_{CH}, midgap gates. Note use of t_{Si} for V_t control.

Summary

- Process/physics-based UFDG is being developed as a generic compact model, applicable to FD/SOI as well as DG MOSFETs, including FinFETs.

- In essence, UFDG is a compact Poisson-Schrödinger solver, and can be useful for optimally designing thin Si-film DG and FD/SOI MOSFETs and the CMOS technologies (and circuits).

- UFDG: FD/SOI CMOS can be scaled to near the L_{gate} = 28nm generation with very good performance, but very thin SOI (t_{Si} < 10nm) and metal gate(s) will be needed.

- UFDG: DG CMOS, pragmatically designed with asymmetrical or symmetrical gates, is potentially scalable to the end the SIA ITRS (L_{gate} ~ 10nm) with extremely good performance, but the technology development, with very thin t_{Si} and possibly metal gates, will be challenging.