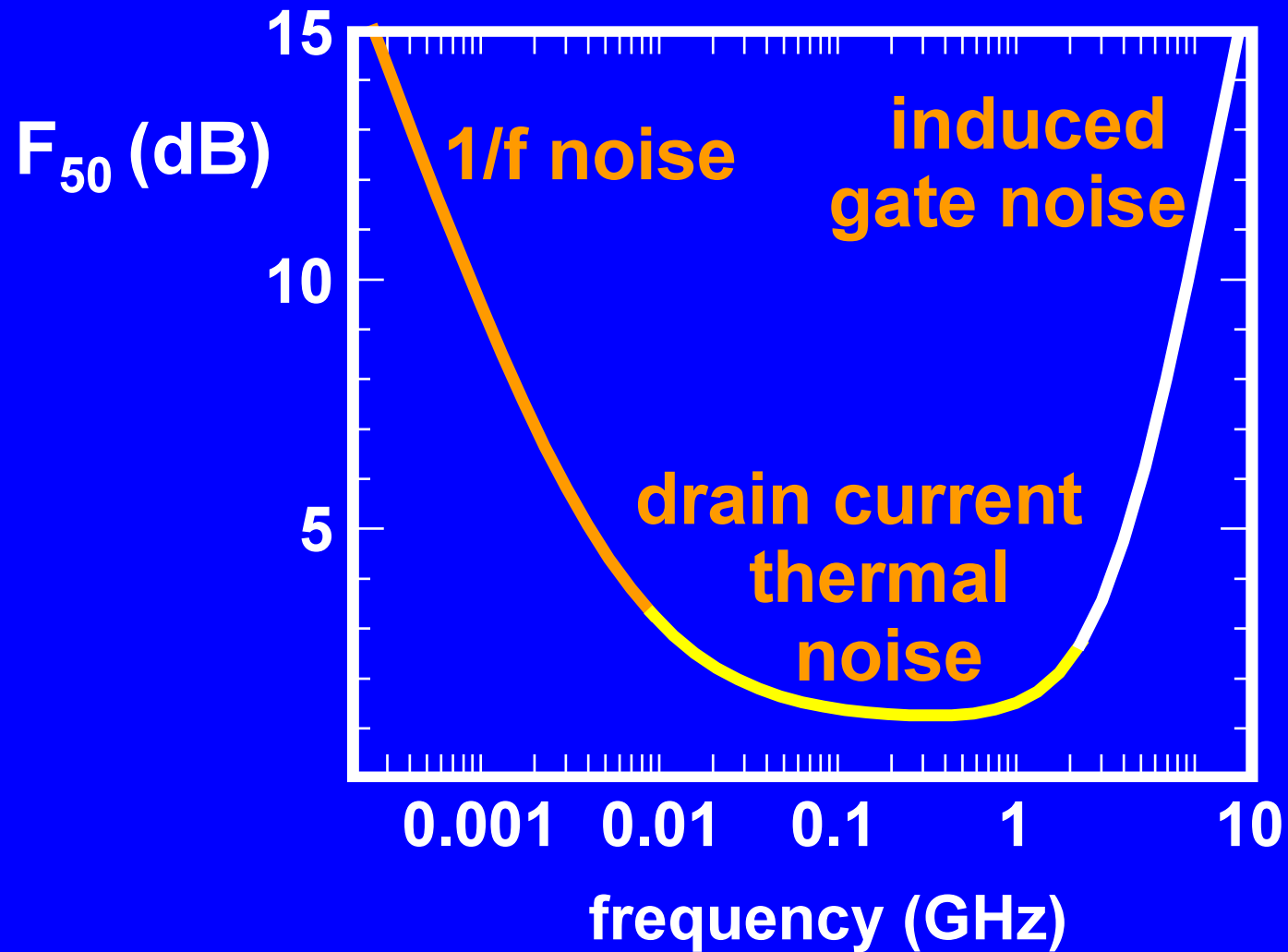


Noise modelling with MOS Model 11 for RF-CMOS applications

**A.J. Scholten, L.F. Tiemeijer, R. van Langevelde,
R.J. Havens, A.T.A. Zegers-van Duijnhoven,
V.C. Venezia[†] and D.B.M. Klaassen**

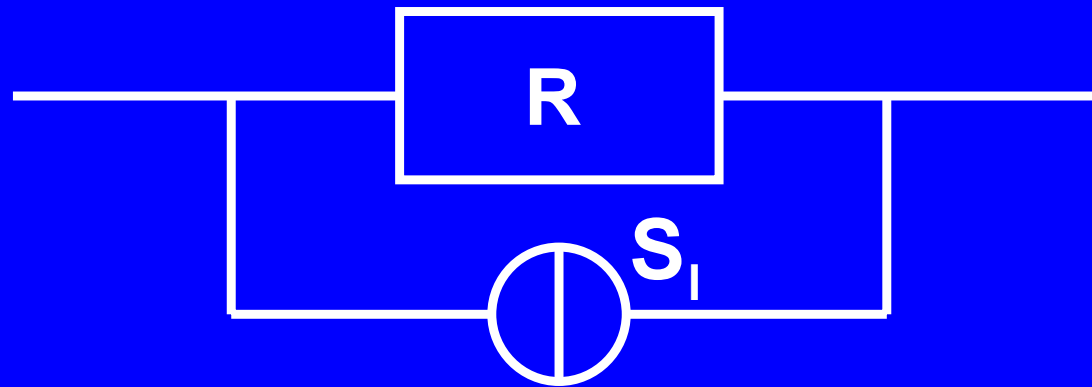
*Philips Research Eindhoven, The Netherlands
[†]Philips Research Leuven, Belgium*

MOSFET noise spectrum



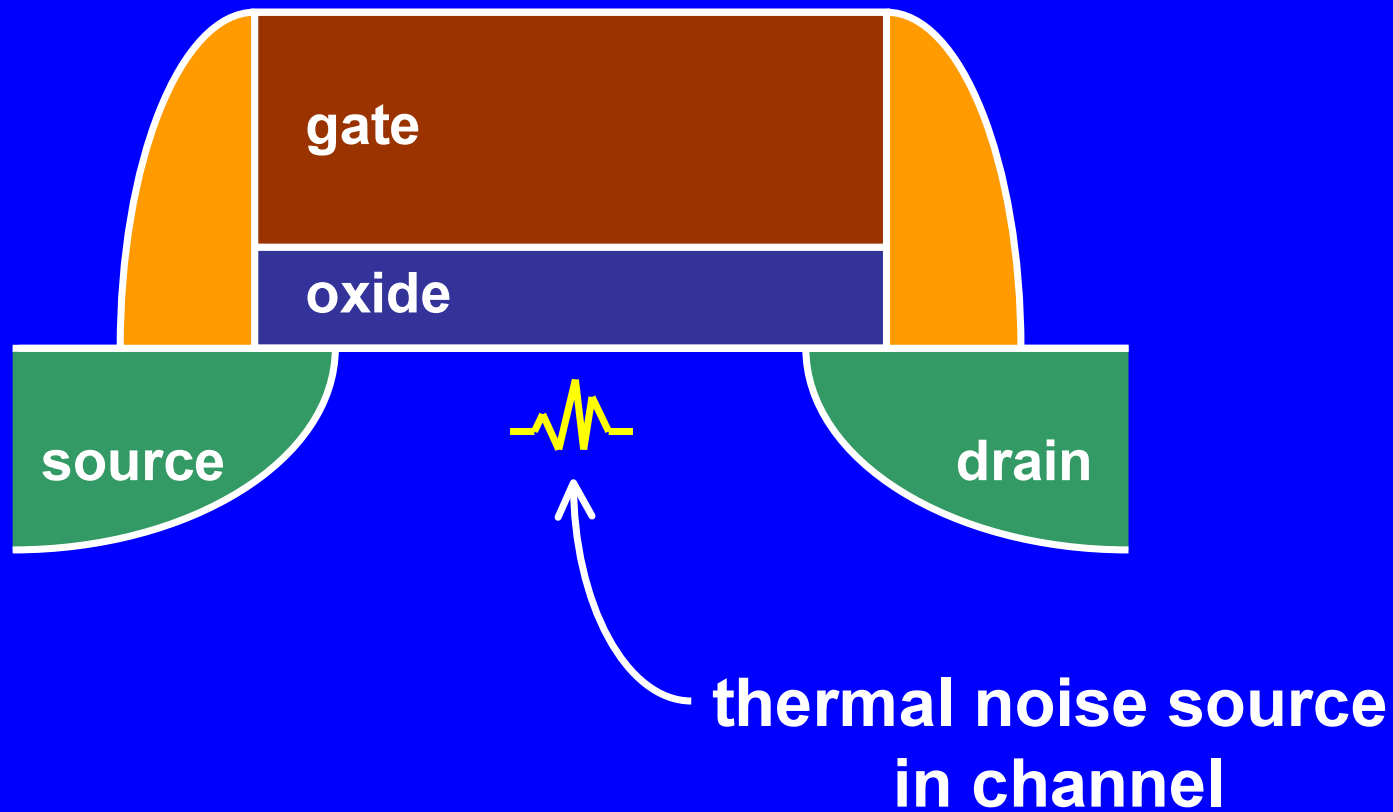
thermal noise

- random thermal motion of charge carriers
- frequency independent: “white”
- e.g. resistor:

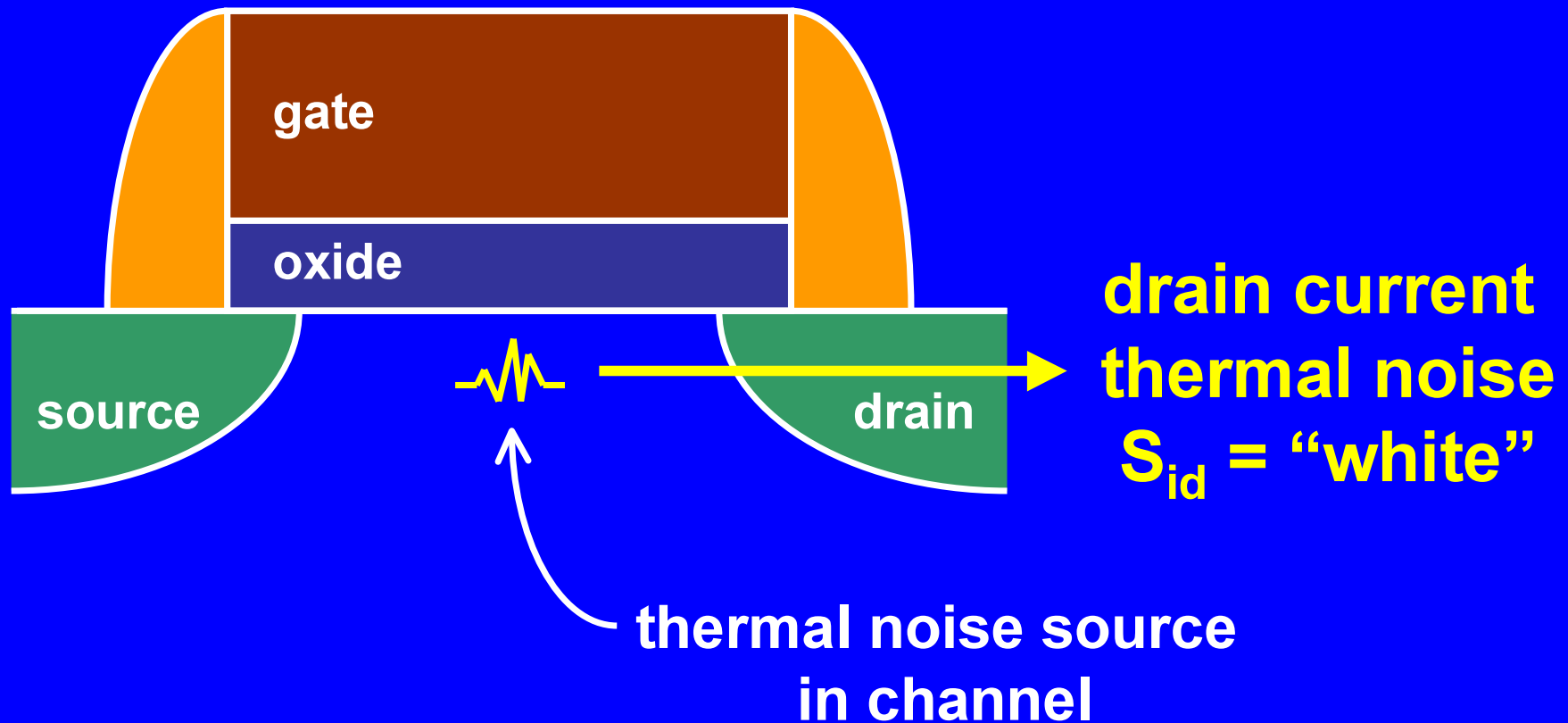


Nyquist's theorem:
$$S_i = \frac{4 \cdot k_B \cdot T}{R} \quad [\text{A}^2/\text{Hz}]$$

thermal noise in MOSFETs



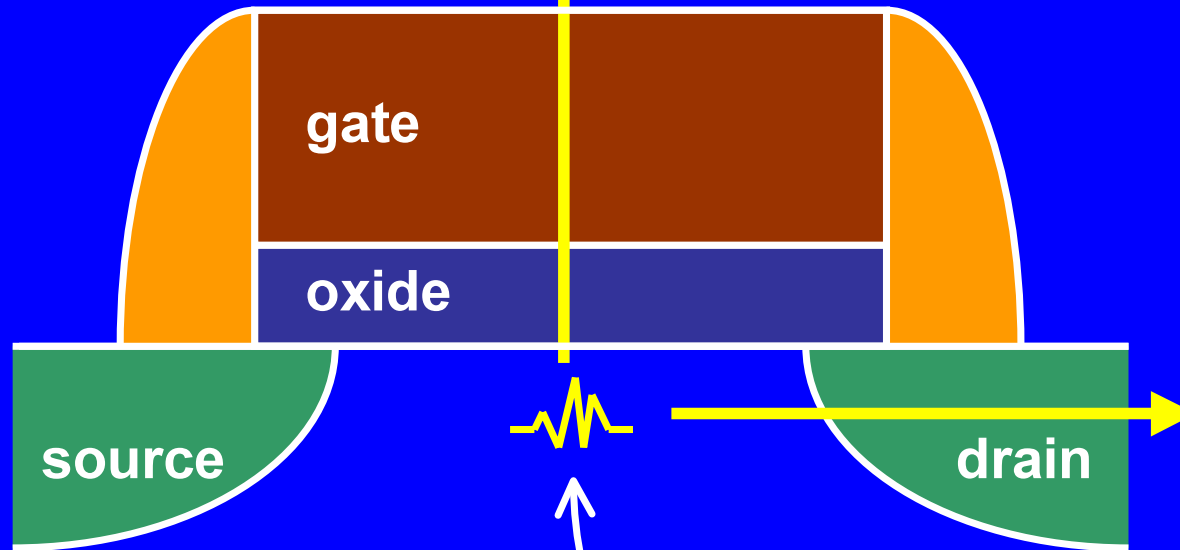
thermal noise in MOSFETs



thermal noise in MOSFETs

gate current thermal noise
“induced gate noise”

$$S_{ig} \propto f^2$$



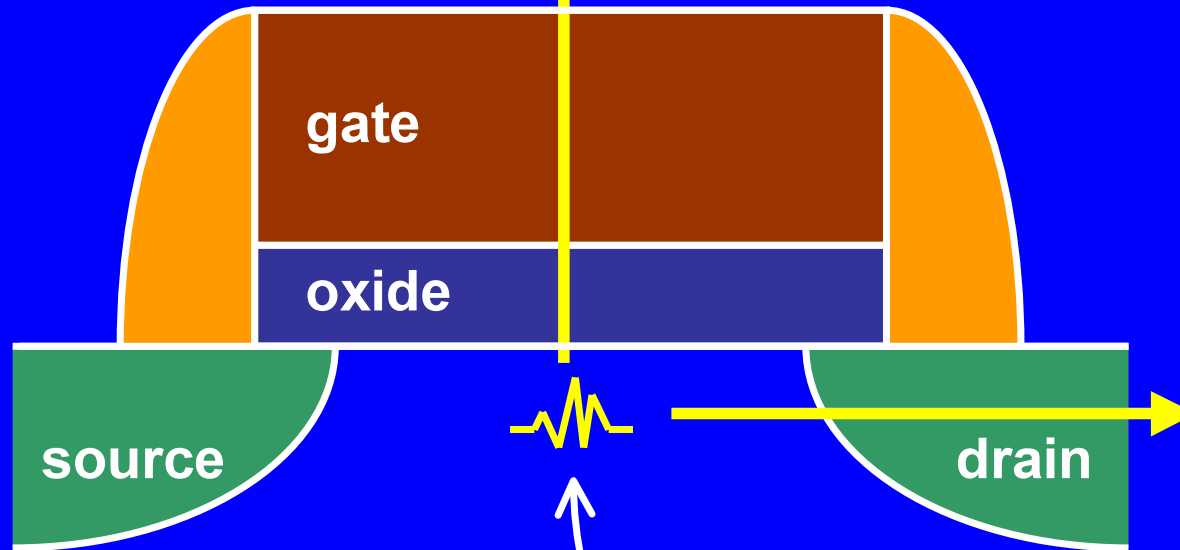
drain current
thermal noise
 $S_{id} = \text{"white"}$

thermal noise source
in channel

thermal noise in MOSFETs

gate current thermal noise
“induced gate noise”

$$S_{ig} \propto f^2$$

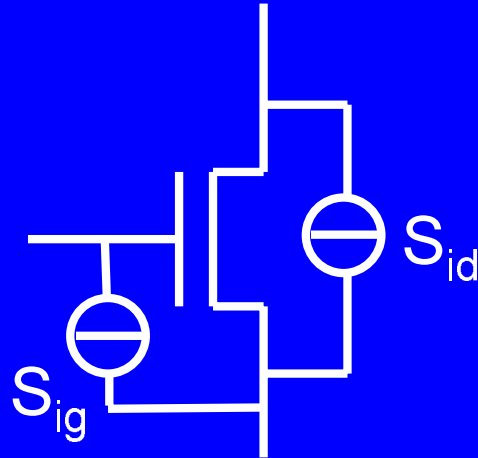


S_{id} and S_{ig}
correlated!

drain current
thermal noise
 S_{id} = “white”

thermal noise source
in channel

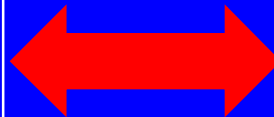
thermal noise in MOSFETs



S_{ig} and S_{id}
are correlated

Physics, Modelling

- S_{ig}
- S_{id}
- complex correlation coefficient, c



Circuits, Design

- equivalent noise resistance, R_n
- optimal source admittance, Y_{opt}
- minimum noise figure, F_{min}

$$F = F_{min} + \frac{R_n}{G_s} \cdot |Y_s - Y_{opt}|^2$$

**equivalent descriptions
both with 4 parameters**

motivation

⇒ enhancement S_{ID} up to factor 10:

- Abidi (1986)
- Klein (EDL 1999)
- Franca-Neto (ESSDERC 1999)
- ...

⇒ enhancement S_{IG} up to factor 30:

- G. Knoblinger, ESSDERC2001

motivation

⇒ enhancement S_{ID} up to factor 10:

- Abidi (1986)
- Klein (EDL 1999)
- Franca-Neto (ESSDERC 1999)
- ...

⇒ enhancement S_{IG} up to factor 30:

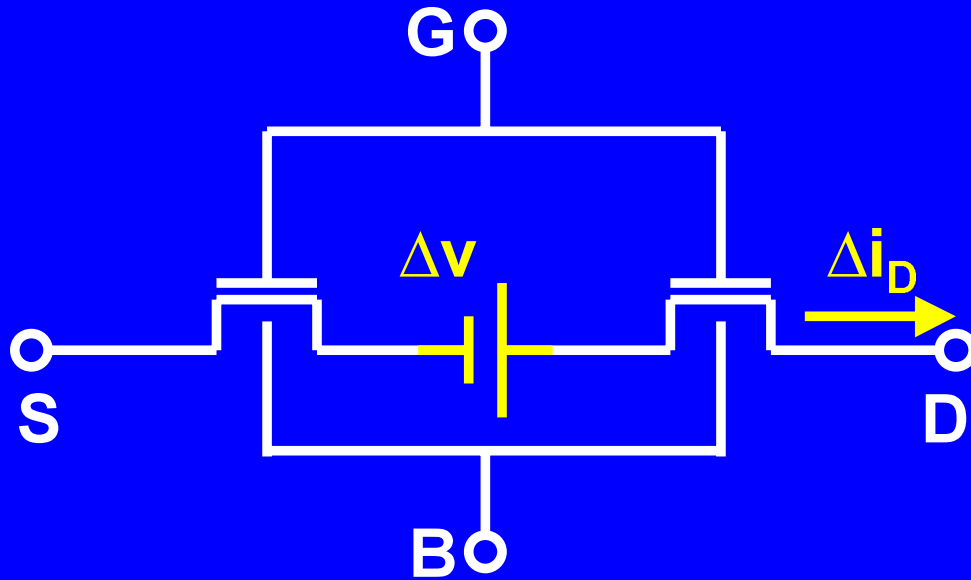
- G. Knoblinger, ESSDERC2001

calls for a detailed investigation

contents

- introduction
- **RF noise model**
- results thermal noise
- layout effects
- additional noise sources
- conclusion

drain current noise model (I)



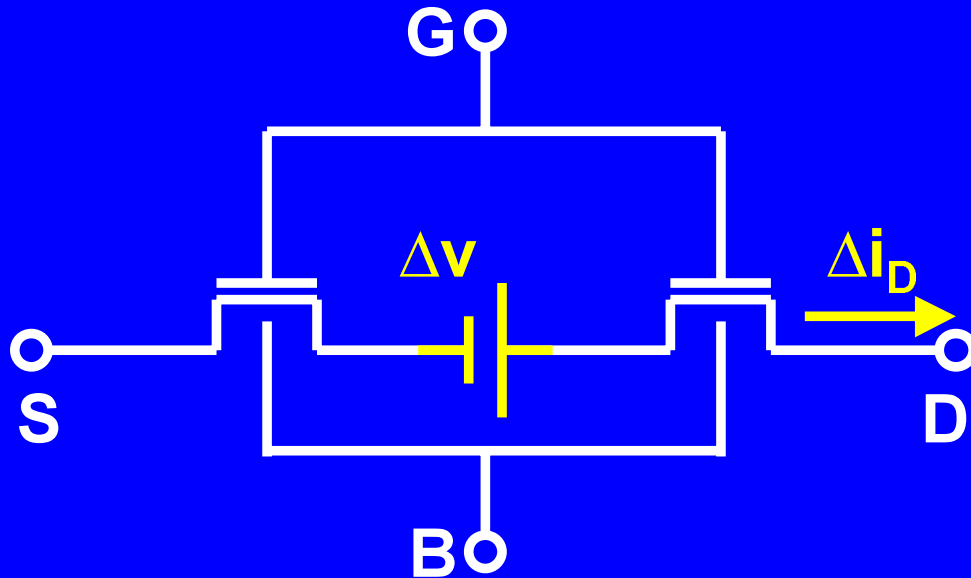
MOSFET equations:

$$I_D = g(x) \cdot \frac{dV}{dx}$$

$$g(x) = W \cdot \mu(x) \cdot Q_i(x)$$

$$\Rightarrow \Delta i_D = \frac{-g(x)}{L} \cdot \Delta v$$

drain current noise model (I)



MOSFET equations:

$$I_D = g(x) \cdot \frac{dV}{dx}$$

$$g(x) = W \cdot \mu(x) \cdot Q_i(x)$$

$$\Rightarrow \Delta i_D = \frac{-g(x)}{L} \cdot \Delta v$$

Nyquist's law: $S_{\Delta v} = \frac{4 \cdot k_B \cdot T}{g(x)}$

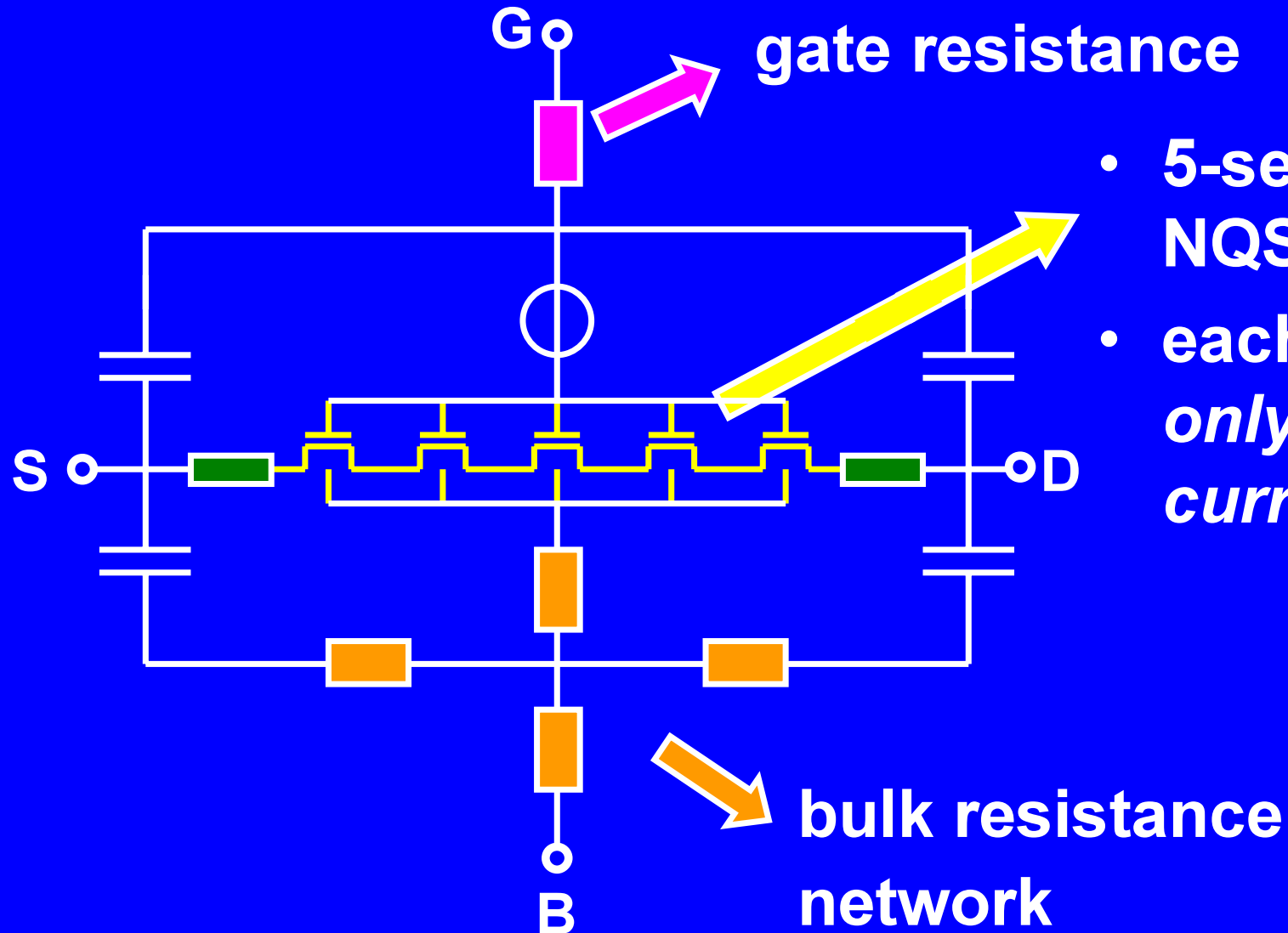
drain current noise model (II)

$$\Rightarrow S_{ID} = \frac{4 \cdot k_B \cdot T}{I_D \cdot L^2} \cdot \int_0^{V_{D(SAT)}} g^2(V) dV$$

Klaassen & Prins (1967)

- calculation based on MOS Model 11
(www.semiconductors.philips.com/Philips_Models)
- velocity saturation
- mobility reduction
- channel length modulation
- all parameters follow from DC and CV
- **no hot electron effects**
- **no additional parameters**

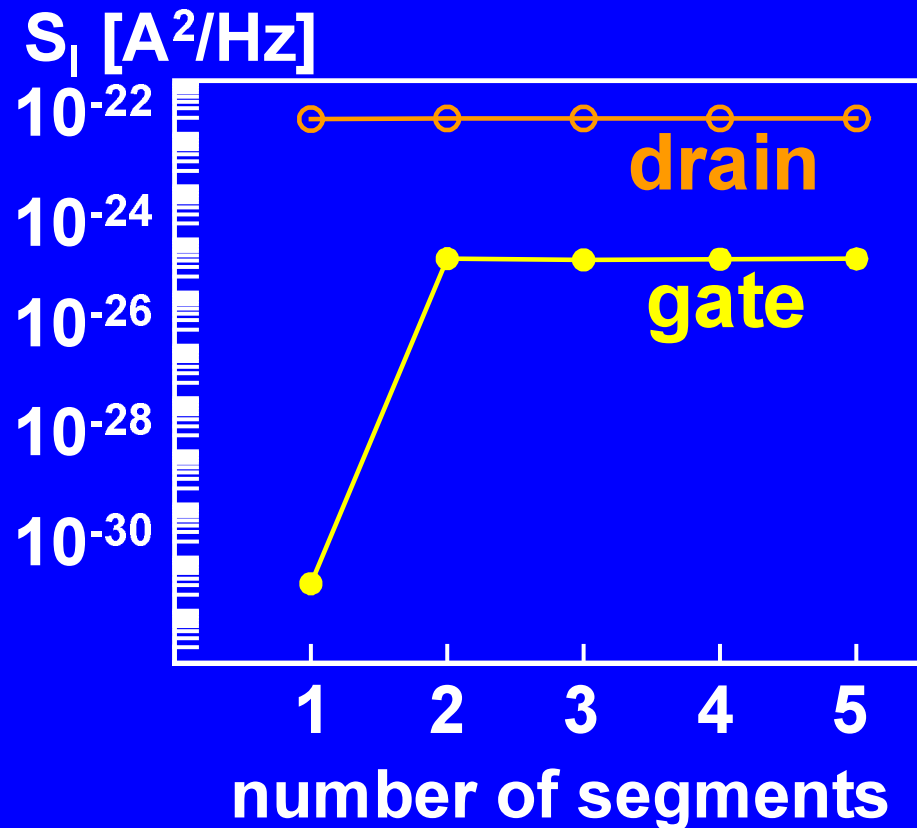
RF noise model (I)



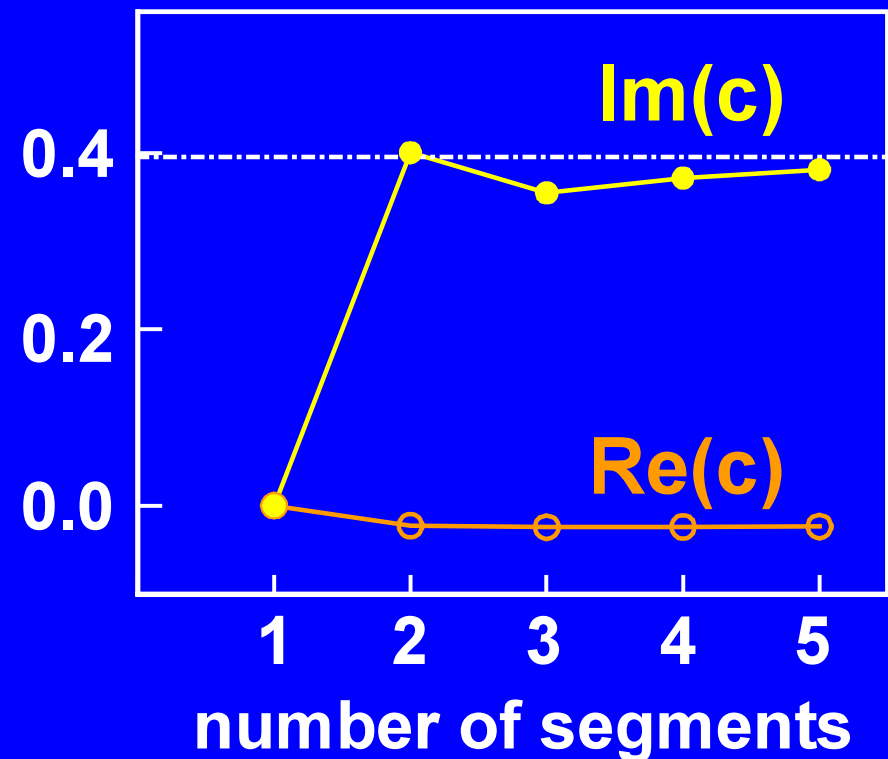
- 5-segment NQS model
- each segment: *only drain current noise*

RF noise model (II)

segmentation leads to induced gate noise



correlation coefficient



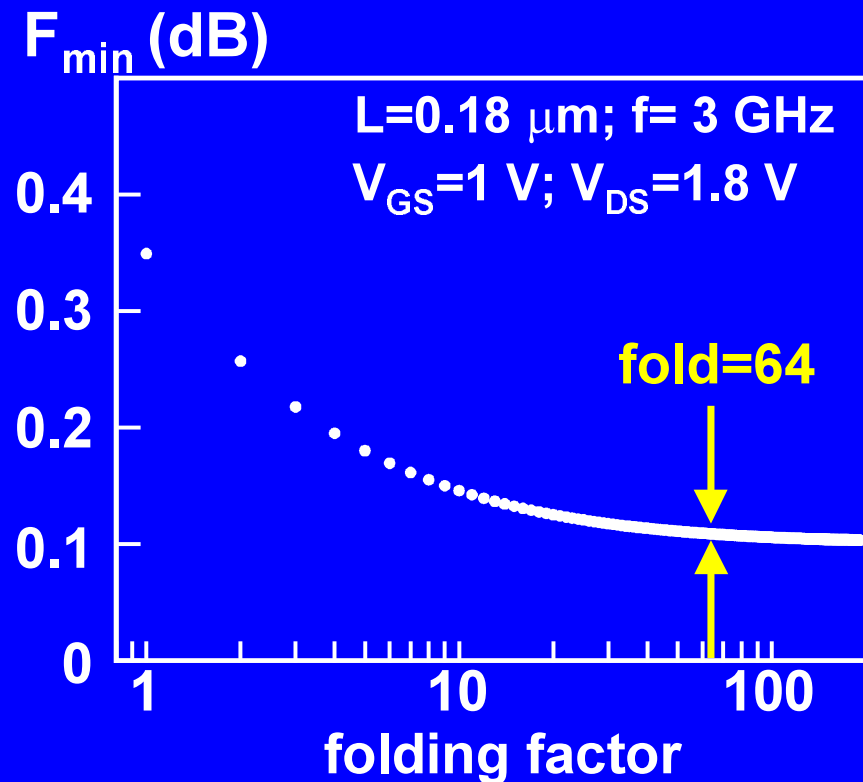
$L=2 \mu m$; $f=0.1 \text{ GHz}$
 $V_{GS}=1 \text{ V}$; $V_{DS}=1.8 \text{ V}$

contents

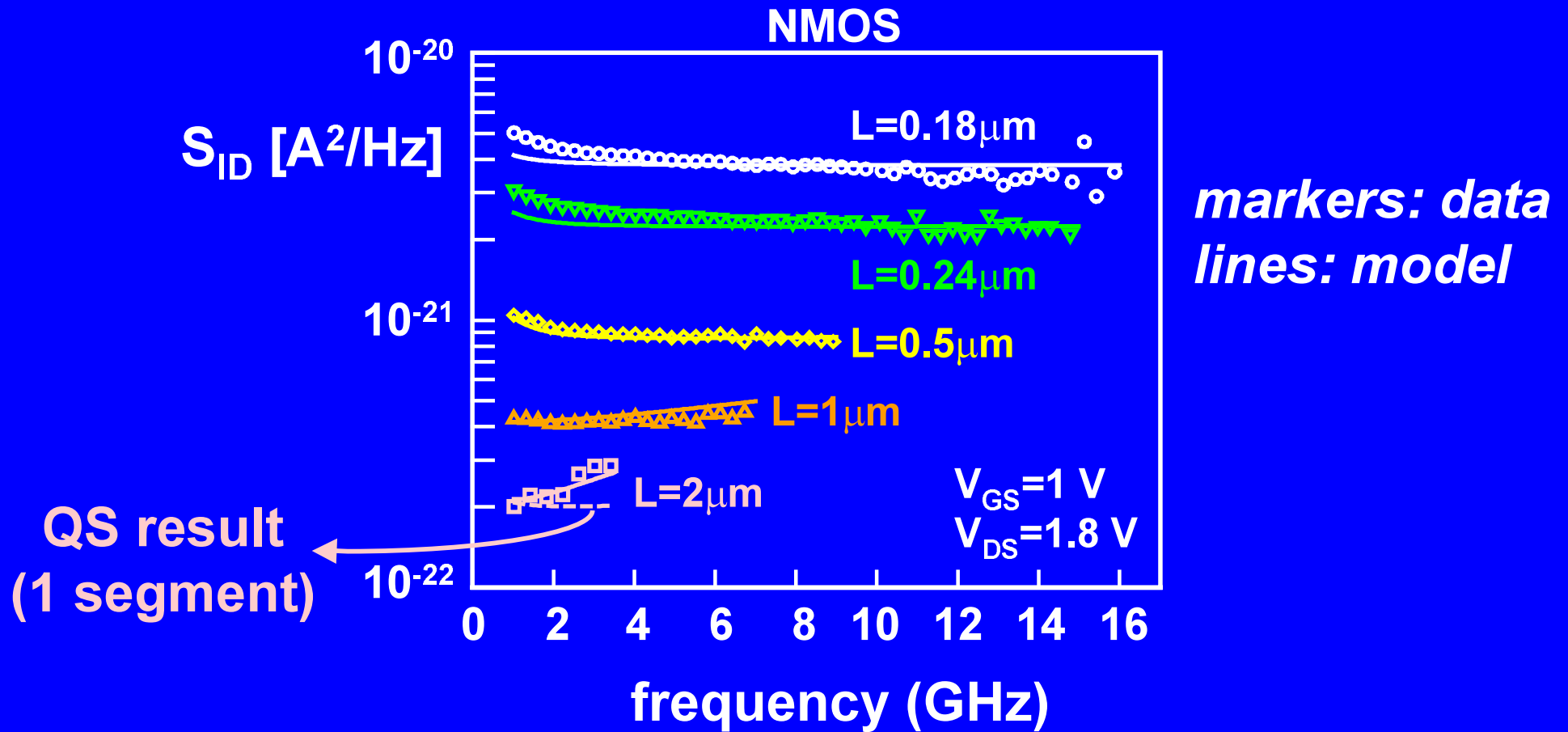
- introduction
- RF noise model
- **results thermal noise**
- layout effects
- additional noise sources
- conclusion

measurements

- noise figure meter + RF extension to 20 GHz
- new technique, using 3 fixed source impedances
- full de-embedding down to DUT level
- S_{id} , S_{ig} , $\text{Re}(c)$, $\text{Im}(c)$
- 0.18 μm technology
- optimized layout ($f_{\text{max}}=150$ GHz; see IEDM2001)

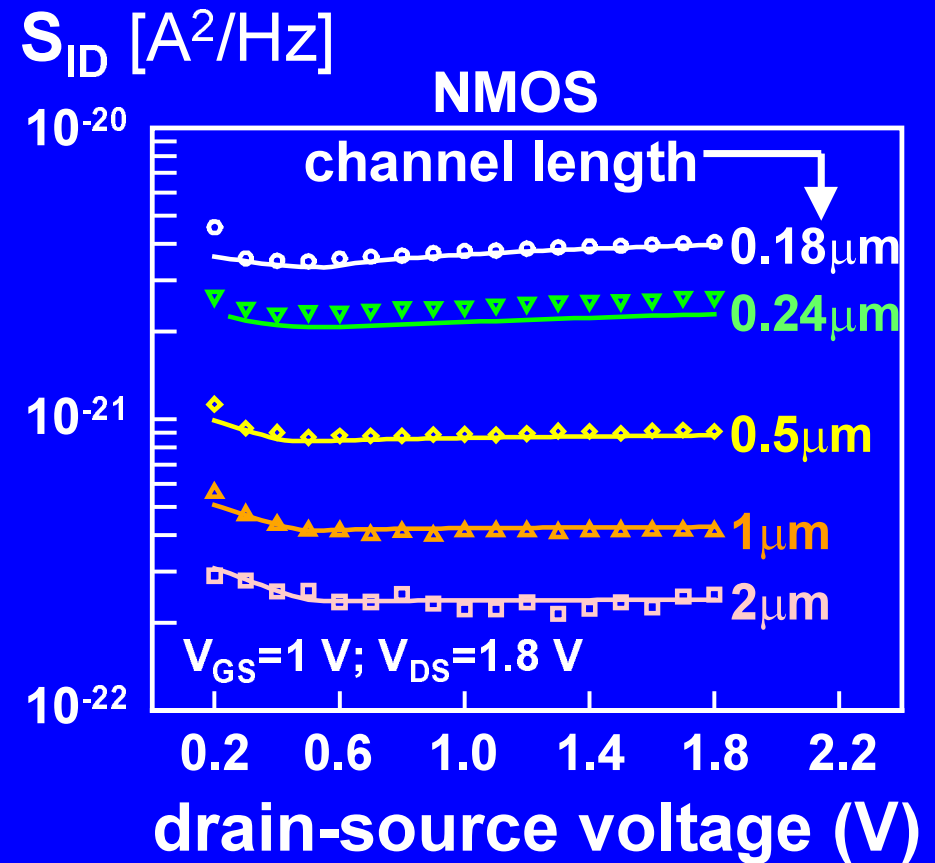
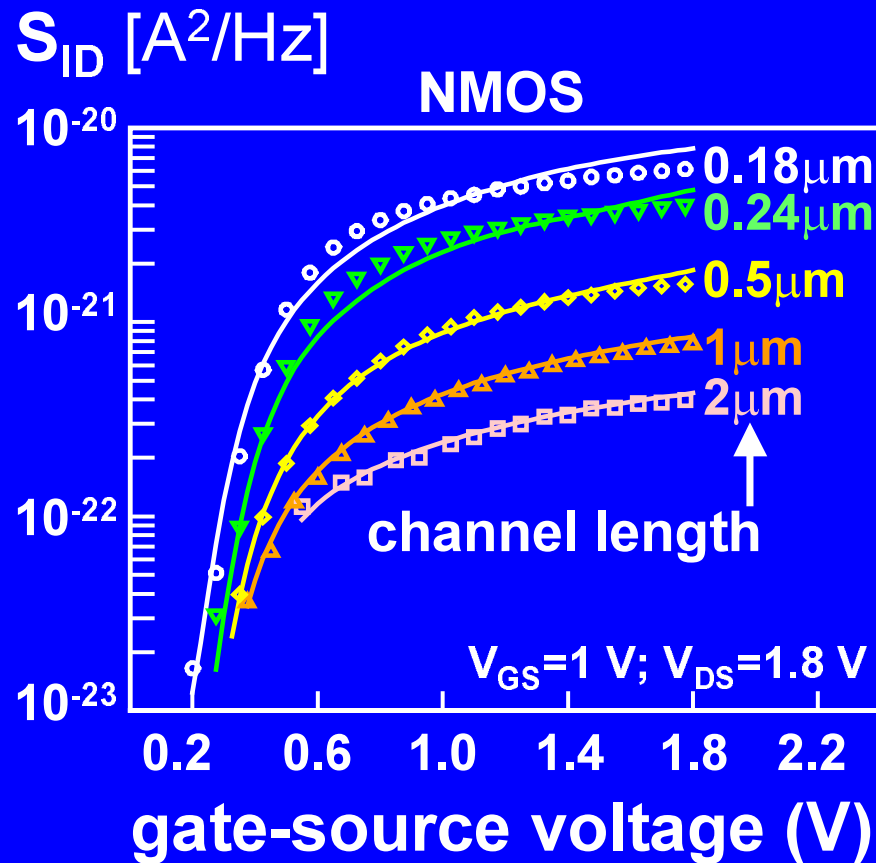


drain current noise (I)



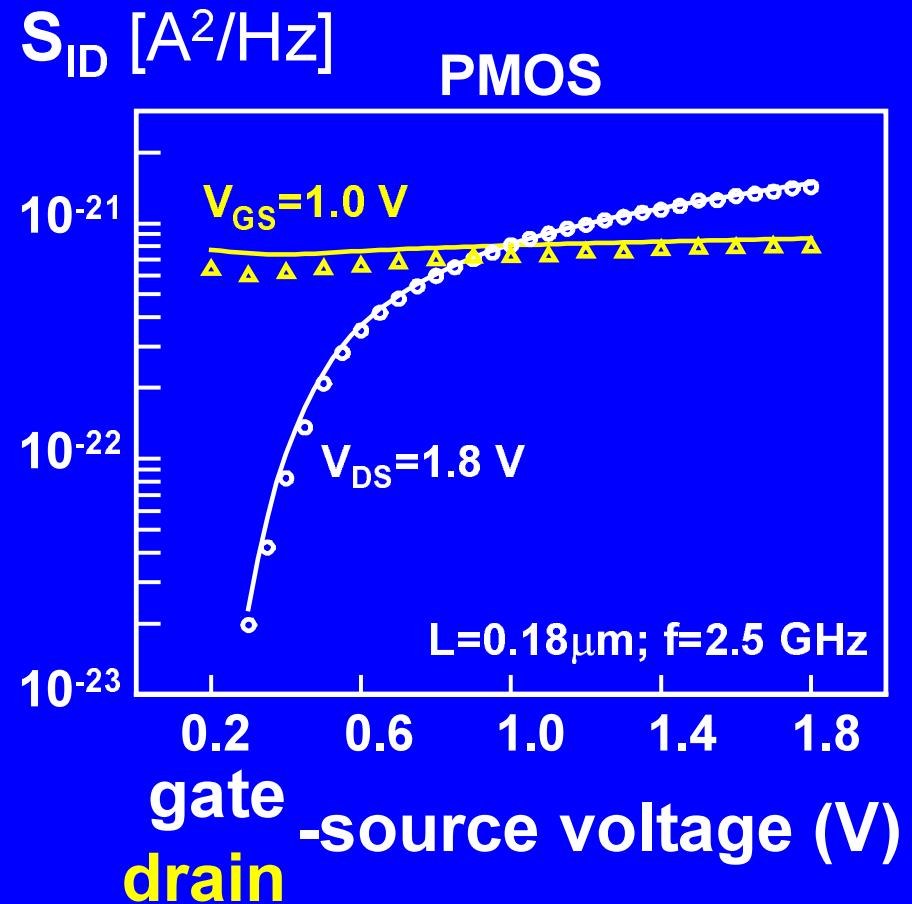
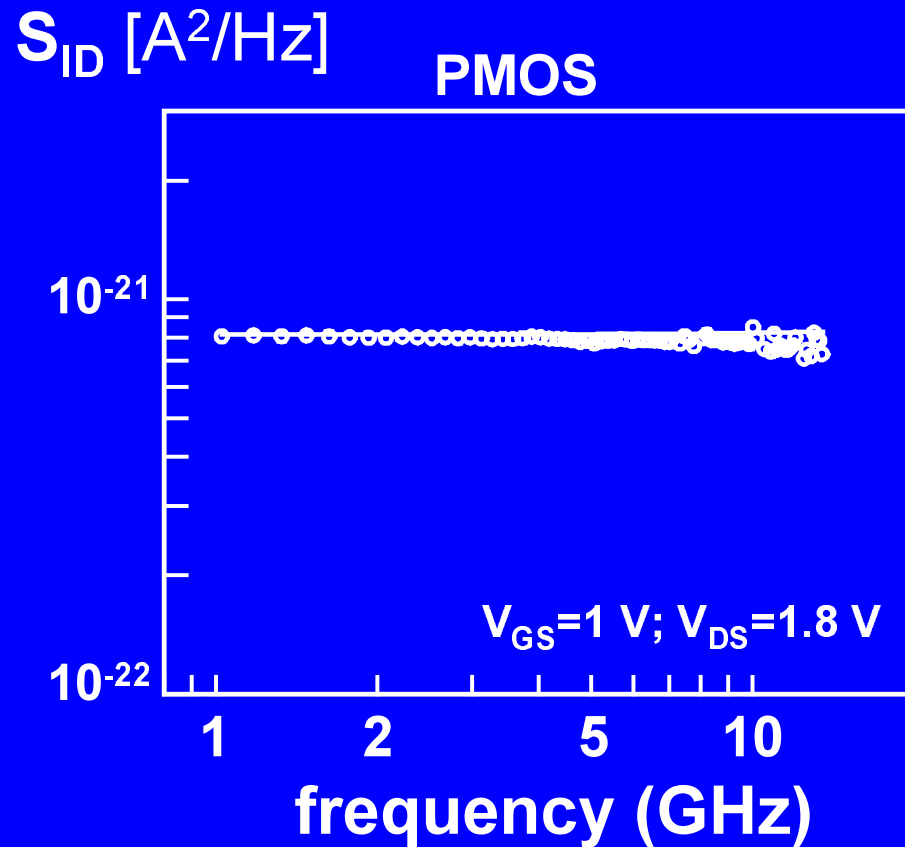
*excellent prediction thermal noise
without parameter fitting*

drain current noise (II)



bias dependence verified

drain current noise (III)



model verified for PMOS

drain current noise (IV)

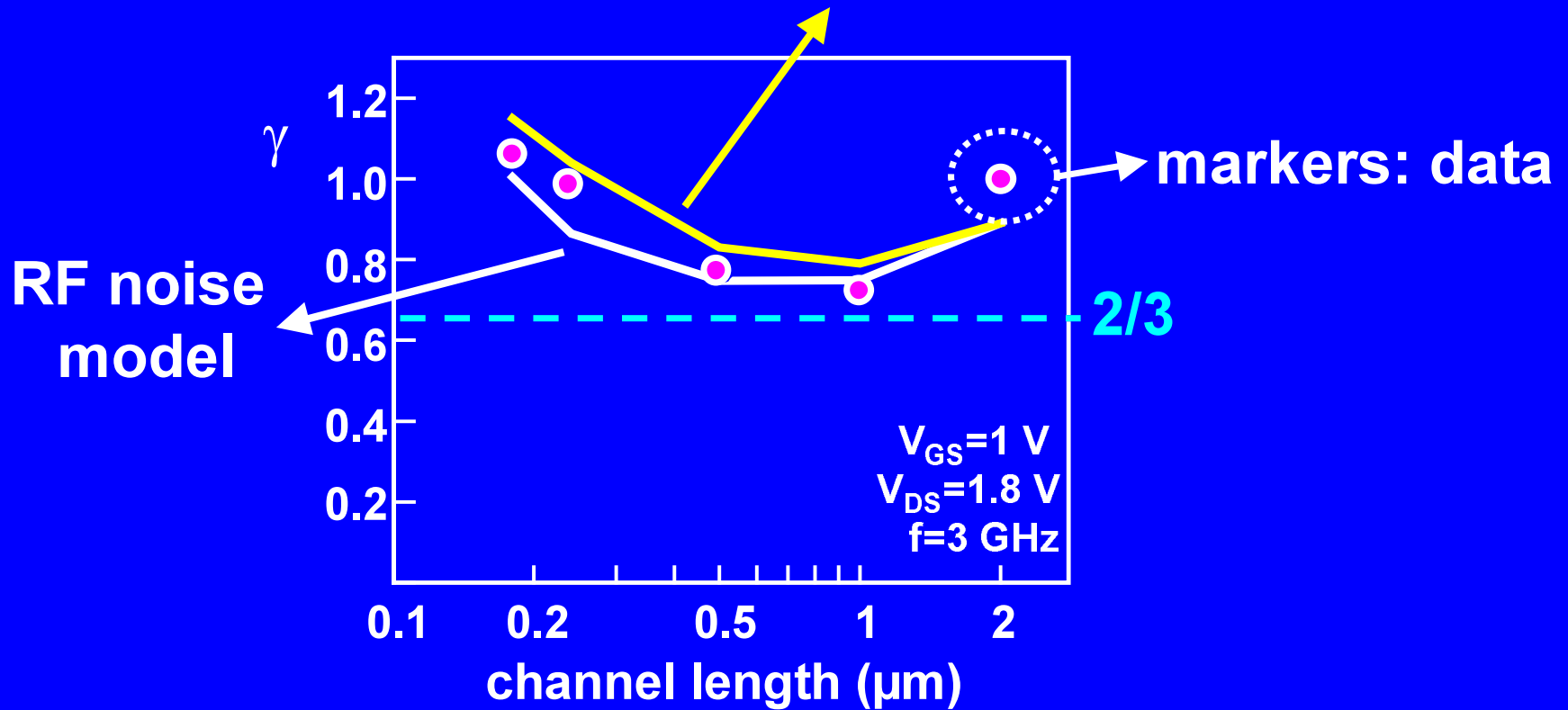
white noise gamma factor: γ

$$S_{id} \equiv 4 k_B T \cdot g_{do} \cdot \gamma$$

- γ quantifies amount of drain current noise
- $g_{do} = g_{ds}$ at zero V_{ds}
- long-channel:
 - $\gamma = 1$ (linear regime)
 - $\gamma = 2/3$ (saturation)

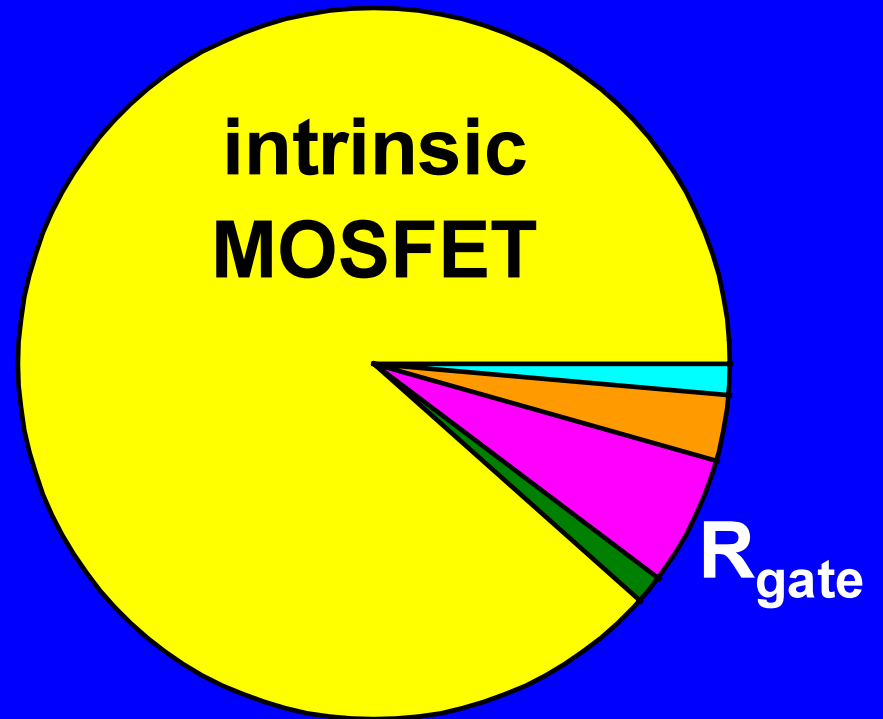
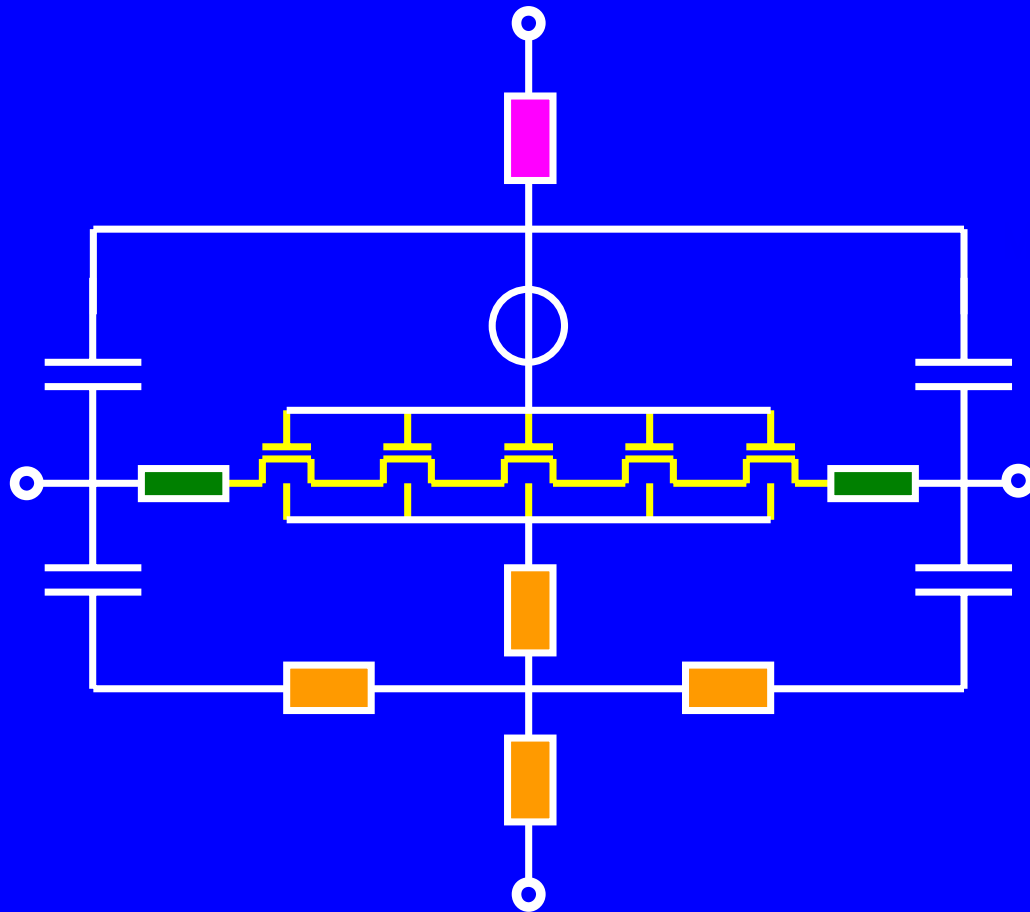
drain current noise (V)

DD-MC simulation
(Jungemann, IEDM 2001)



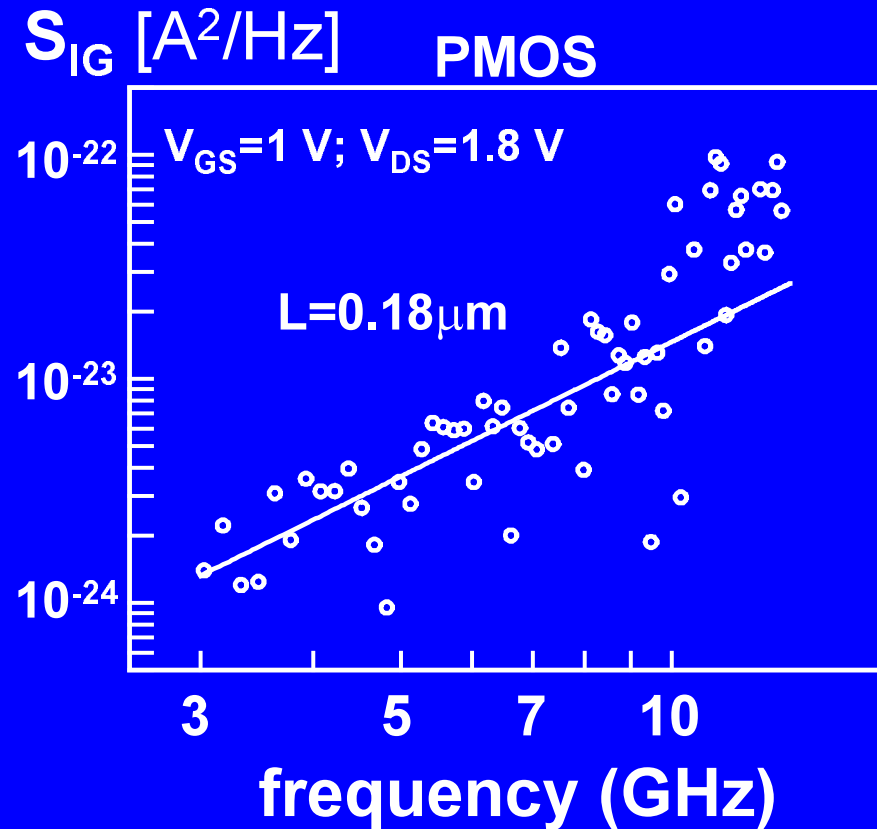
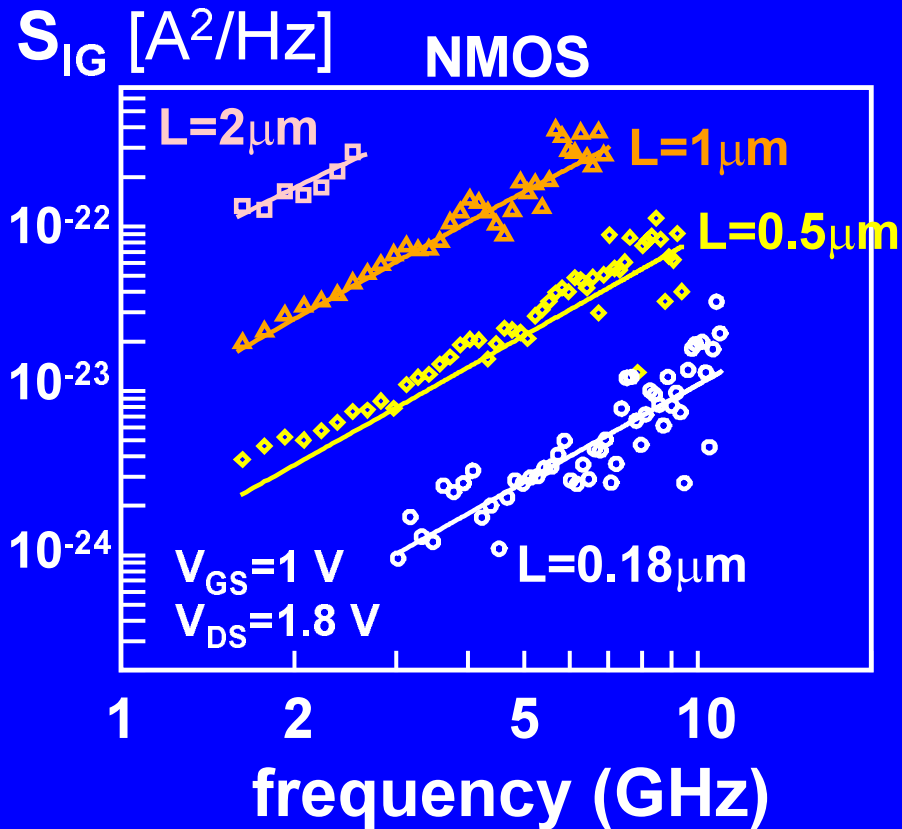
moderate increase of γ in 0.18 μm CMOS

drain current noise (VI)



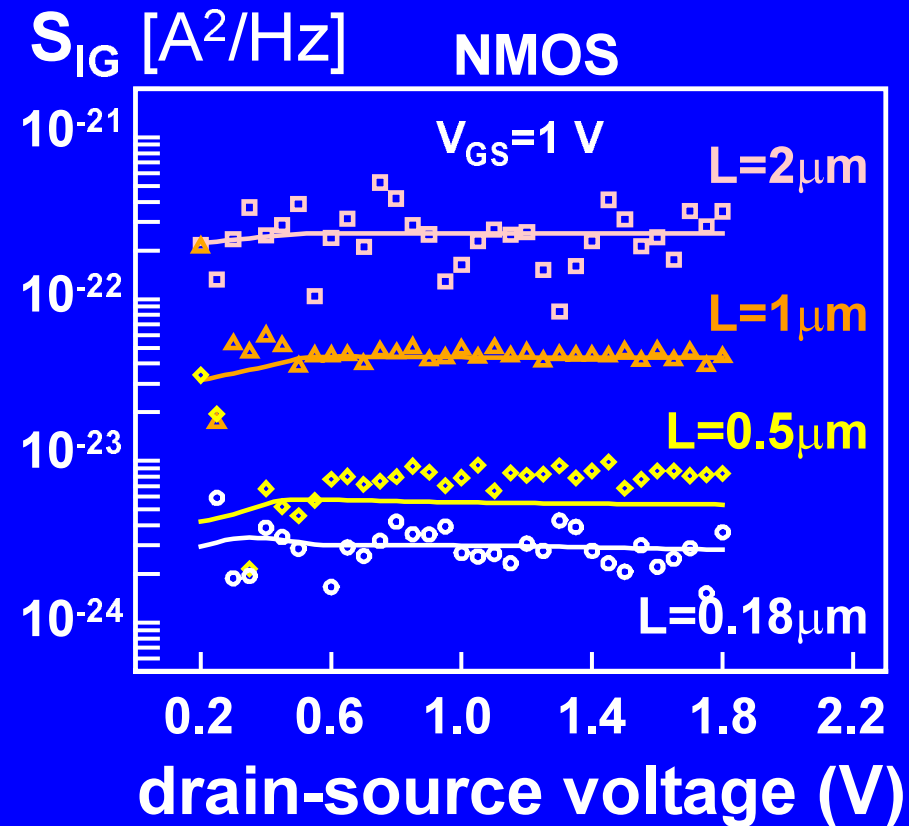
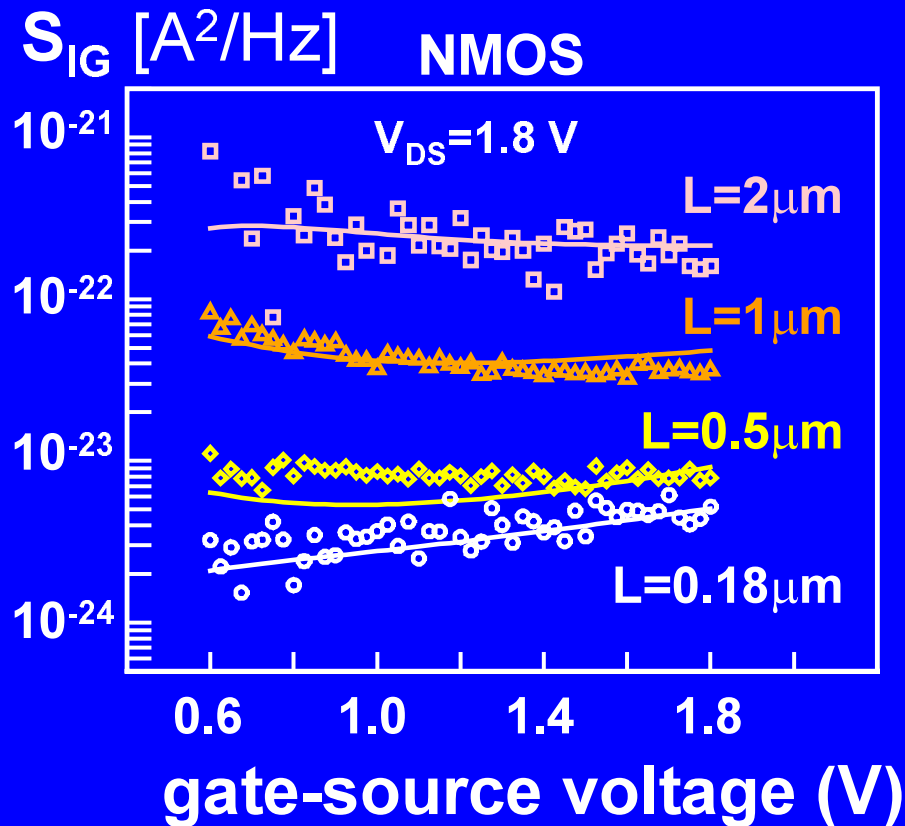
*major noise contribution 0.18 μm NMOS, $f=3$ GHz:
intrinsic MOSFET thermal noise*

gate current noise (I)



*excellent prediction induced gate noise
without parameter fitting*

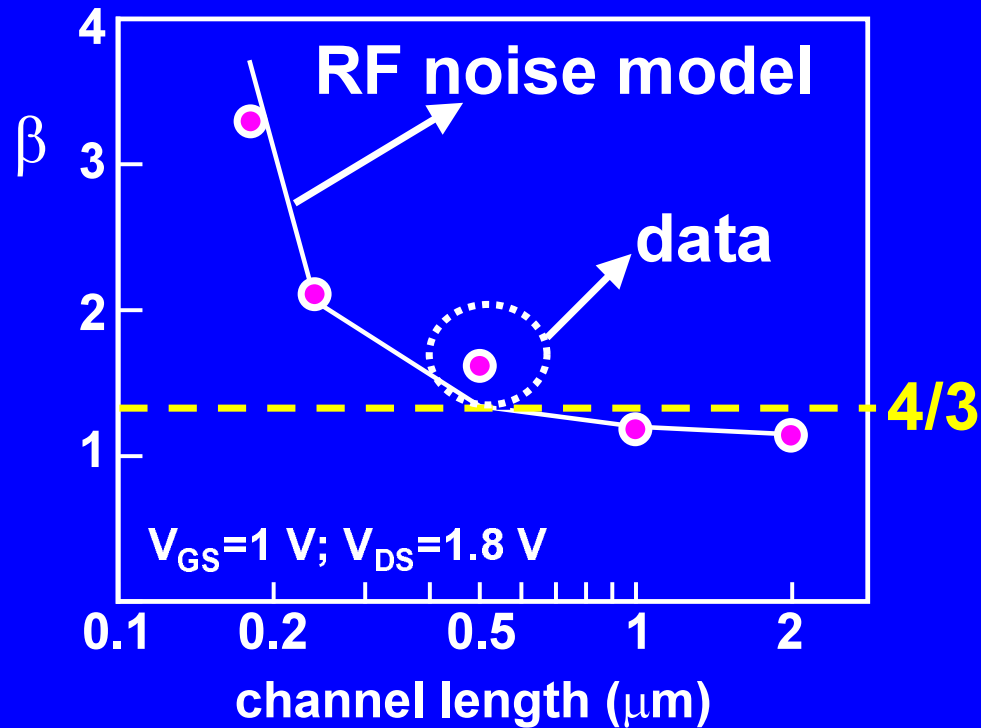
gate current noise (II)



bias dependence verified

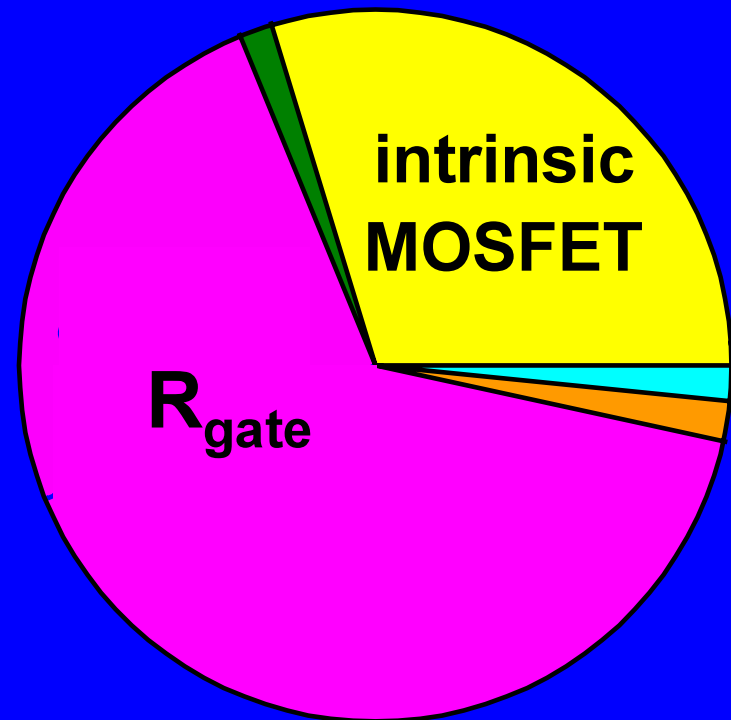
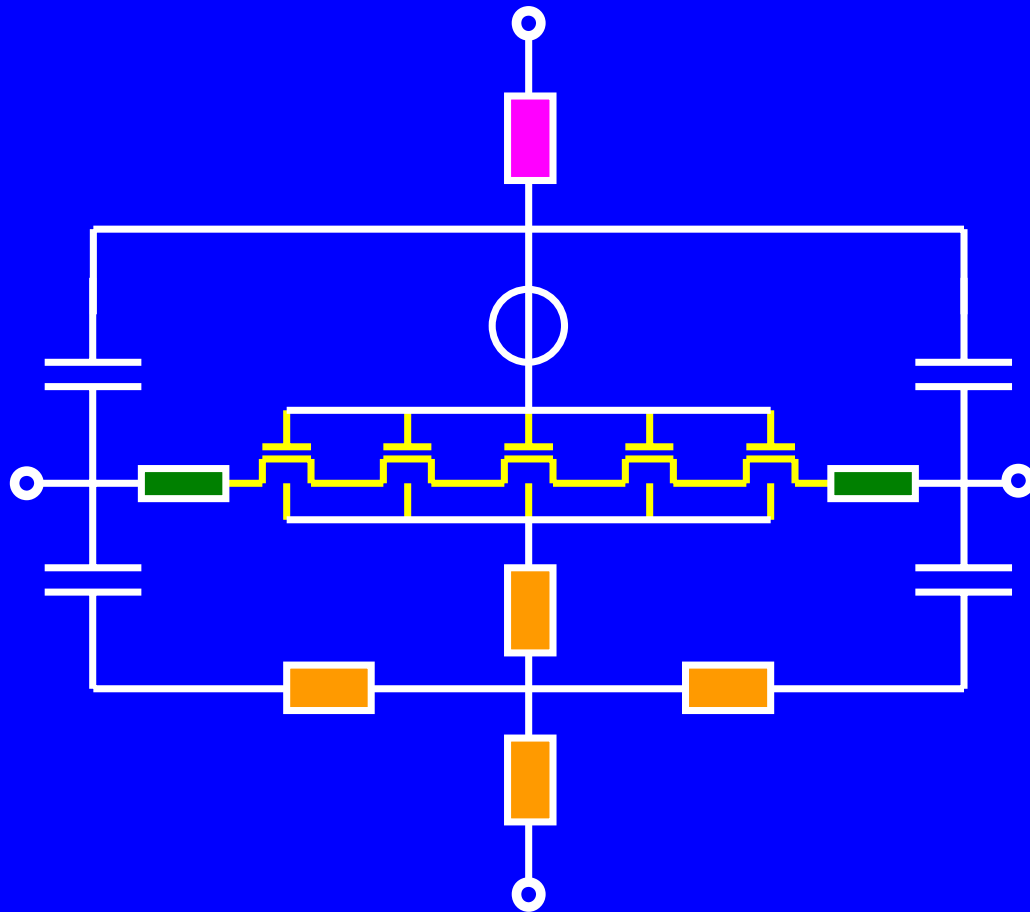
gate current noise (II)

$$S_{ig} \equiv \beta \cdot \frac{4 k_B T \cdot (\omega C_{GS})^2}{5 g_{do}}$$



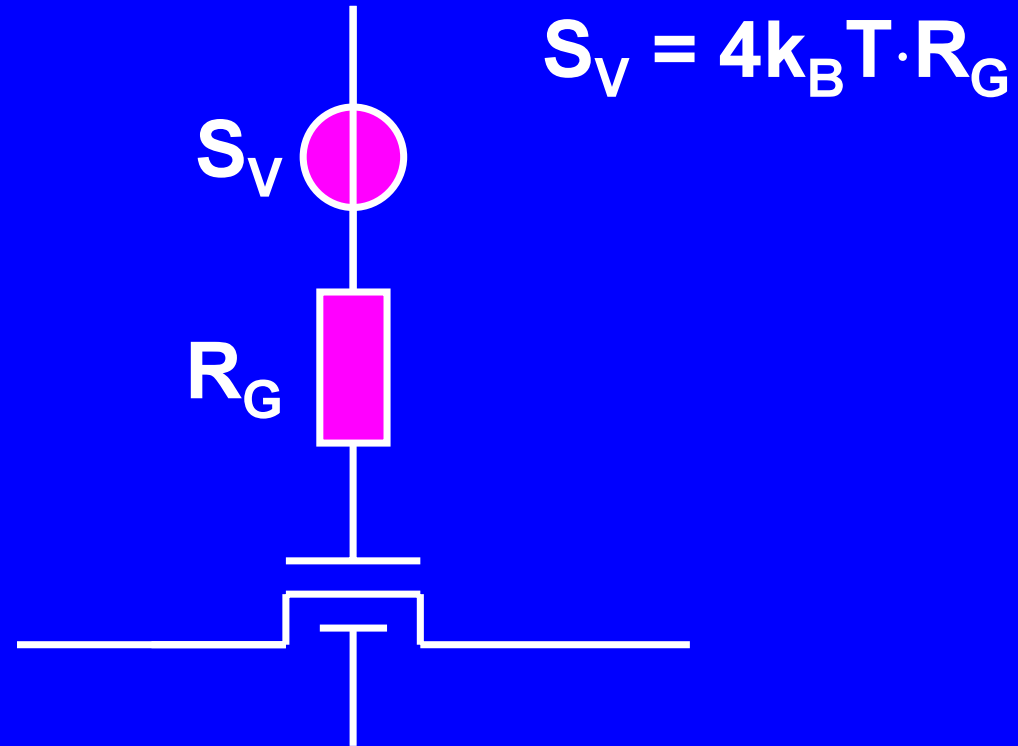
- β quantifies the amount of gate current noise
- long channel: $\beta = 4/3$ (saturation)
- **short channels:**
strong increase of β

gate current noise (IV)

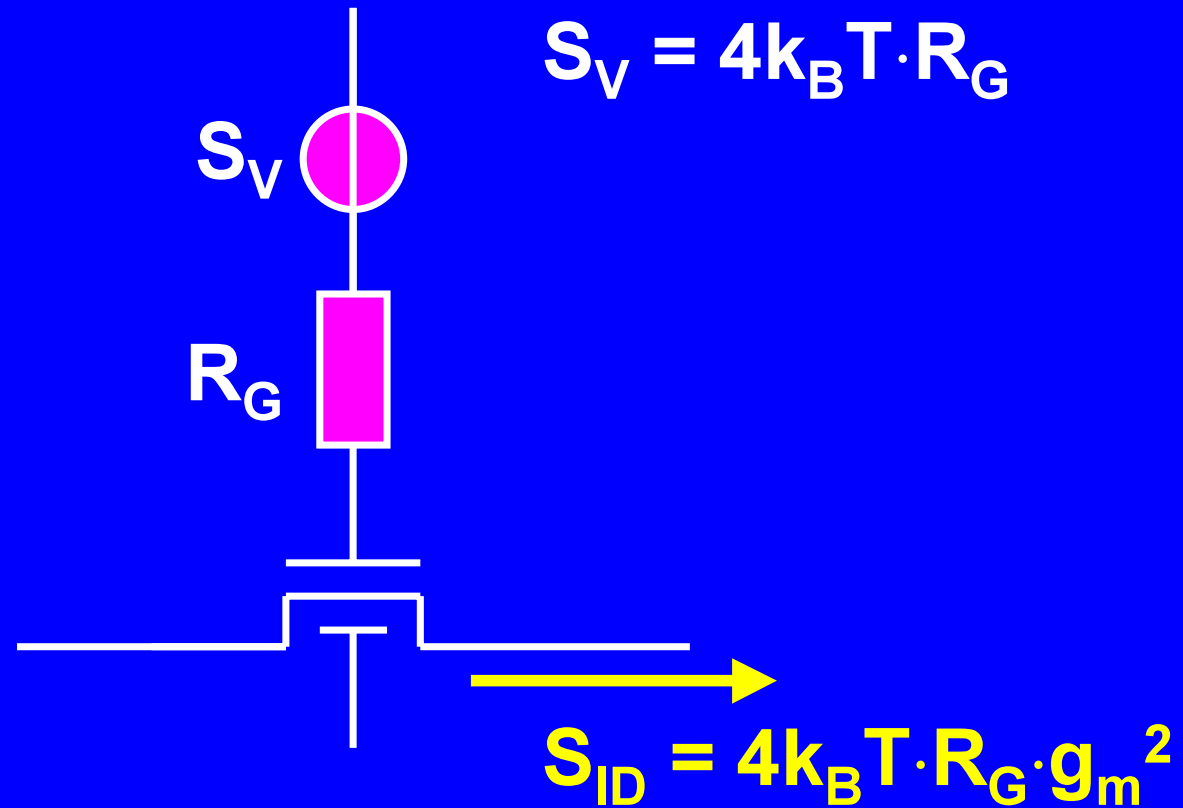


*major noise contribution 0.18 μm NMOS, $f=3$ GHz:
gate resistance*

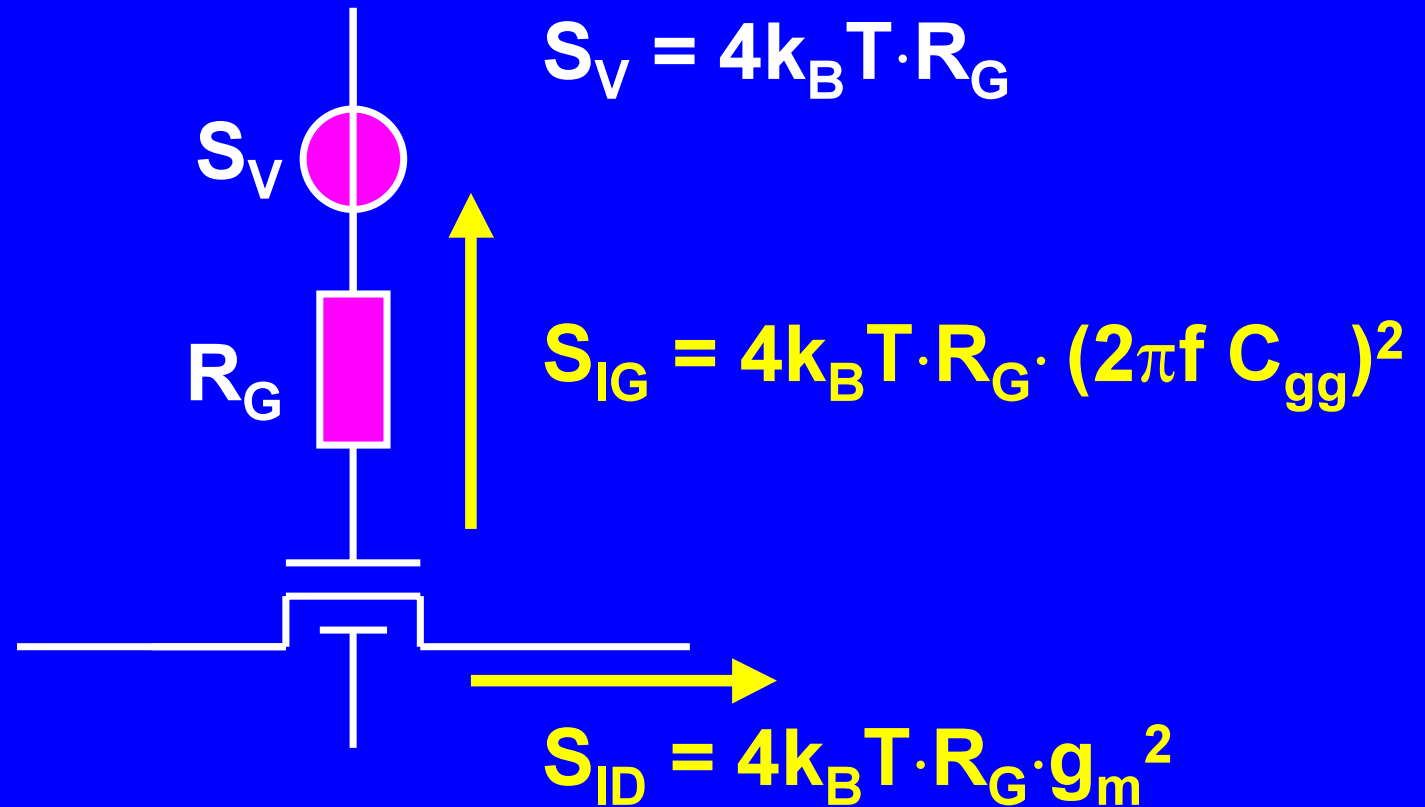
gate current noise (V)



gate current noise (V)

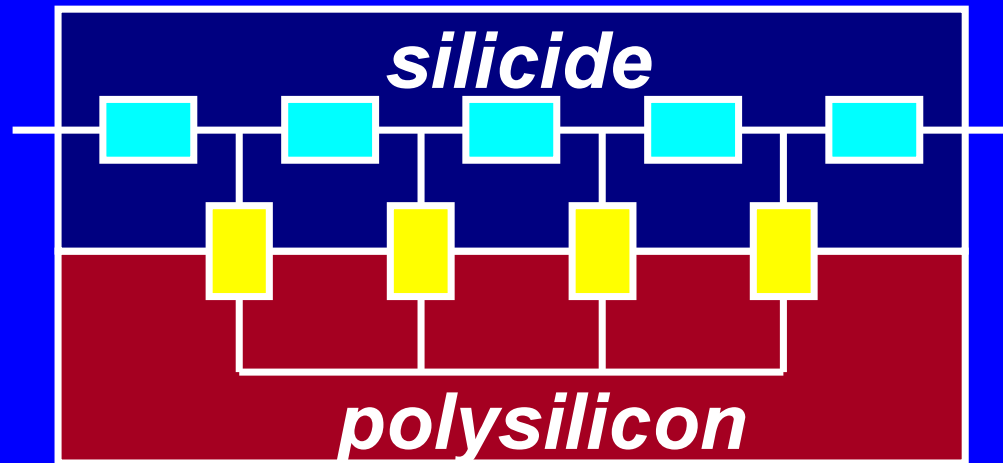


gate current noise (V)

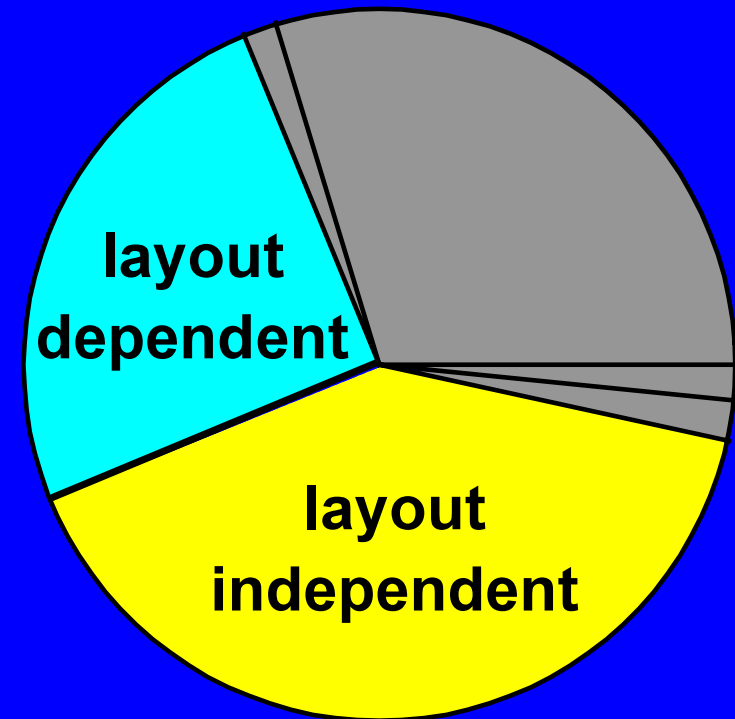


**gate resistance leads to noise $\propto f^2$ in gate current
(resembles induced gate noise)**

gate current noise (VI)



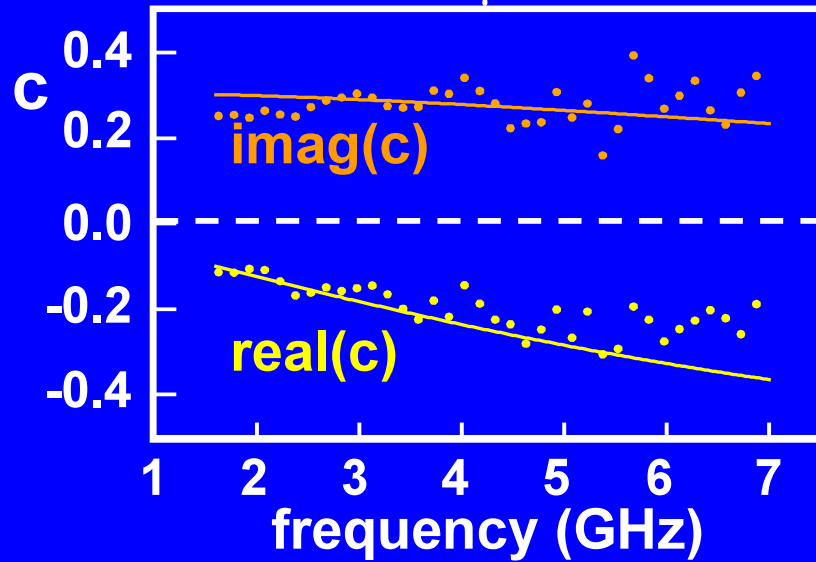
***optimized layout:
gate resistance dominated
by
silicide-to-polysilicon
contact resistance***



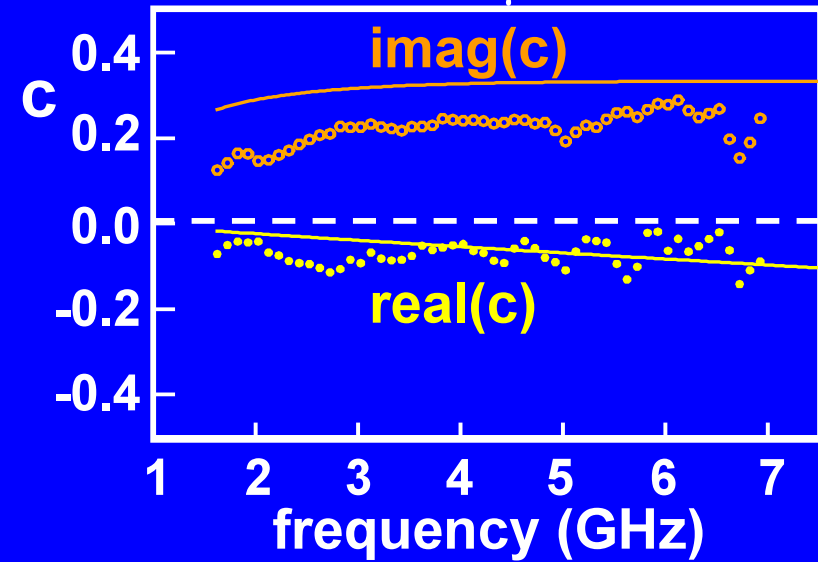
(Litwin, T-ED 48, p.2179)

correlation coefficient

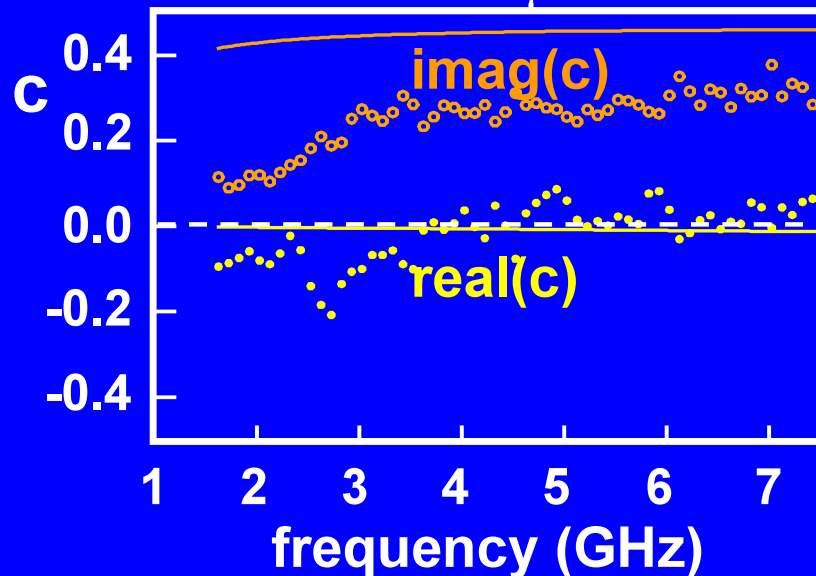
$L=1\mu\text{m}$



$L=0.5\mu\text{m}$

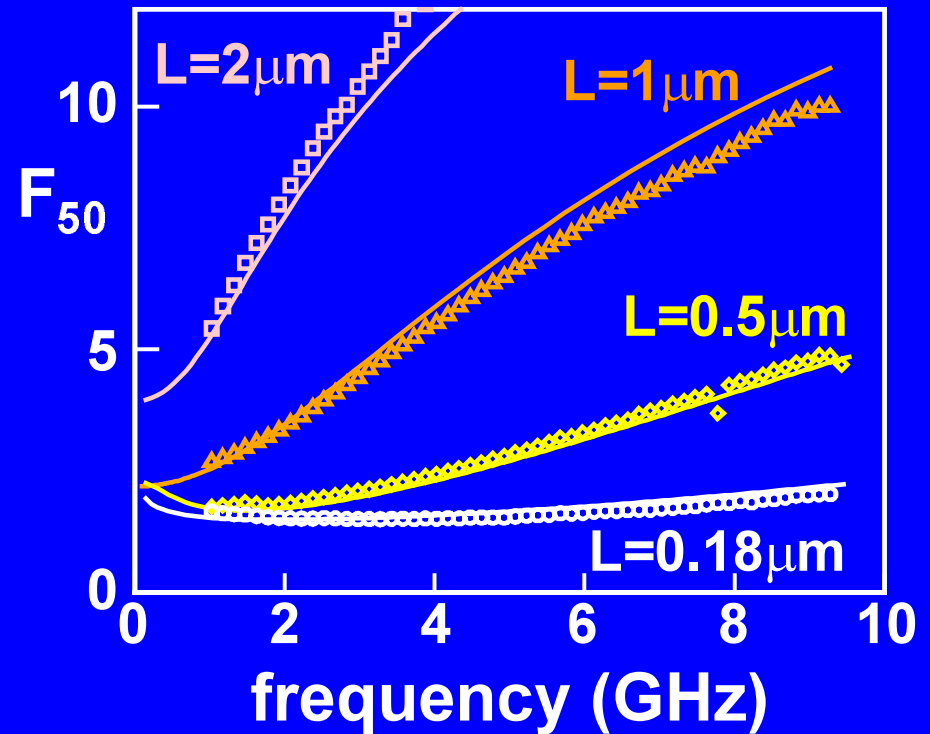
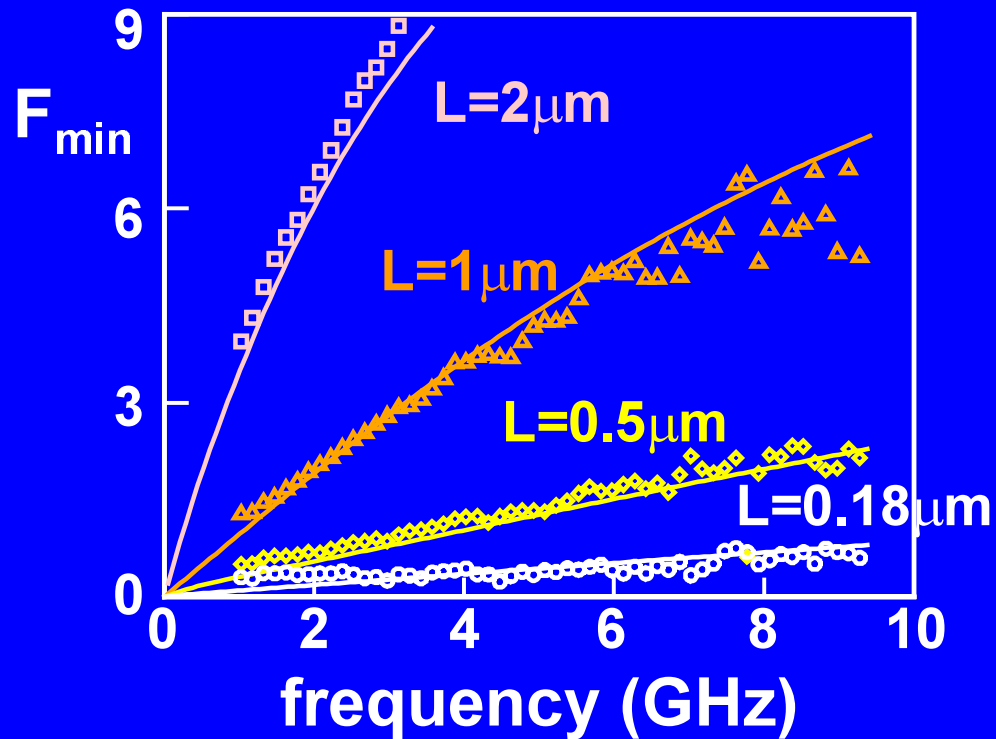


$L=0.18\mu\text{m}$



- reasonable agreement correlation coefficient
- limited by measurement accuracy

minimum and 50Ω noise figure



F_{min} of $0.18 \mu\text{m}$ NMOS well below 1dB for $f < 10$ GHz

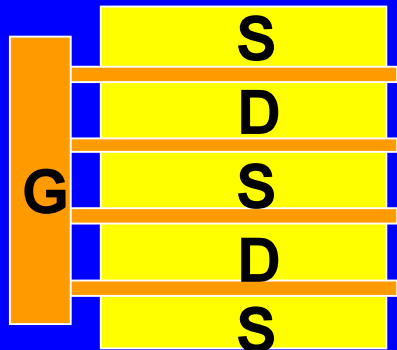
F_{50} of $0.18 \mu\text{m}$ NMOS well below 2dB for $f < 10$ GHz

contents

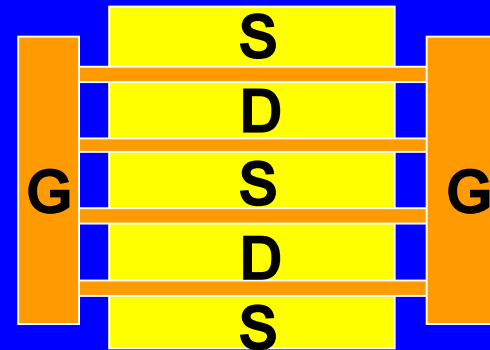
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layout effects (introduction)

standard, fold = 1, contact = 1



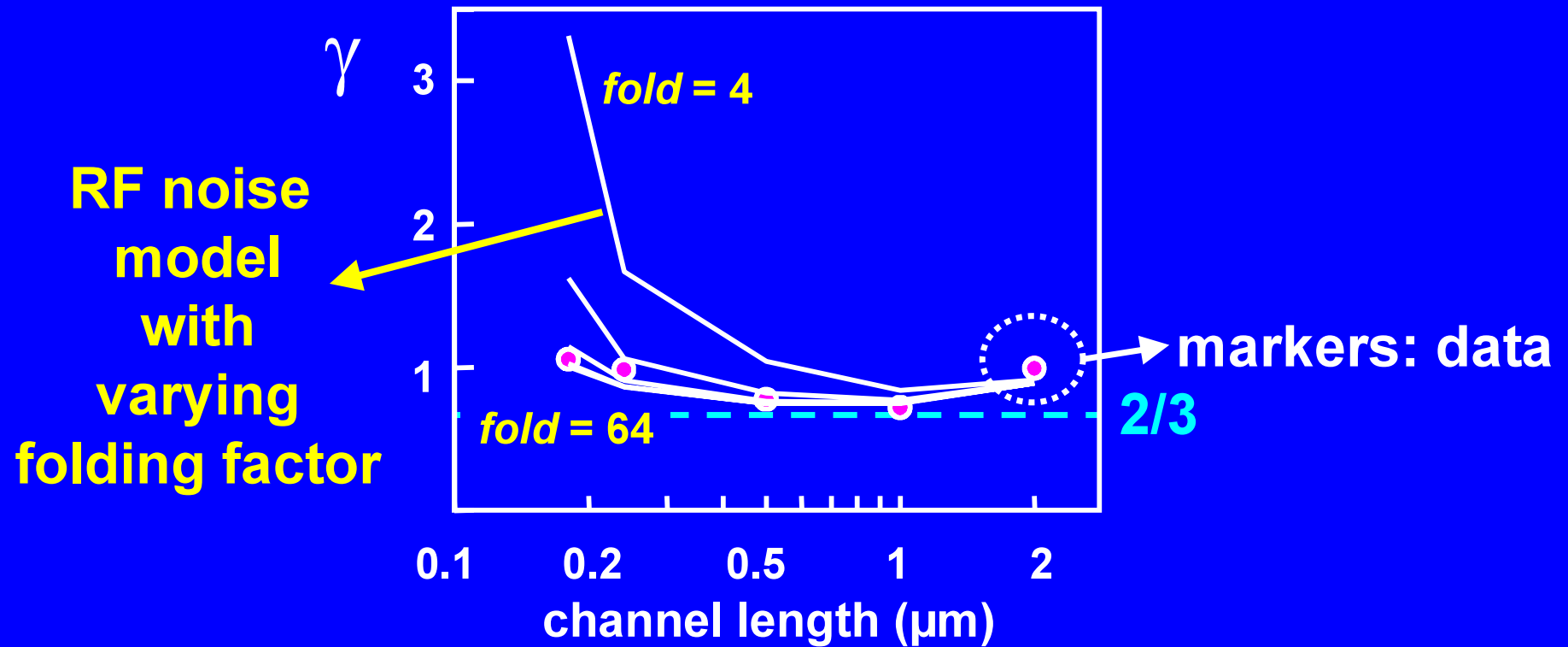
fold = 4, contact = 1



fold = 4, contact = 2

$$R_{gate} = \frac{W_g \cdot R_{sheet}}{3 \cdot fold^2 \cdot contact^2 \cdot L_g}$$

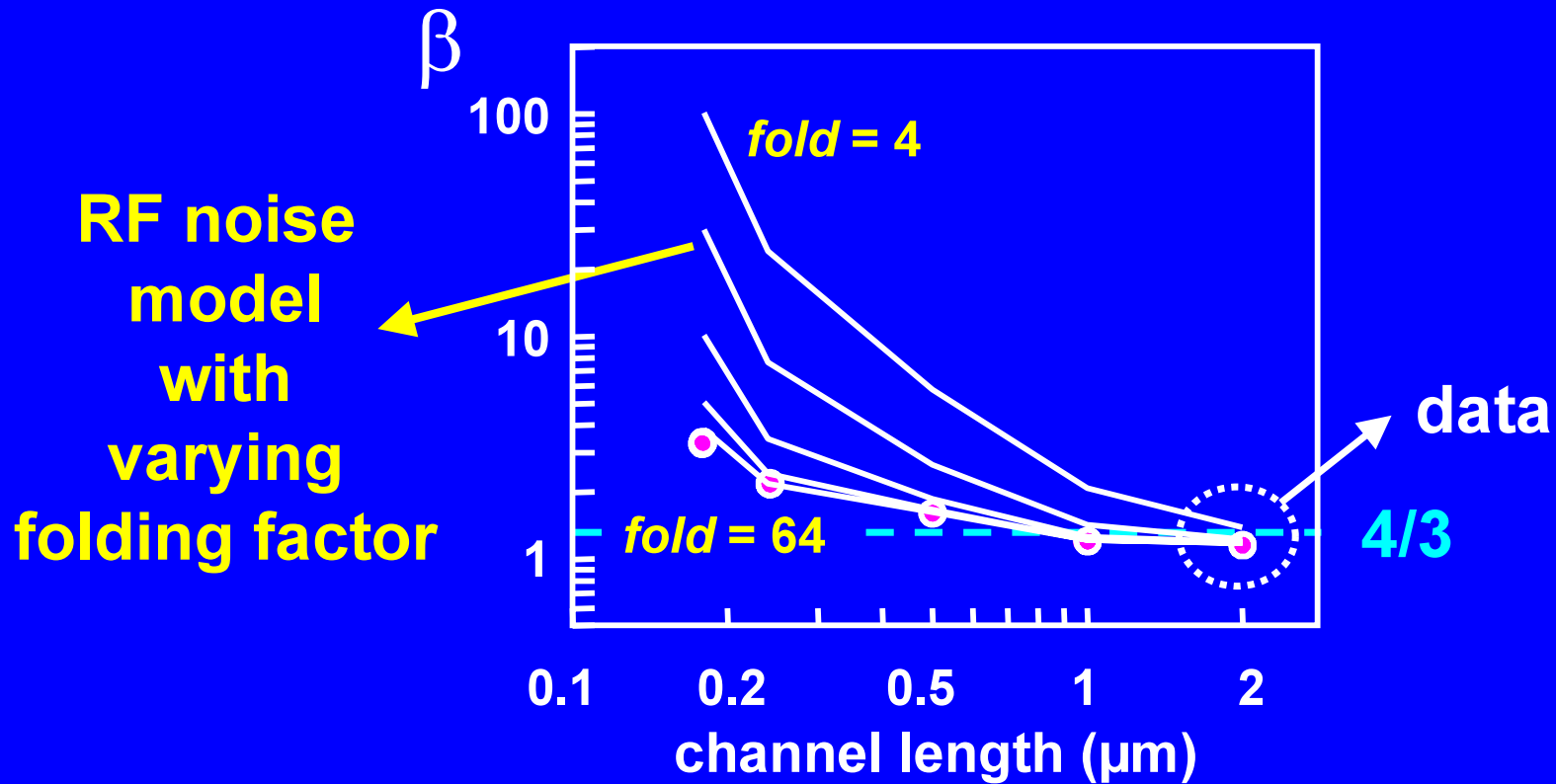
layout effects (drain current noise)



increase of γ with decreasing folding factor

layout effects (gate current noise)

$$S_{ig} \equiv \beta \cdot \frac{4 k_B T \cdot (\omega C_{GS})^2}{5 g_{do}}$$

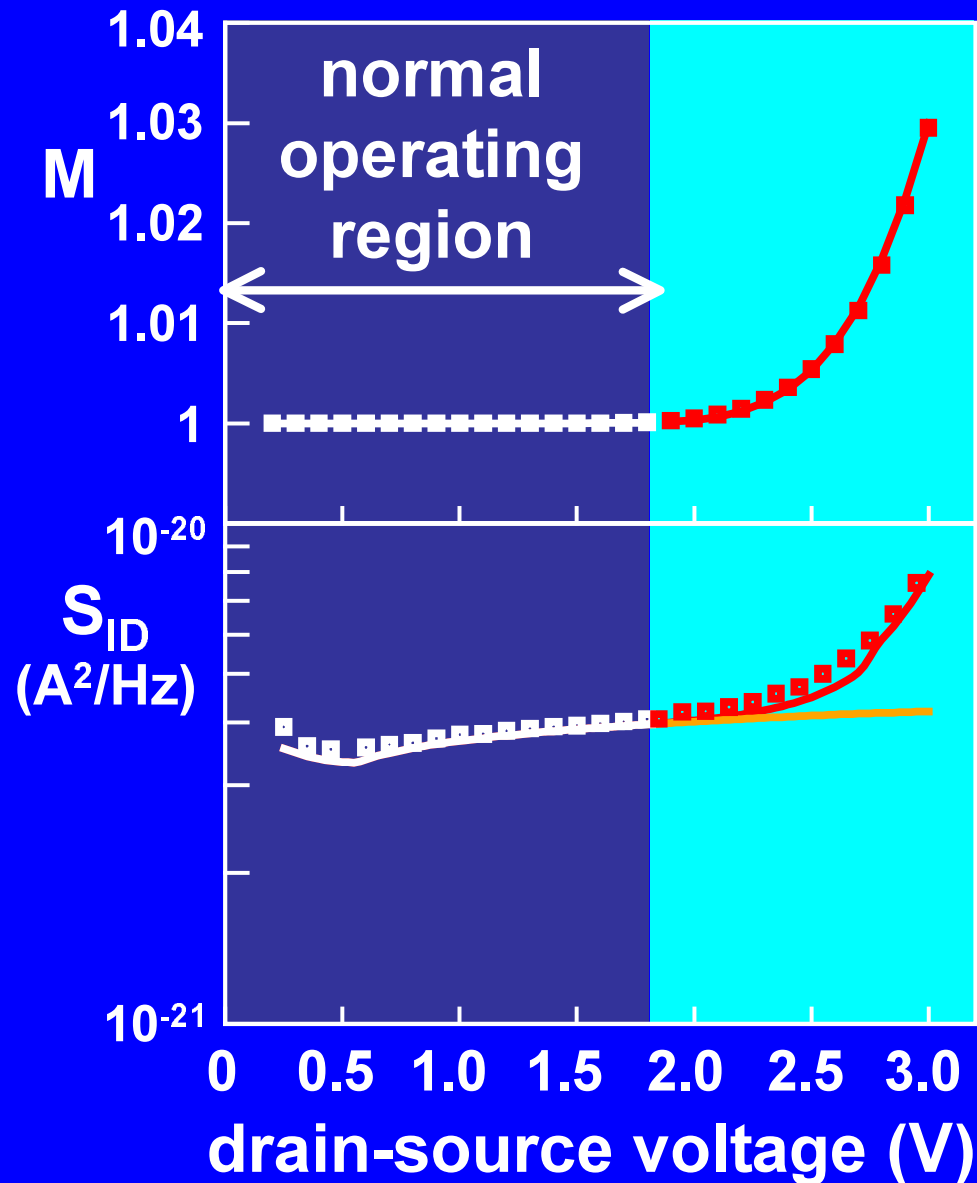


*dramatic increase of β
with decreasing folding factor*

contents

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avalanche noise



avalanche multiplication:

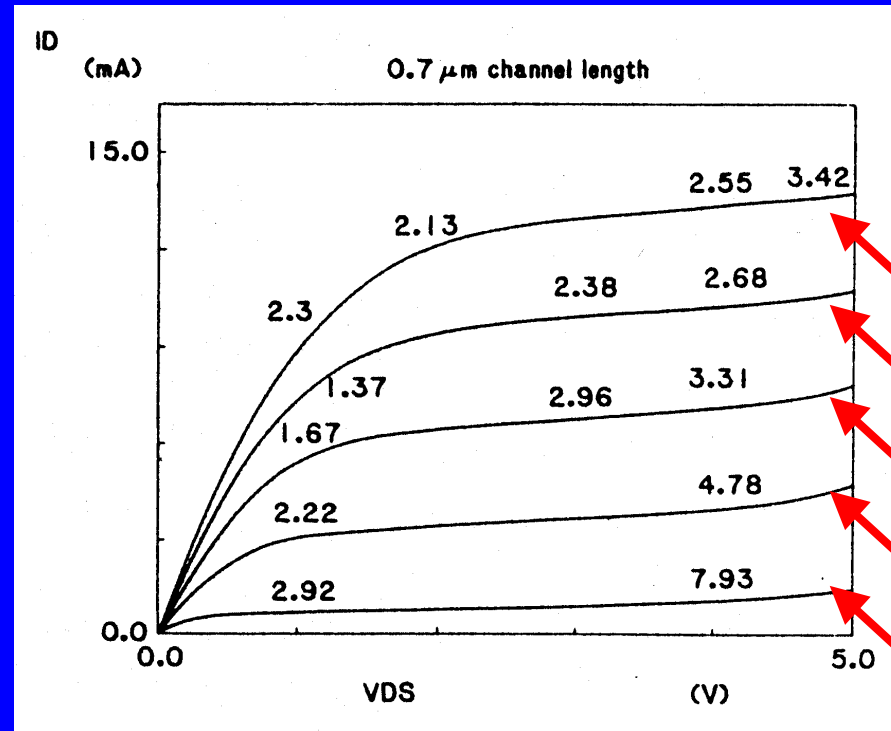
$$M \equiv \frac{I_D}{I_S} > 1$$

avalanche noise
[van der Ziel (1978)]:

$$S_{ID} = M^2 \cdot S_{IS} + 2 \cdot q \cdot I_B \cdot (M - 1)$$

avalanche noise

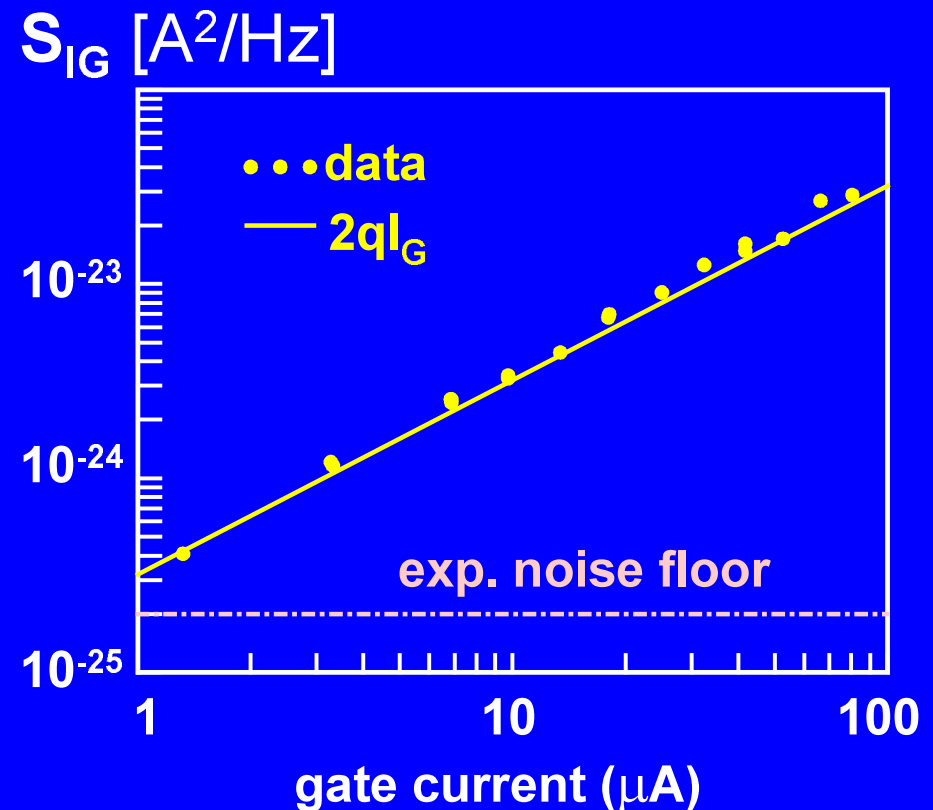
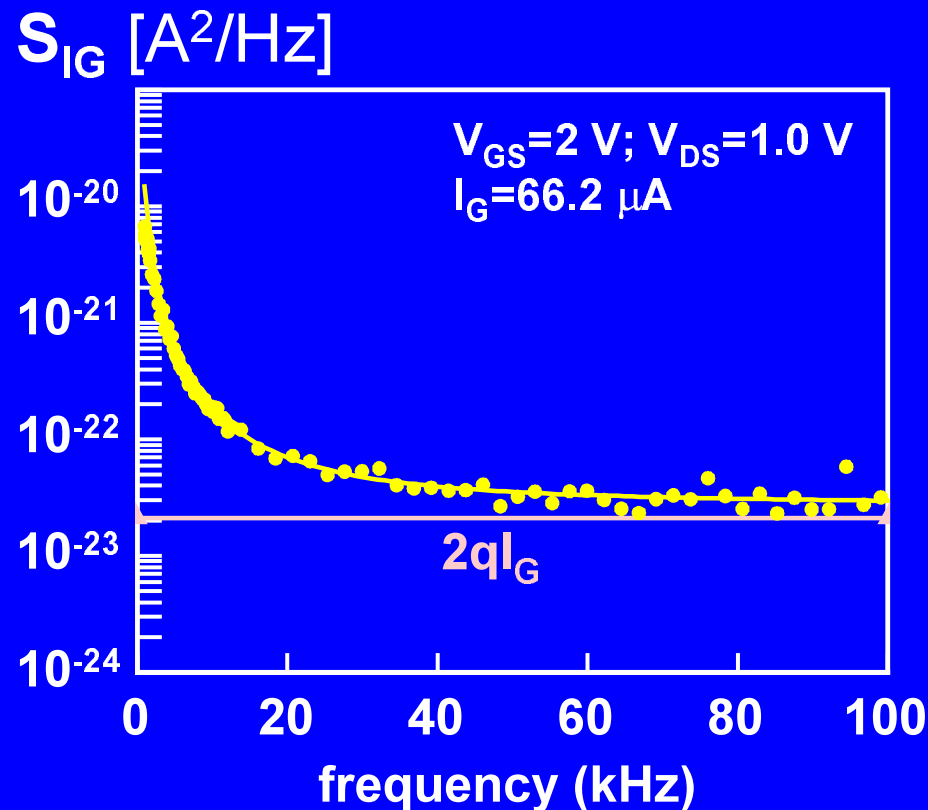
Abidi (1986)



additional noise Abidi partly due to excessive bulk current

shot noise in gate leakage current

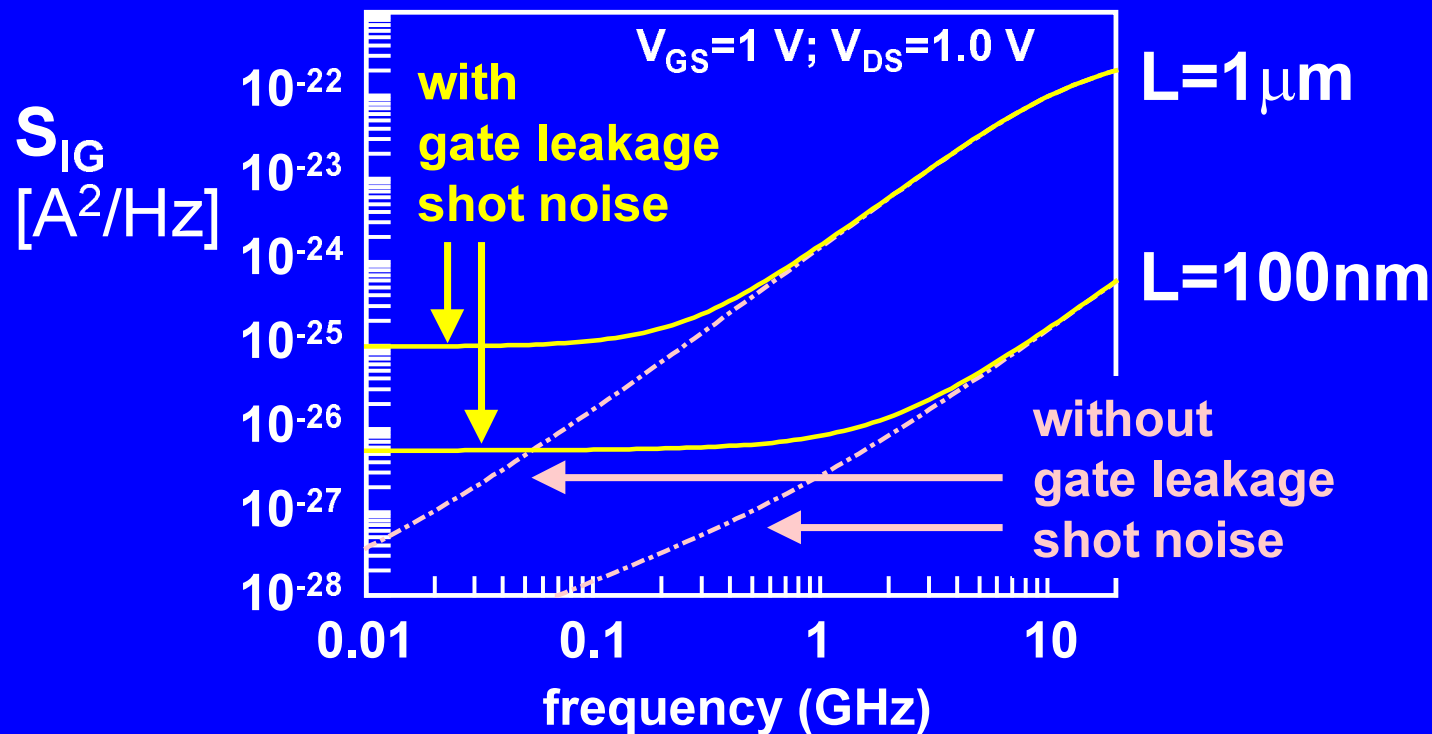
low-frequency noise in a 10/10 n-channel
with 1.5 nm EOT



*first experimental observation of shot noise
in gate leakage current*

shot noise in gate leakage current

impact on RF noise behavior
simulated using RF noise model



*shot noise in gate leakage current
only relevant at intermediate frequencies*

contents

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- additional noise sources
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conclusion (I)

drain current noise

- *no* observation of large enhancement thermal noise in deep-submicron CMOS
- confirmed by MC simulations
- model without carrier heating gives excellent results
- without any parameter fitting

conclusion (II)

gate current noise

- **enhancement in deep-submicron CMOS**
- **short channel devices:**
gate resistance dominates
even for optimized device layouts
- **due to silicide-to-polysilicon contact resistance**
- **may explain some results in literature**
- **deep submicron CMOS: attractive noise figures**