BJT Modeling With VBIC, Basics and v1.3 Updates

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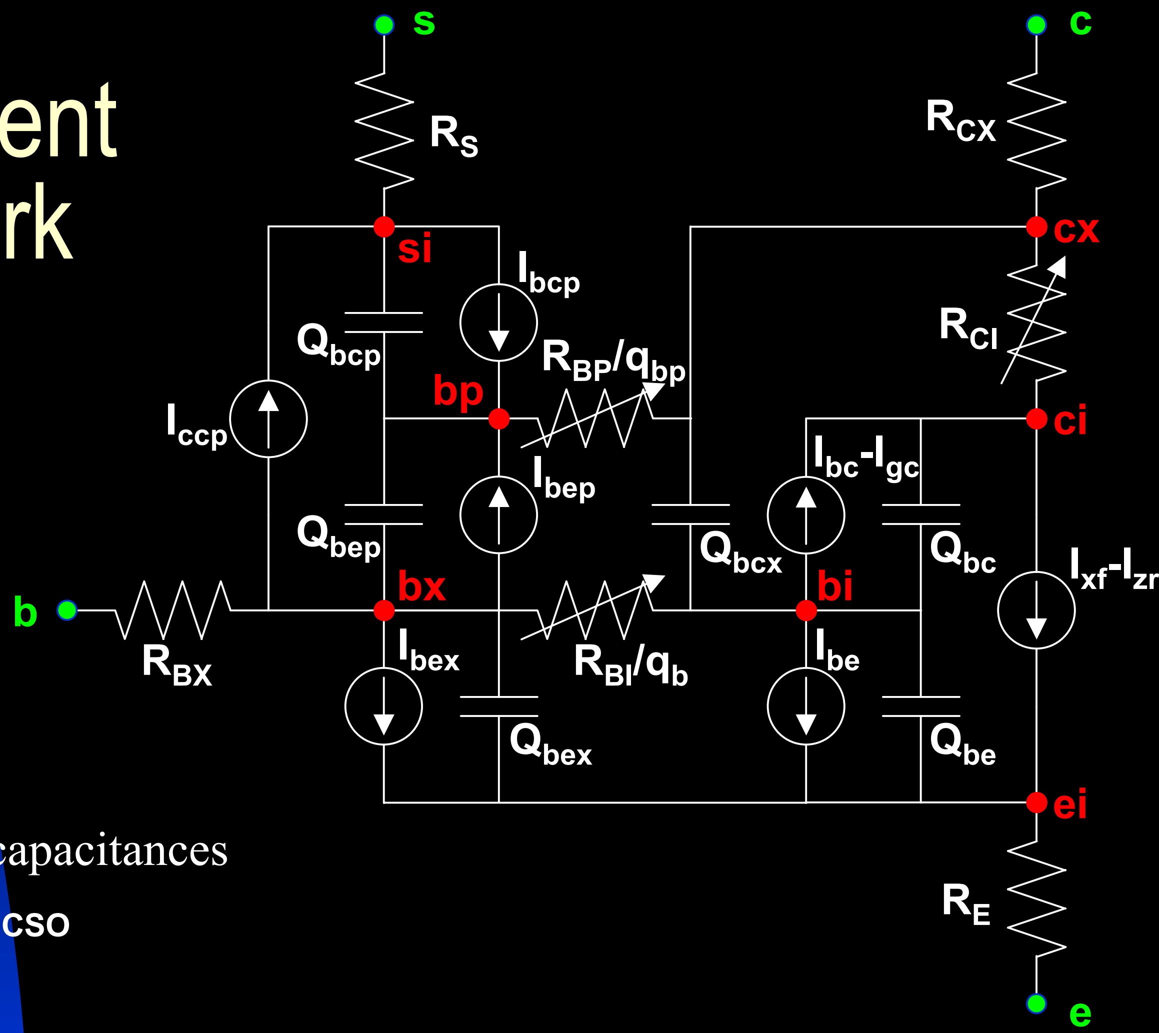
Outline

- Introduction
- Review of VBIC v1.2
- Updates for VBIC v1.3
  - General simulator/convergence updates
  - Other general updates
  - Depletion R_C model for vertical PNPs
  - Excess phase reformulation
  - Quasi-neutral base recombination
  - IBM and NSC updates

Equivalent Network



Not shown:

Fixed overlap capacitances

C_{BEO}, C_{BCO}, C_{CSO}

VBIC v1.2 Compared to SGP

- Separation of I_c and I_b, not linked via B_F
- Early effect model based on depletion charge
- Full parasitic PNP modeling
- Self-heating modeling
- Base-emitter breakdown model
- Weak avalanche model
- Improved depletion, diffusion charge models
- Improved temperature modeling
- Constant overlap capacitances

VBIC v1.3

- Under development now
- Some updates finished, others planned
- General areas of enhancement
  - Robustness
  - Incremental additions (e.g. extra TCs)
  - Improvements for higher voltage device modeling
  - Other additions (IBM, NSC)

Robustness

- `gmin` and `pnjmaxi` explicitly added to model formulation
  - Before expected to be added, simulator specific
- Explicit linearization added, above `pnjmaxi`
- Improved numerical protection for normalized base charge and weak avalanche models
- Max/Min implemented for local temperature
- Shrink factor support added

PNPV R_C Modulation

- No P^+ buried layer
- Depletion pinching of collector, by substrate/isolation, modulates R_C
- Can be modeled, approximately, in a subckt by including a JFET for R_C
- Included as alternative R_C modulation model, based on diffused resistor model

$$I_{rci} = \frac{V_{rci}}{R_{CI}} \left(1 - D_{FC} \sqrt{P_{FC} + 2V_{cx-si} + V_{rci}} \right)$$

Base-Collector "Pinning"

- For lightly doped collectors with no buried layer, the base-collector depletion region can push through to the substrate/isolation
- C_{bc} drops sharply at that point
- Early voltage increases sharply at that point
  - Still some Early effect from sidewall
- Implemented via two components of Q_{BC}, with a "pinning" voltage at which the charge from one component (smoothly) limits

Self-Heating Modeling

- VBIC was the first new generation BJT model to include self-heating
  - Primarily because of extremely easy implementation, automated code generation from a high-level model description
- Simple single R_{TH} and C_{TH} model, also adopted by other models, has limitations
- VBIC v1.3 has $R_{TH}(T)$ model
- Considering adding multi-pole Y_{TH} model

Proc. APMC
pp. 716-721, 2001

VBIC MODEL APPLICABILITY AND EXTRACTION PROCEDURE FOR InGaP/GaAs HBT

S.V. CHEREPKO and J.C.M HWANG
Lehigh University

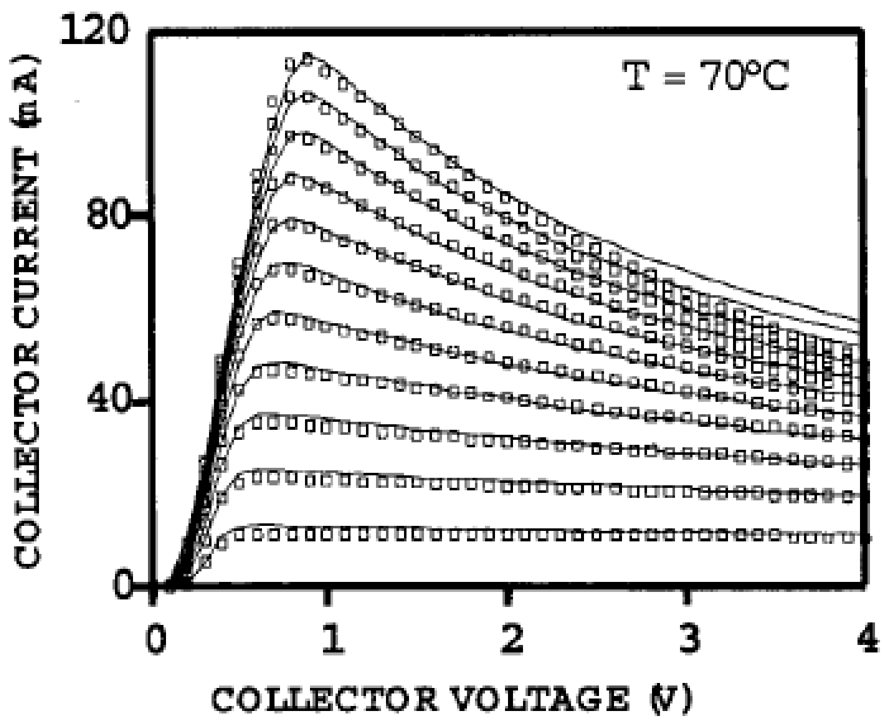


Fig. 4 (symbols) Measured vs. (lines) simulated *I-V* characteristics.
I_B = 0.075,0.15,...,0.875 mA bottom top.

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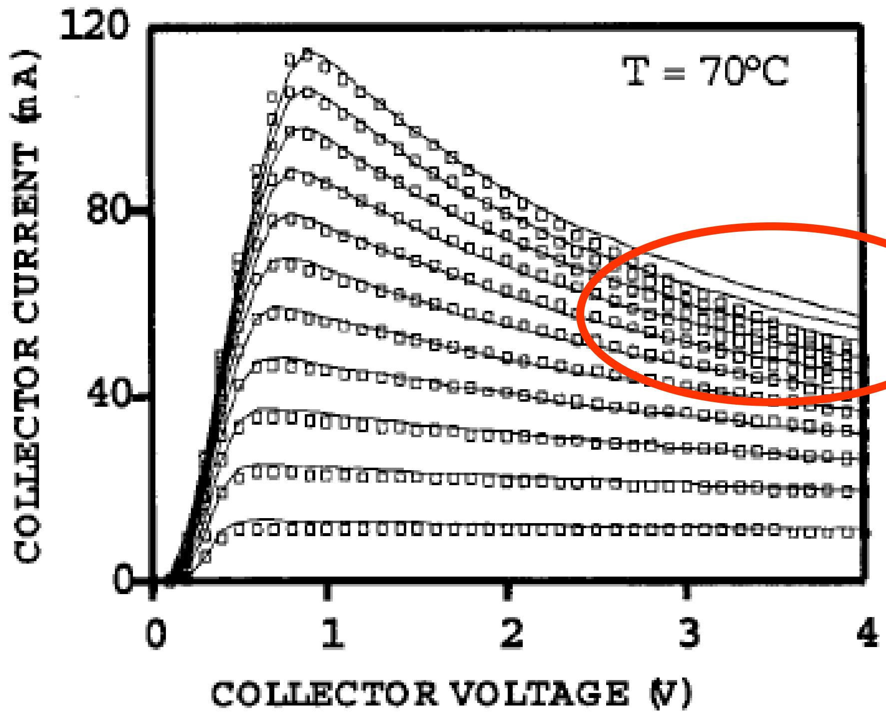

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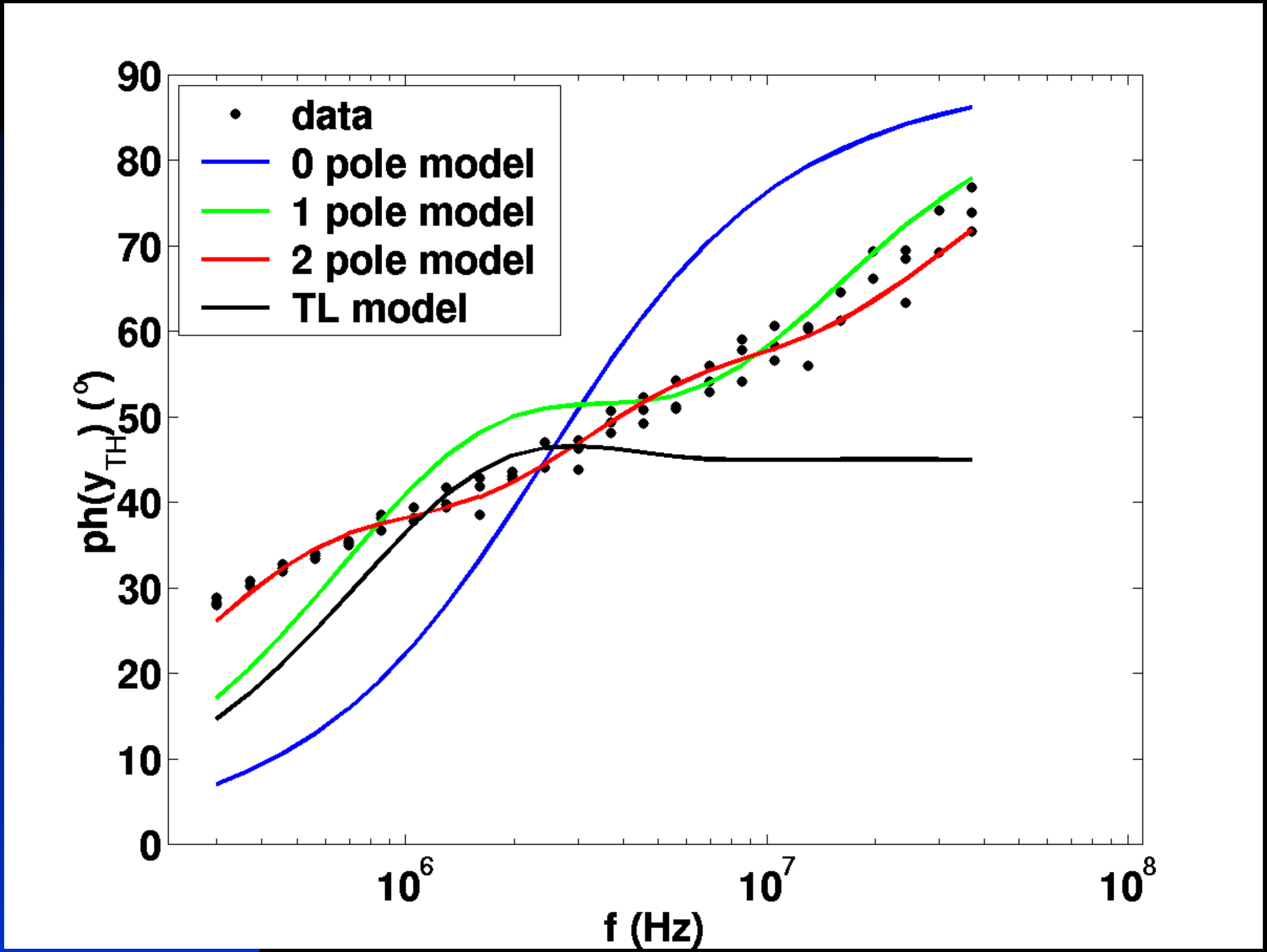
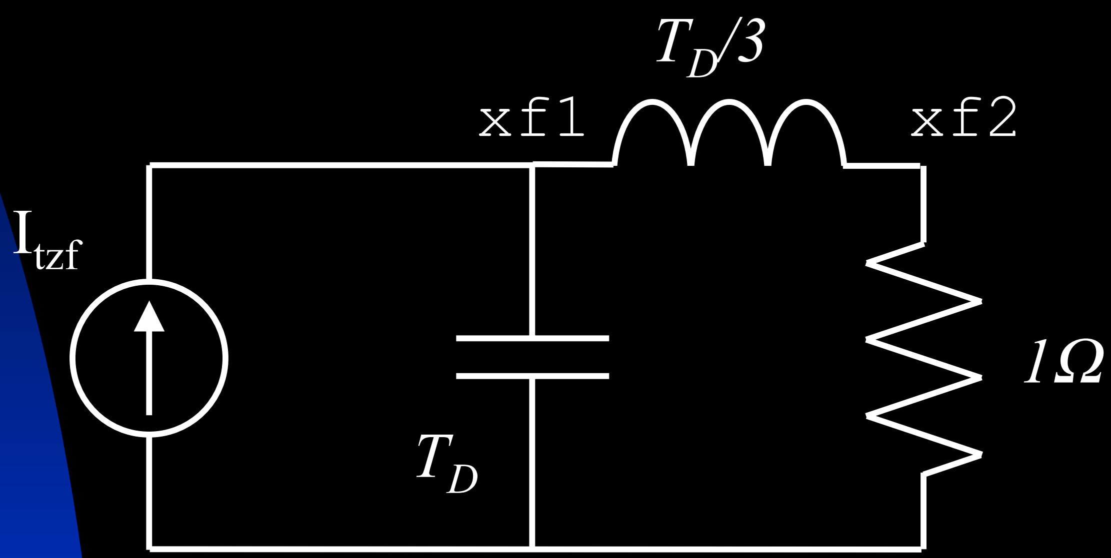
Extracted Ph(y_{TH})



Excess-Phase Remapping

- Original Weil-McNamee formulation implemented as RLC circuit



Excess-Phase Remapping

- Consistent for all analyses types, not just for AC or transient
- Inductor is messy to handle in nodal formulation
- Only really 2 unknowns as inductor current equals V(xf2), do not have to carry extra current in MNA formulation
- Non-standard for implementation

Excess-Phase Remapping

$$I_{tzf} - ddt(T_D V(xf1)) - I_L = 0$$

$$I_L - V(xf2) = 0$$

$$V(xf1) - V(xf2) = ddt(I_L T_D / 3)$$

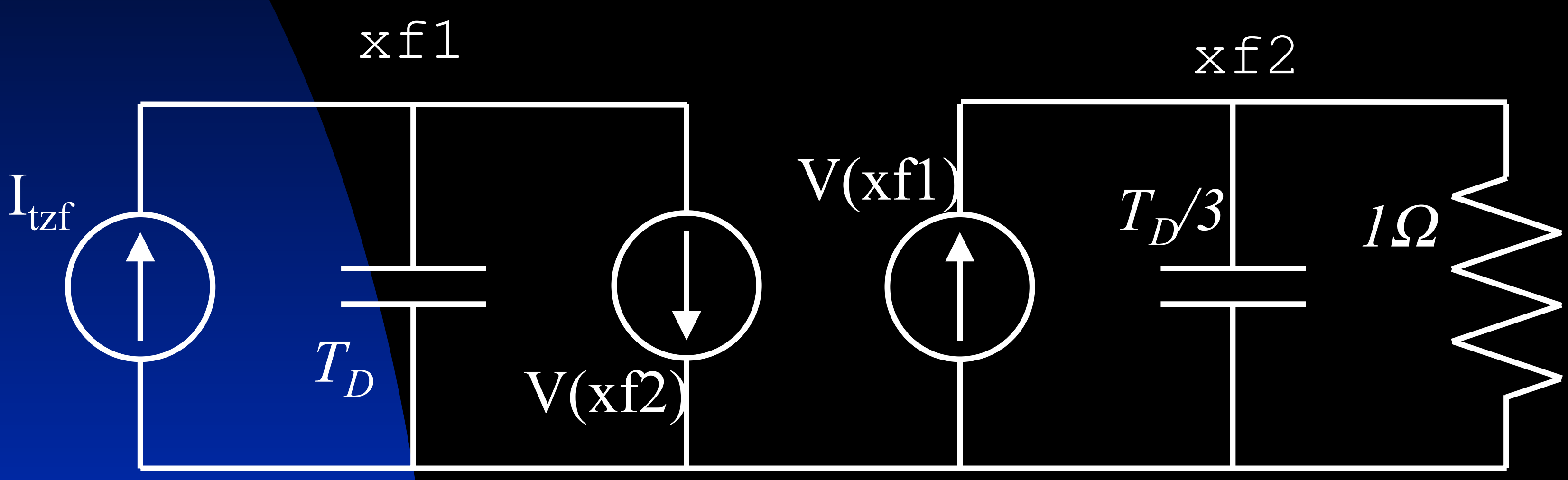
Excess-Phase Remapping

$$I_{tzf} - ddt(T_D V(xf1)) - V(xf2) = 0$$

$$V(xf2) + ddt(V(xf2)T_D/3) - V(xf1) = 0$$

Excess-Phase Remapping

- Equivalent in VCCS type elements



Early Voltages

- Temperature dependence of the Early effect determined by the temperature dependence of depletion charge model
- Not accurate enough for some devices, especially those with low built-in potentials at high temperature
- Linear TCs added for Early voltages

$$V_{EF}(T) = V_{EF}(T_{NOM})(1 + TC_{VEF}(T - T_{NOM}))$$

Reverse Operation

- First order theory ties, through reciprocity, reverse I_S to forward I_S
- Data shows this is not always a good approximation
  - Especially for III-V HBTs
- A separate I_S is provided for reverse operation, with a separate TC
- Implemented as ratio w.r.t. forward I_S, for simple extraction and compatibility

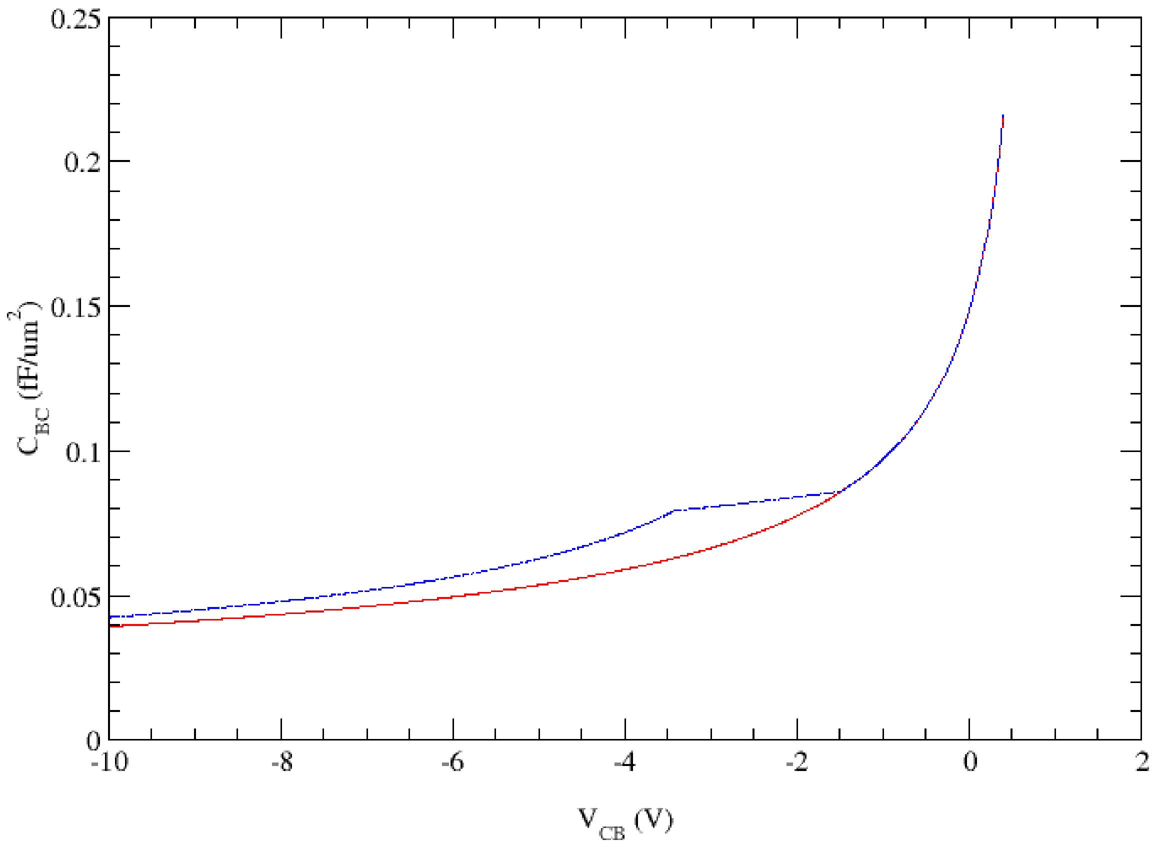
Transit Time

- VBIC v1.2 transit time model from SGP, with minor addition of depletion modulation
- Recognized weak part of the model
- Is being updated for v1.3, based on both SiGe HBTs and high voltage devices (NPN and PNP) in SmartPower technologies

Variable Collector Doping Model

- Has been shown that adjusting the collector doping profile with different levels and spikes can improve large signal linearity
- Some devices also have variable dopings in the collector
- Empirical collector doping model implemented
  - Parameterized in terms of voltage rather than depth, for simple parameter extraction

Collector-Base Capacitance



Quasi-Neutral Base Recombination

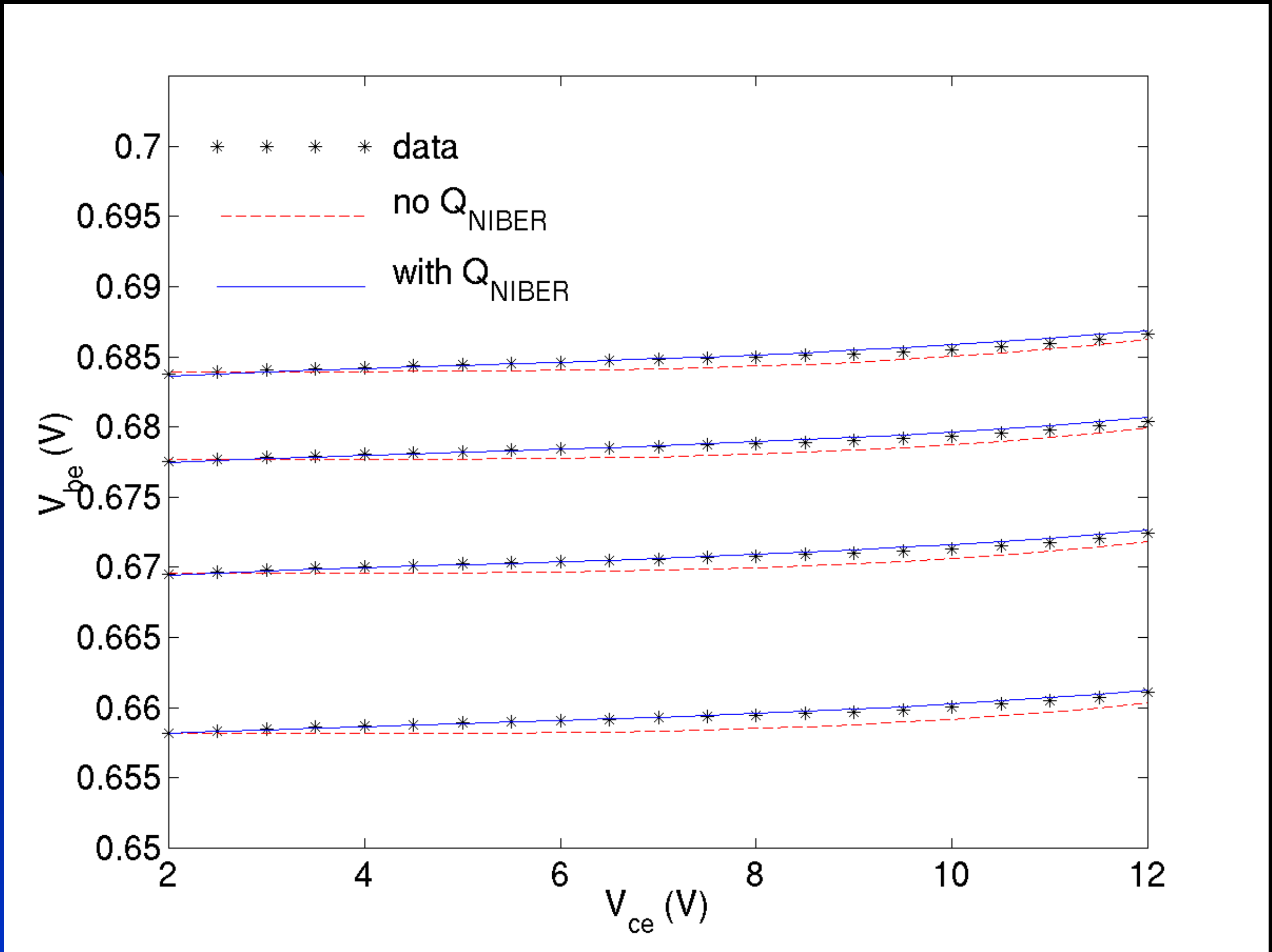
- VBIC I_b model is based on recombination and generation in the quasi-neutral emitter, and the emitter contact, and in the base-emitter space-charge region
- In wide base devices neutral base recombination also occurs
  - Visible in output characteristics, and in β variation with collector bias

Quasi-Neutral Base Recombination

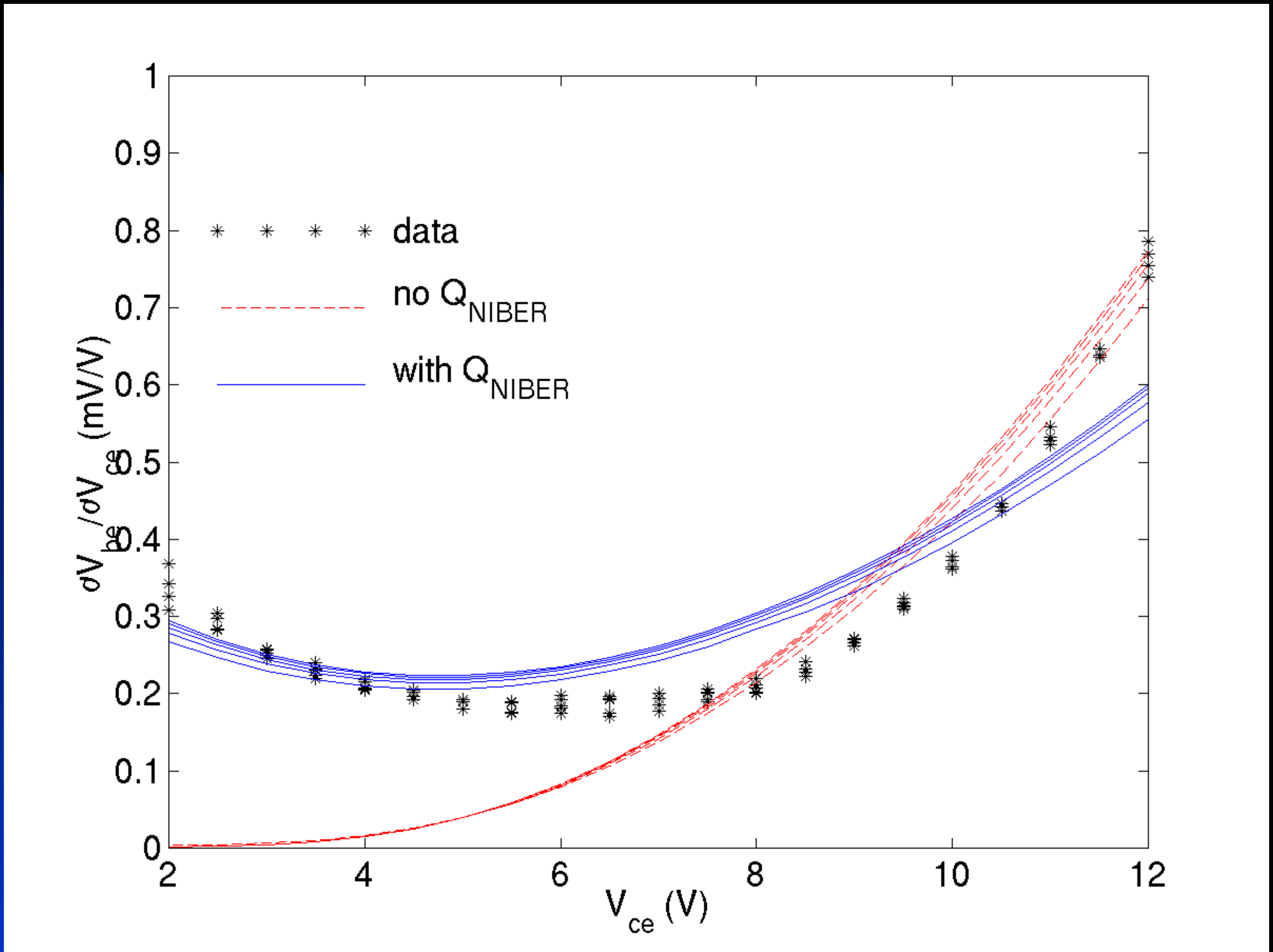
- The base volume is linked to the q_1 component of normalized base charge
  - Although details of N(x), which affects R/G, are not included
- Separate I_{BEI} into emitter and base components

$$I_{BEI} = I_{BEI}^{e} + I_{BEI}^{b} q_1 = I_{BEI}^{0}\left(1 + Q_{NIBEIR}\left(q_1 - 1\right)\right)$$

Quasi-Neutral Base Recombination



Quasi-Neutral Base Recombination



IBM Updates

- Alternative placement of control voltages for weak avalanche for high breakdown devices
- Slightly modified avalanche expression for this also
- Separate depletion capacitance parameters for C_{JC} and C_{JEP}
- Temperature dependent transit times
  - Linear temperature dependence
- Acknowledge D. Sheridan for provision of details

NSC Updates

- Model for I_B bias and geometry dependence for special effect seen in SiGe devices provided by A. Sadovnikov of NSC
- Details to be published elsewhere

Summary

- Updates for VBIC v1.3 in progress at present, target release date April 2003
- Details of some updates provided
- Others still in implementation
- Model is defined in Verilog-A, updates are implemented there, C code is generated from this