Compact Modeling for RF and Microwave Integrated Circuits

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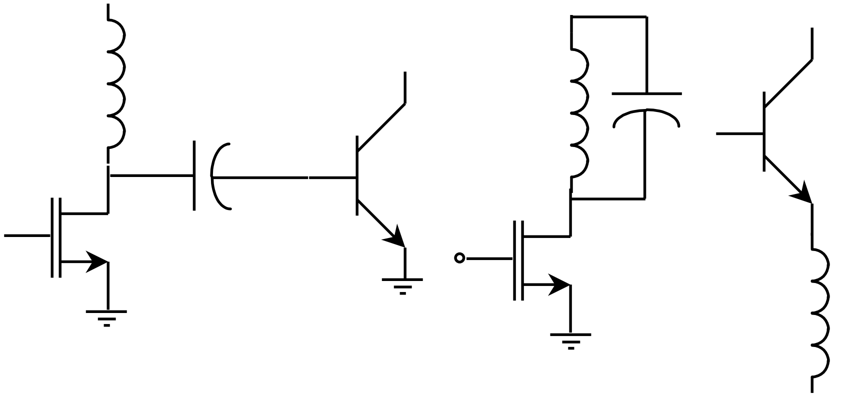
BSIM

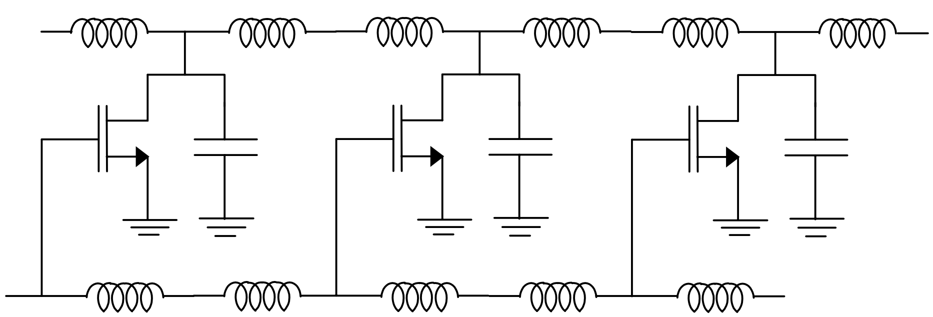
BWRC

Outline

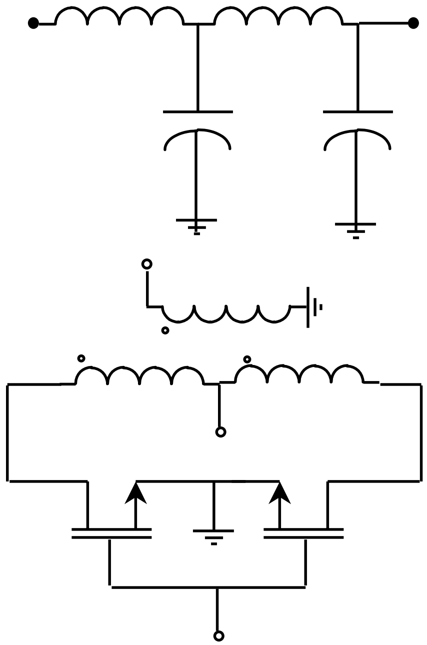
- RF and Microwave Applications
- Insights from Maxwell's Equations
- Inductors and Transformers
- Capacitors and Varactors
- Transmission Lines and Resistors
- Substrate Coupling, IC Interconnect
- Package and PCB Modeling
- Active Device Modeling

Applications of Compact Models

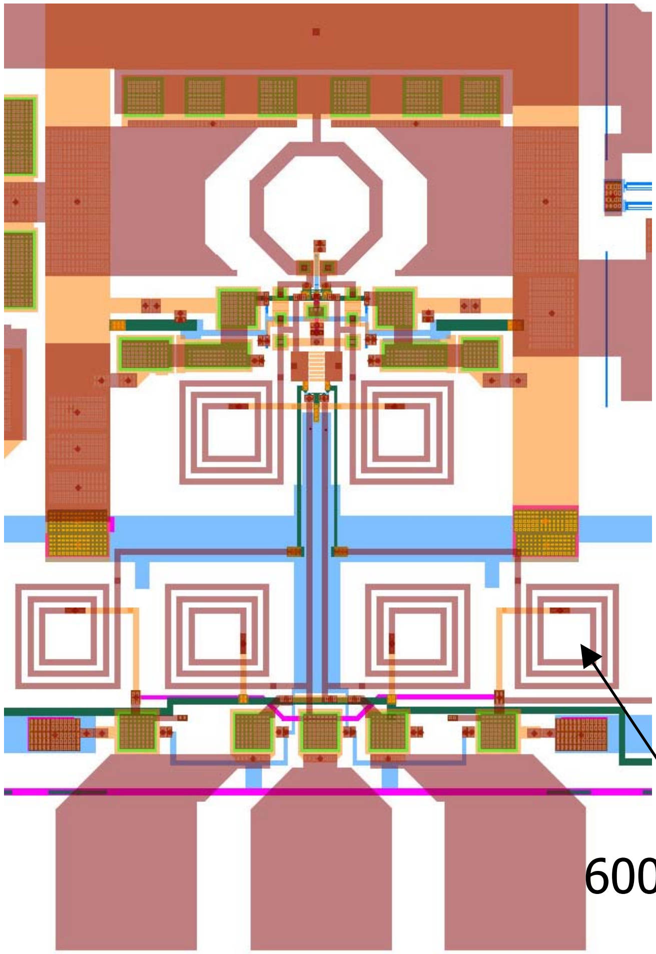




- Narrow-band impedance matching
- Tuned loads (resonant tank)
- Low noise degeneration and feedback
- Linear filters (high dynamic range)
- Fully differential circuits
- Artificial transmission lines
- Low voltage/low power design



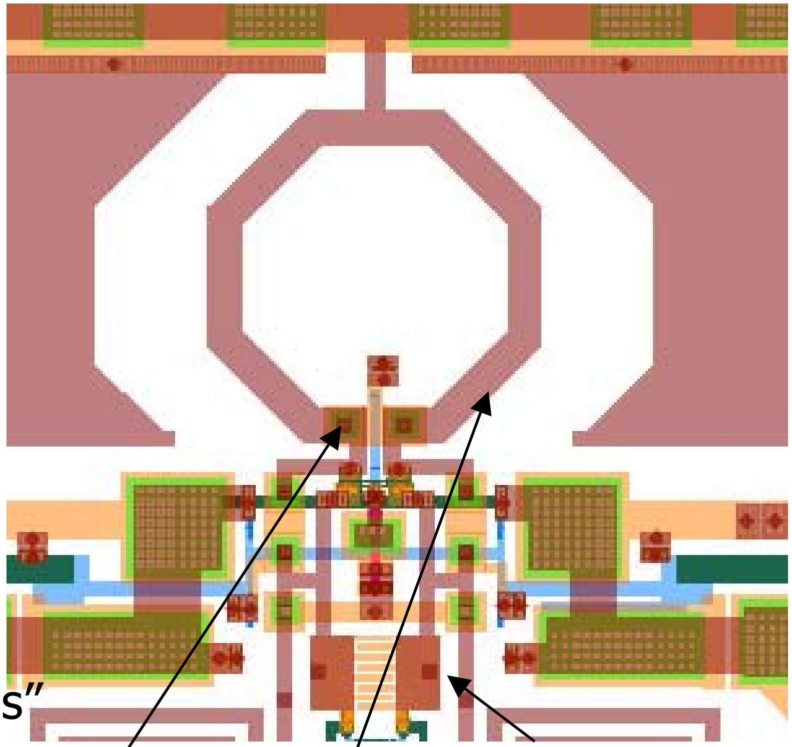
“RF” Compact Modeling



600 pH “Chokes”

- 55 GHz Oscillator Layout
- Passives “Lumped”

Low Loss MIM Cap and Inductor Ring
Tightly Coupled for Low Loss

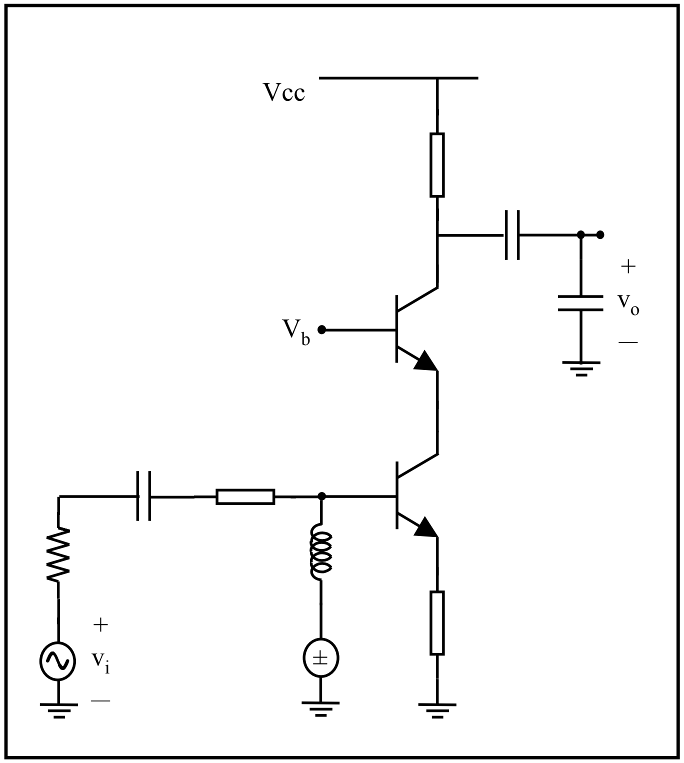


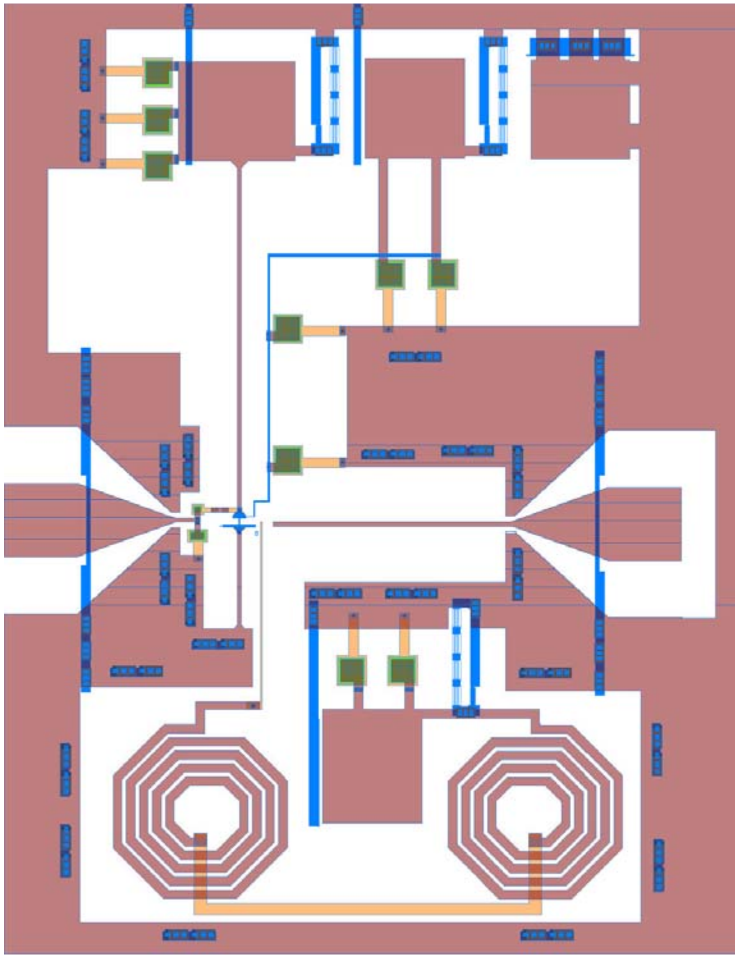
Tank MIM

Low-Loss Custom
Cap Divider

150 pH Loop
Q>30 (HFSS)

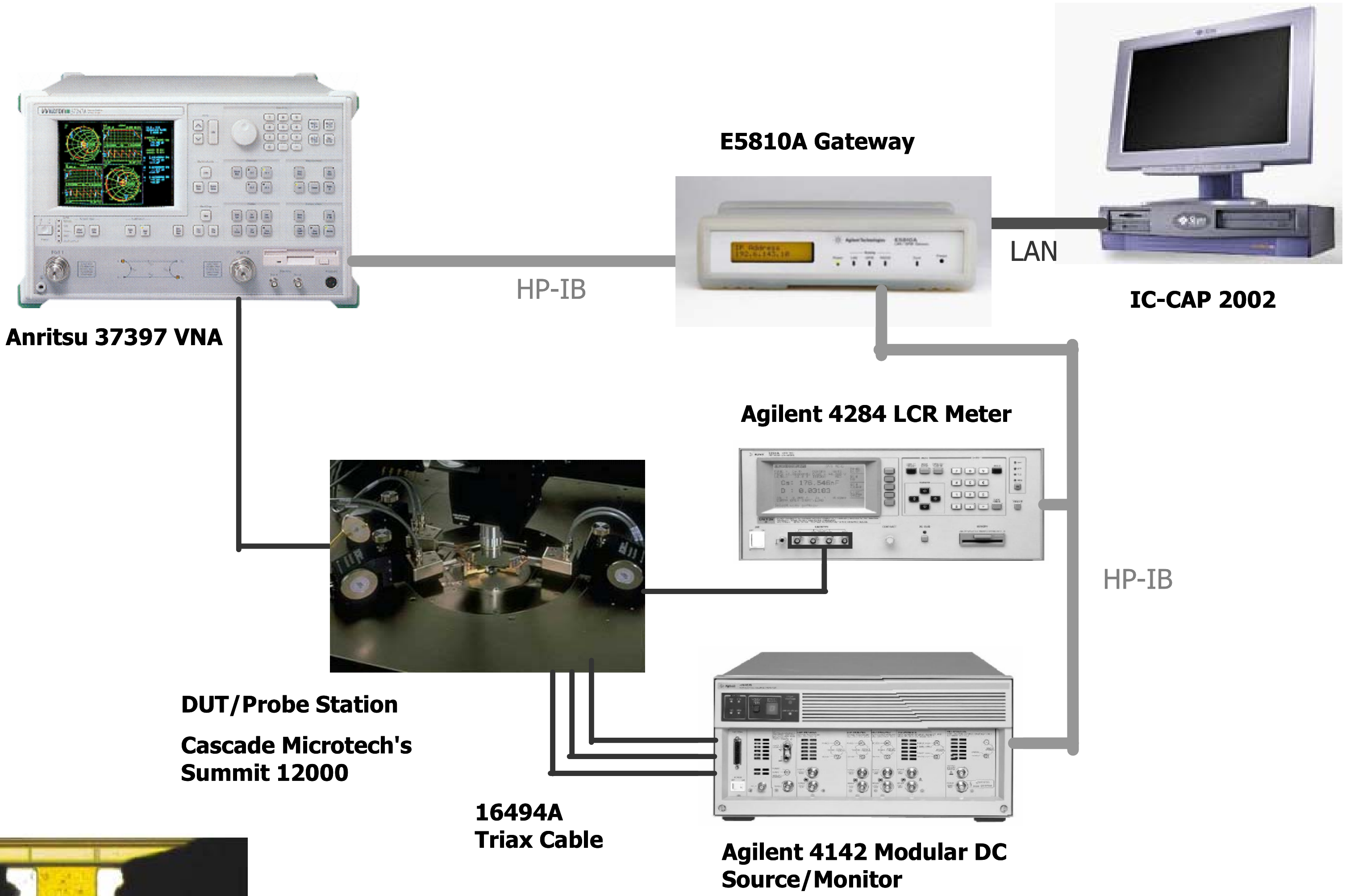
“Microwave” Compact Modeling





- 28 GHz LNA
- Embrace Distributed Circuit Elements

Measurements at Microwave



E5810A Gateway

Anritsu 37397 VNA

HP-IB

LAN

IC-CAP 2002

Agilent 4284 LCR Meter

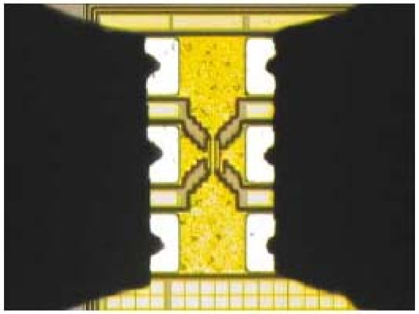
HP-IB

DUT/Probe Station

Cascade Microtech's
Summit 12000

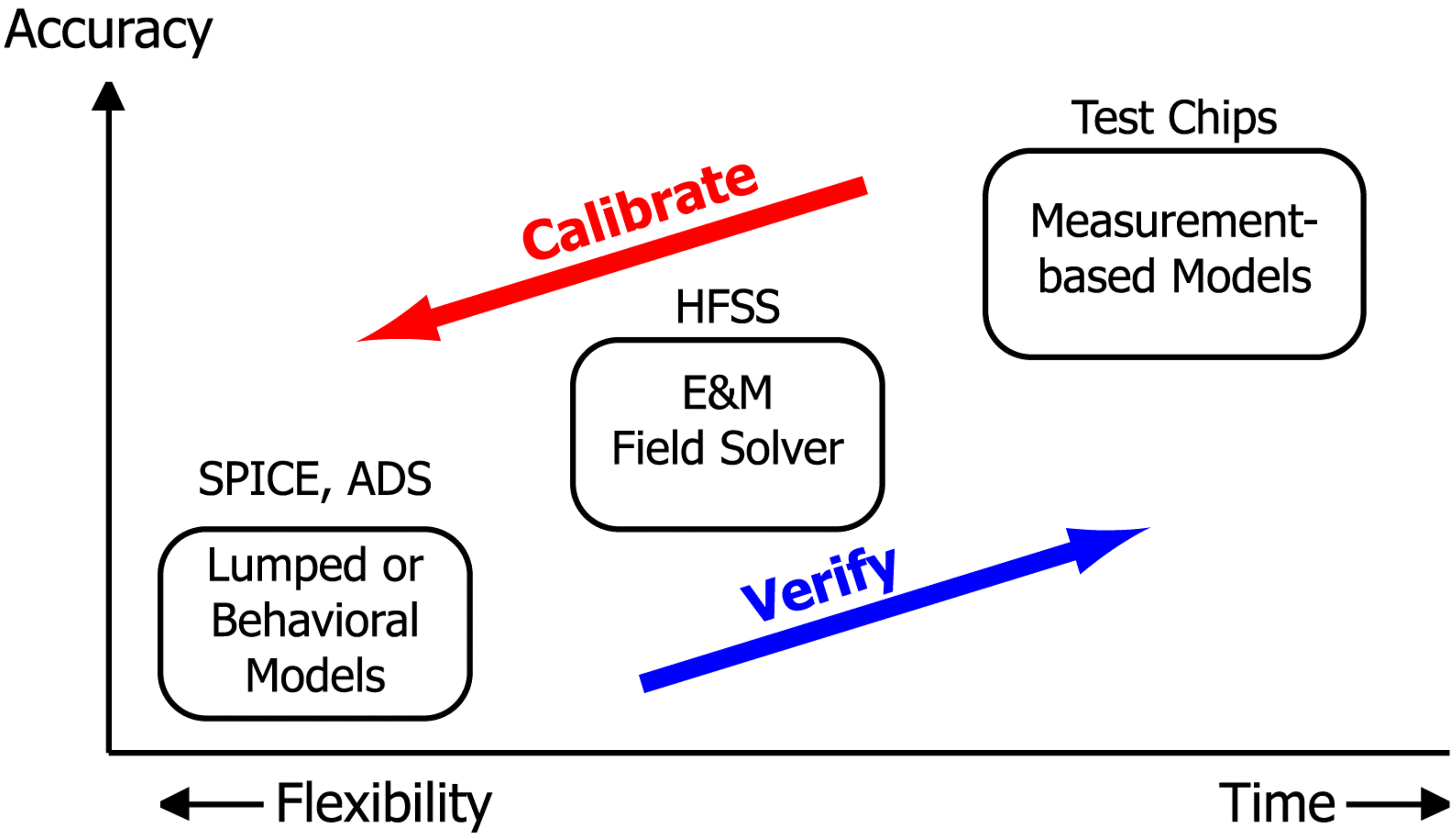
16494A
Triax Cable

Agilent 4142 Modular DC
Source/Monitor



De-embedding and calibration difficult ⇨
Accurate measurements difficult to make above 20 GHz

Compact Modeling Methodology



Calibrate and verify simpler models using most accurate data available

Electromagnetism from Circuit Perspective

Consider the induced field E' due to an applied field E_0

$$E = E_0 + E' = E_0 - \nabla\Phi - \frac{\partial A}{\partial t} = \frac{J}{\sigma}$$

Now integrate above expression over the conducting path

$$\int E_0 \cdot dl - \int \frac{J}{\sigma} \cdot dl - \int \frac{\partial A}{\partial t} \cdot dl - \int \nabla\Phi \cdot dl = 0$$

applied voltage

internal impedance

external inductance

capacitive term

Insights from Maxwell’s Equations

- From Maxwell’s equations (Coulomb Gauge):

$$-\nabla^2 A = j\omega\mu\varepsilon E + \mu J = j\omega\mu\varepsilon'(-j\omega A - \nabla\phi)$$

$$= \underbrace{\omega^2\mu\varepsilon A}_{\text{radiation}} - \underbrace{j\omega\mu\sigma A}_{\text{eddy currents}} - \underbrace{j\omega\varepsilon\mu\nabla\phi}_{\text{disp.}} - \underbrace{\mu\sigma\nabla\phi}_{\text{conduction}}$$

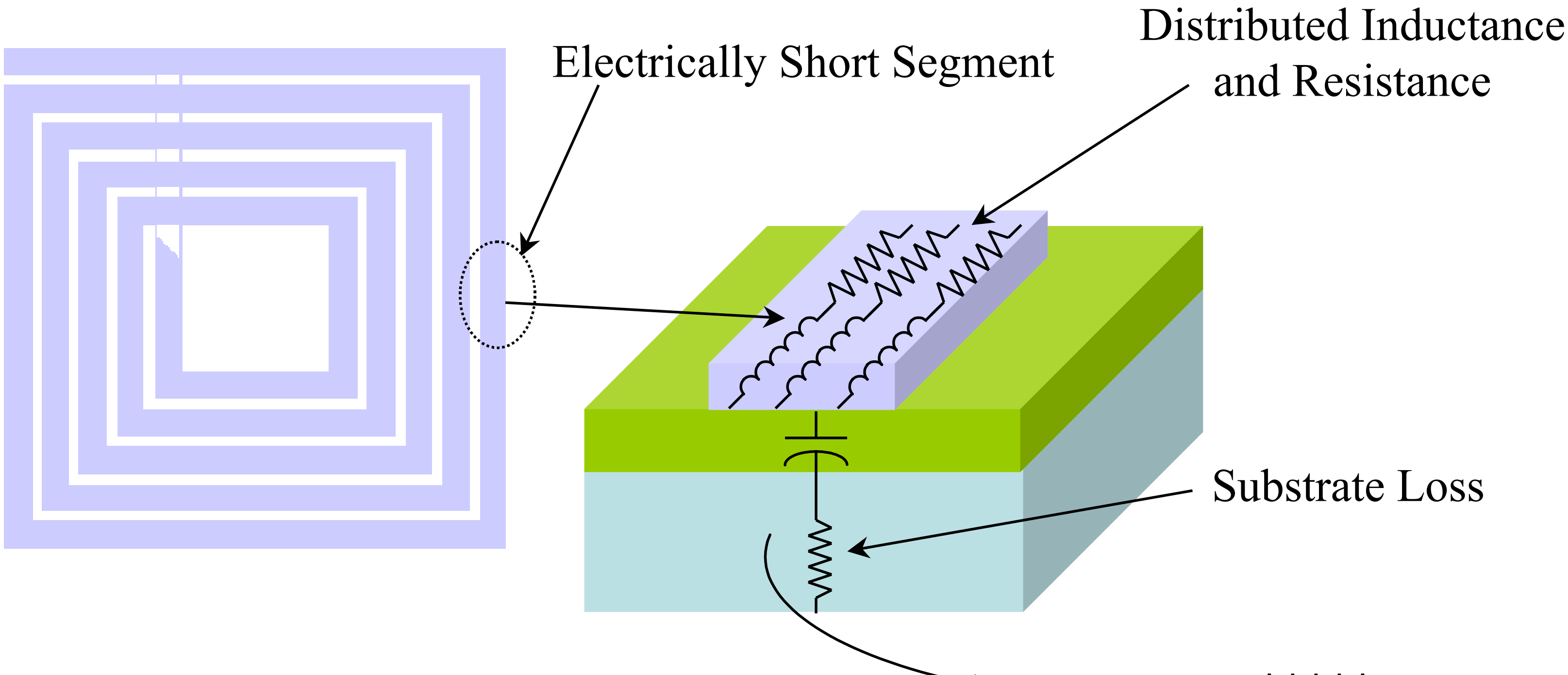
- Neglect radiation as long as $l_{\max} << \lambda$
- Displacement and conduction current are curl-free
- Losses due to conduction currents accounted for by solving:

$$\nabla^2\phi = -\frac{\rho}{\varepsilon'} \qquad \varepsilon' = \varepsilon + \frac{j\sigma}{\omega}$$

- Losses due to eddy currents accounted for by solving:

$$\nabla^2 A = j\omega\mu\sigma A$$

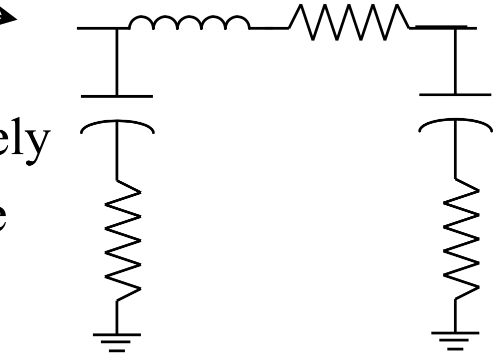
PEEC Formulation



Electrically Short Segment

Distributed Inductance and Resistance

Substrate Loss



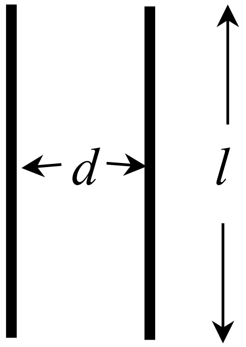
- Model short metal segment as lumped RLC Circuit
- Metal segments are linked capacitively and inductively
- Set up node equations for complete system and solve
- Method equivalent to solving Maxwell’s Equations

Reference: A. Ruehli, H. Heeb, *MTT*, July ‘92

Partial Element Equivalent Circuits (*PEEC*)

Analytic Inductance Computation

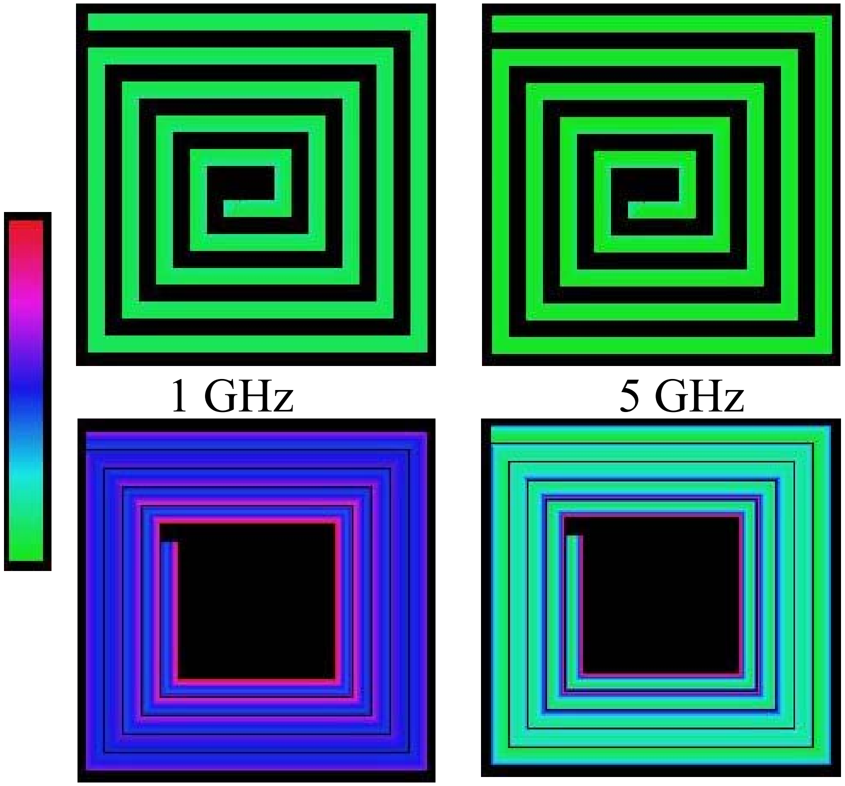
$$\mathrm{M}(l,d) = 2\times10^{-4}\times l\times\left[\ln\left(\sqrt{1+\left(\frac{l}{d}\right)^2}+\frac{l}{d}\right)-\sqrt{1+\left(\frac{d}{l}\right)^2}+\frac{d}{l}\right]$$



$$M \approx 2\times10^{-4}\times l\times\left(\frac{d}{l}-\ln(d)+\ln(2l)-1\right) \qquad d/l \ll 1$$

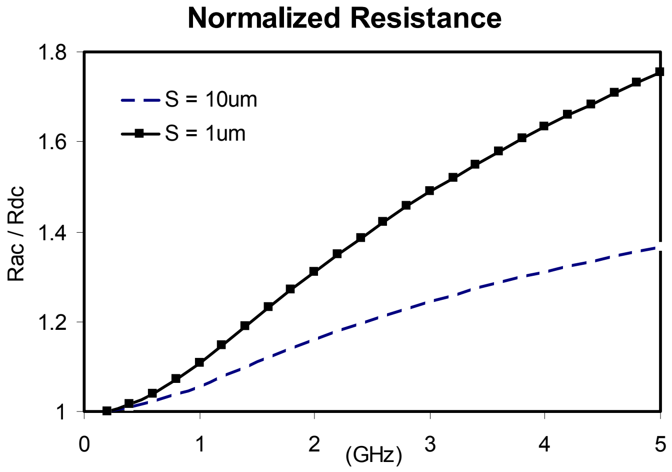
- Average ln(*d*) over the cross section (*Geometric Mean Distance*)
- Can perform this integration for many cases of interest
- Symmetry arguments can be used to derive mutual inductance between non-equal-length filaments
- For non-parallel geometries can use filamental approximations

Numerical Inductance Computation



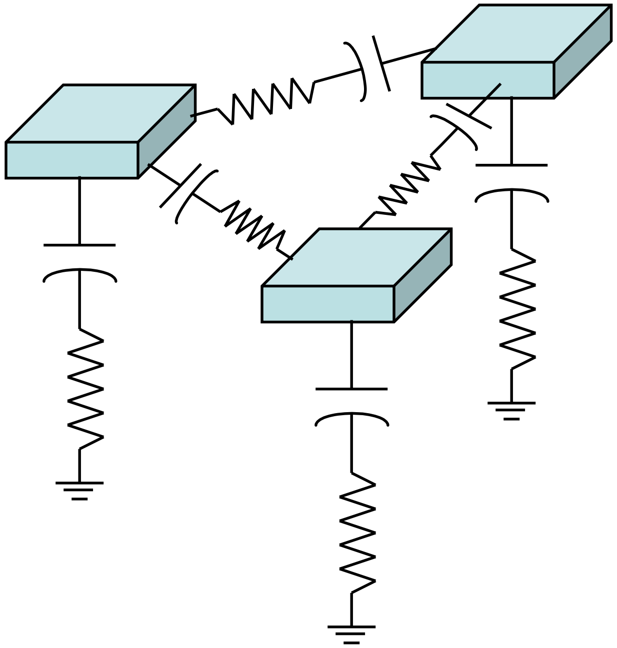
L=200 μ
W=10 μ
S = 10 μ
N = 5

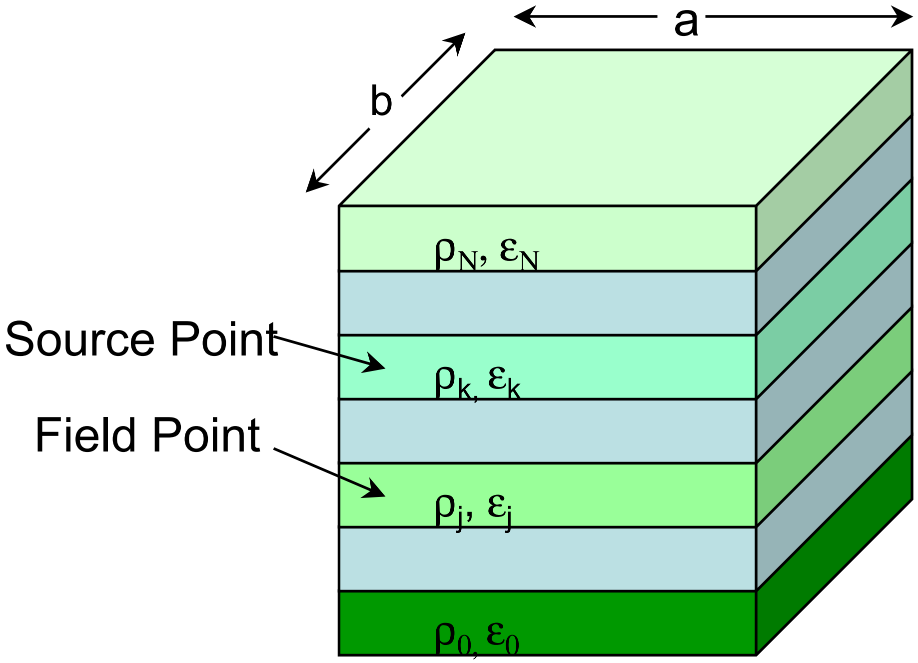
L=200 μ
W=10 μ
S = 1 μ
N = 5



Numerical simulation captures skin-effect, proximity effect, and substrate-induced eddy current losses

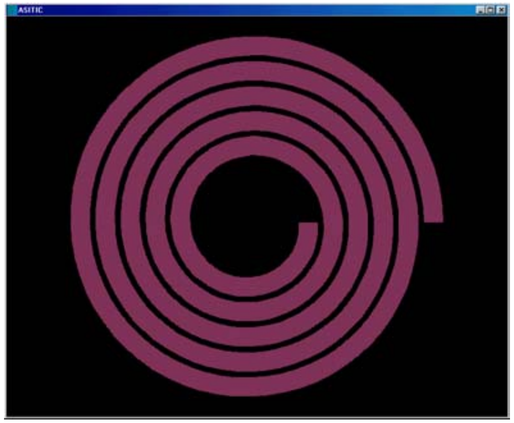
Capacitance Computation



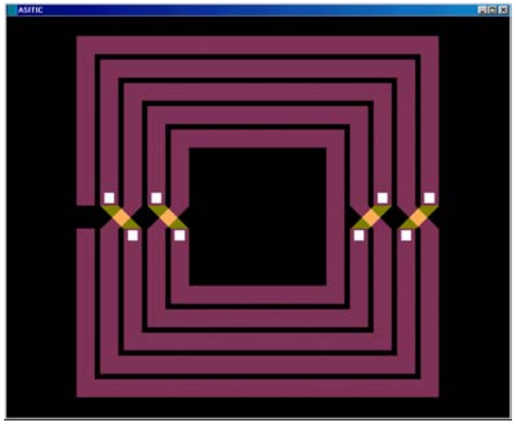


- Simple heuristic formulas don’t take substrate into account
- A multi-layer Green function approach gives capacitive coupling impedance between metal layers on top of lossy Si substrate
- This computation is useful for passive devices (capacitors, inductors, transformers) as well as interconnect modeling and substrate loss

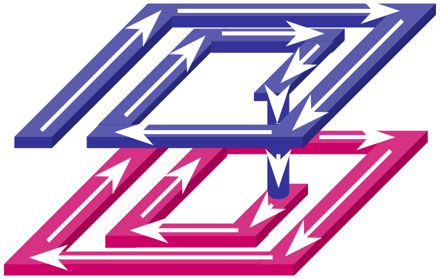
Inductor Layout Options



Circular Spiral Inductor



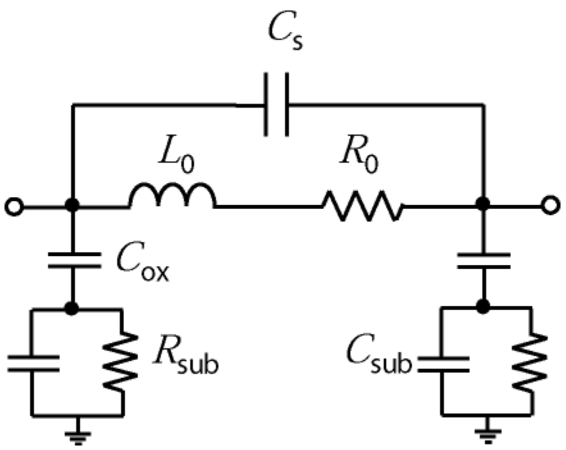
Symmetric Center-Tapped

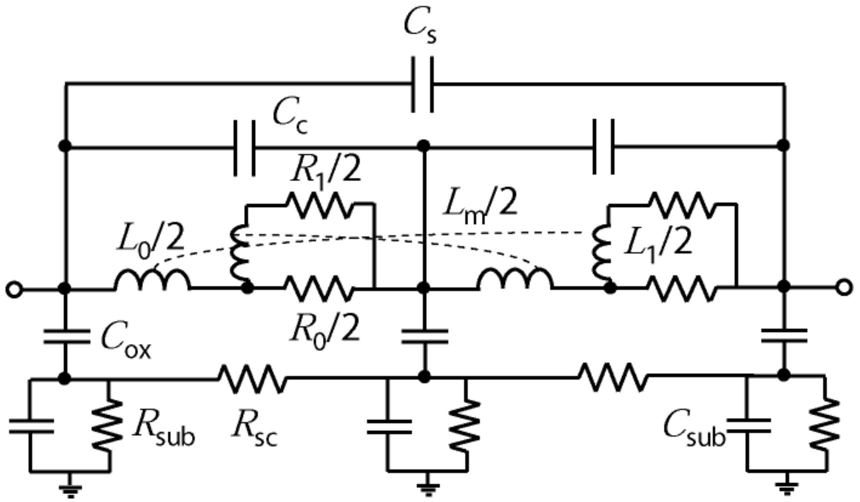


3D Series Connected

- Planar layout can be circular, square, polygon spirals, or “slabs”
- 3D layouts possible:
  - Shunt for low resistance
  - Series for high inductance
- Contact placement and shielding important options
- Diverse physical layout styles make analytical solutions difficult
- Foundry design kits often limit style and grounding options

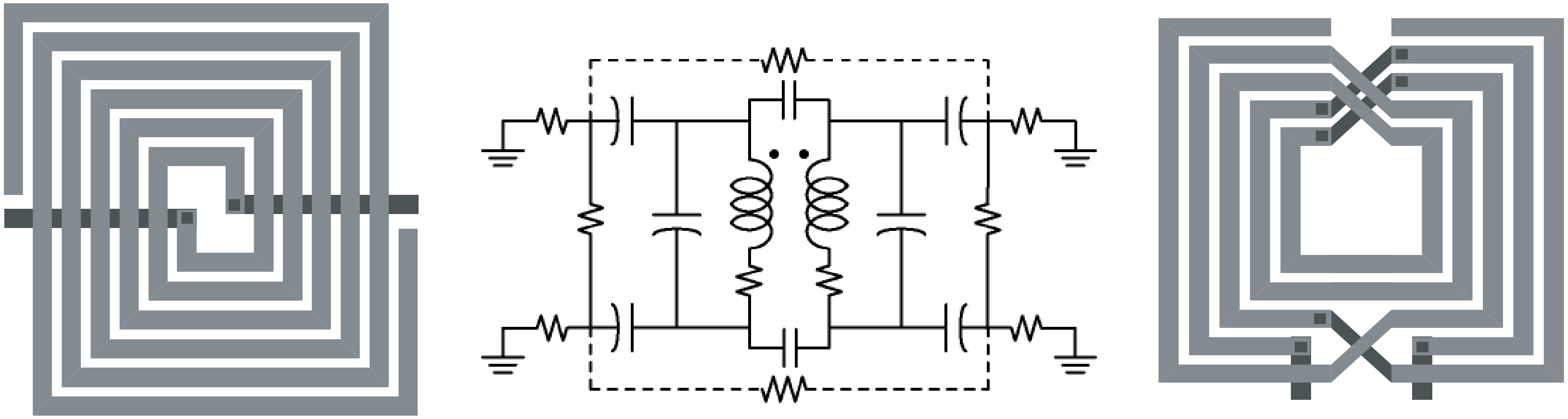
Inductor Compact Models





- Conventional Π model has physical roots
- Model works well over a narrow band
- Model cannot capture frequency-dependent skin-effect and proximity effects: $L(f)$ $R(f)$
- Physically derived 2-Π model can fit data over a wider frequency range

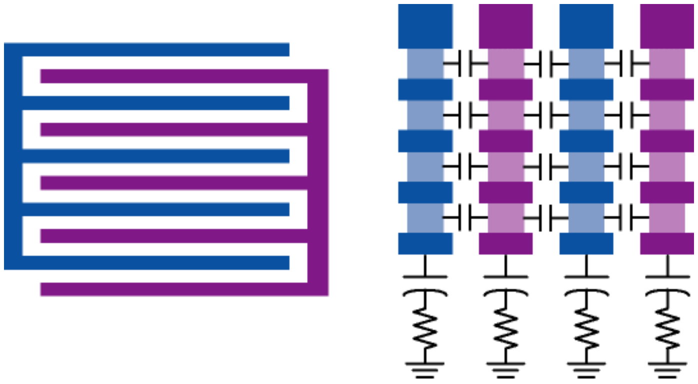
Transformer Layout and Models

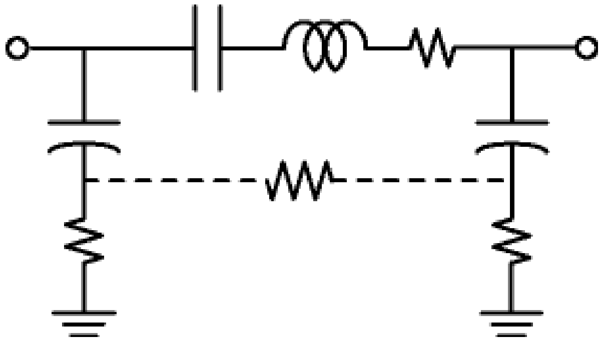


- Layout styles: square, polygon, circular, balanced, coupled lines
- To obtain turns ratio, can change width to alter inductance, skip turns on secondary, or put secondary turns in shunt (low loss)
- Modeling similar to inductor (self and mutual inductance)
- Phase balance between primary and secondary is important
  →Account for capacitive and substrate coupling between primary and secondary

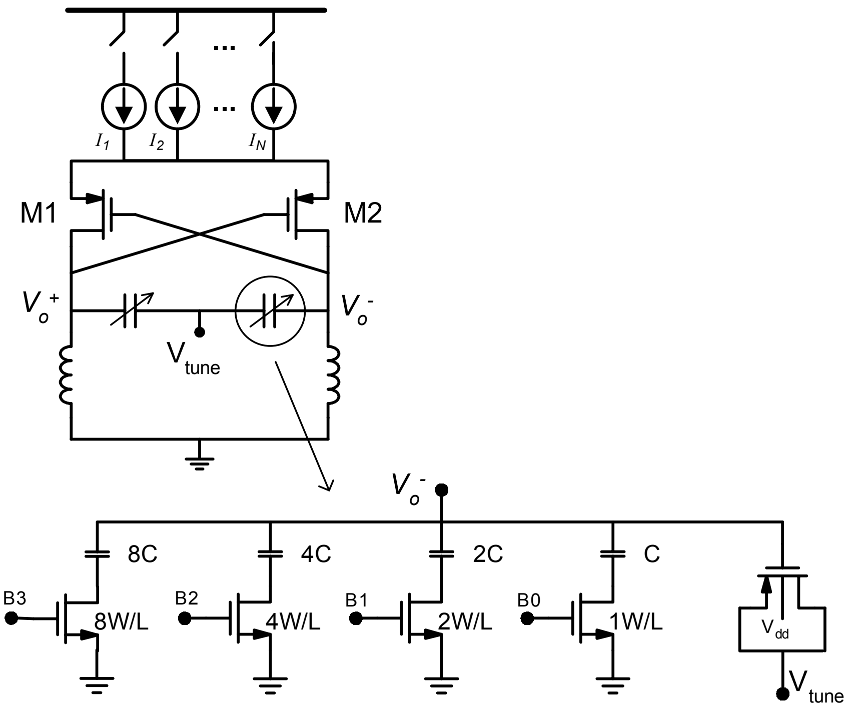
Capacitors and Varactors

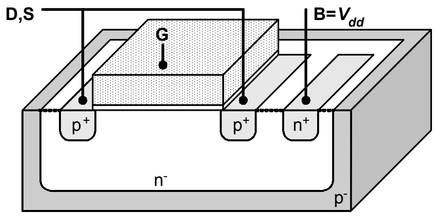
- MIM capacitors are used for high Q applications
- Thin oxide MIM caps are usually an extra option → finger caps are a good alternative
- Varactors are important tuning elements
- MOS varactors require accurate CV-curve modeling of FETs
- Loss mechanism and parasitics:
  - distributed plate resistance
  - dielectric loss tangent
  - substrate parasitics
  - self-resonance

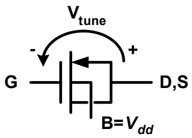


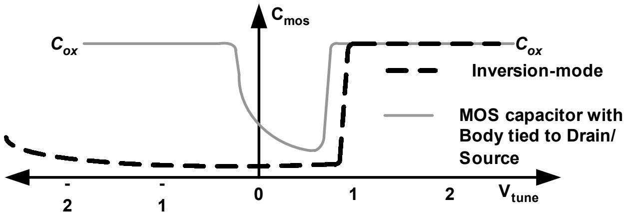


MOS Switches and Varactors





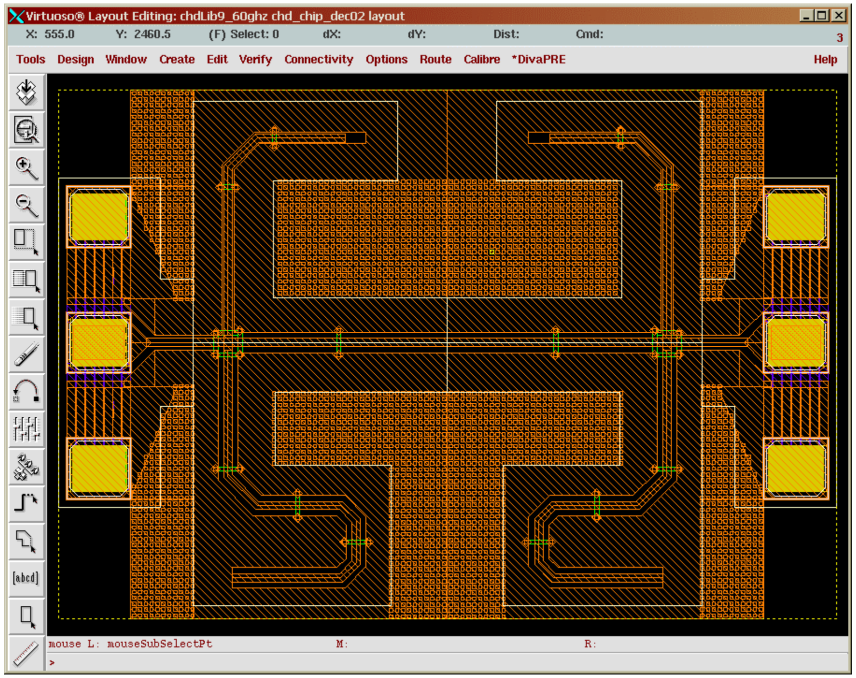


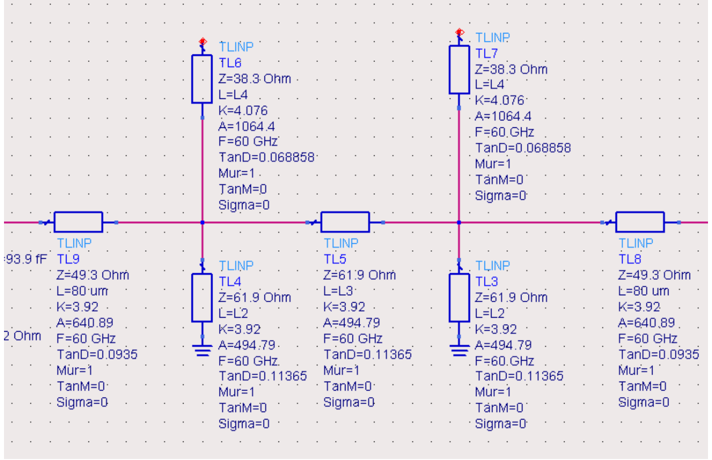


- MOS switches used as coarse tuning elements
- Need accurate models of MOS parasitics (limit on size of switch)
- MOS varactors or junction diode for fine control
- On-chip chokes or resistors to isolate tuning signal from tank

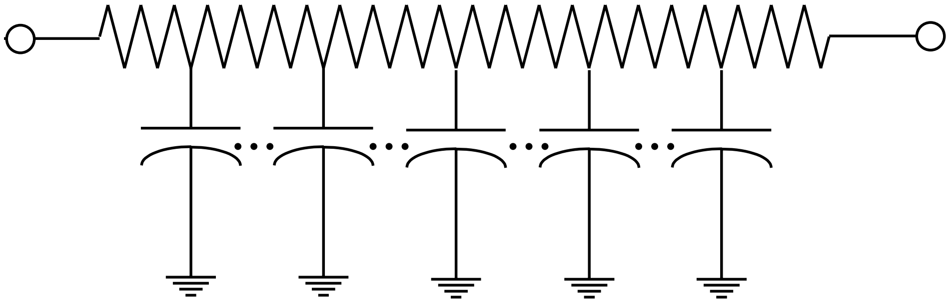
Transmission Lines

- Transmission lines key microwave building blocks
- Only a few parameters characterize line:
  - Characteristic impedance
  - Propagation constant (loss and phase velocity)
- Analysis easier (2D), model inherently scalable in length
- Simulation of loss difficult in SPICE-type simulation





IC Resistors at High Frequency

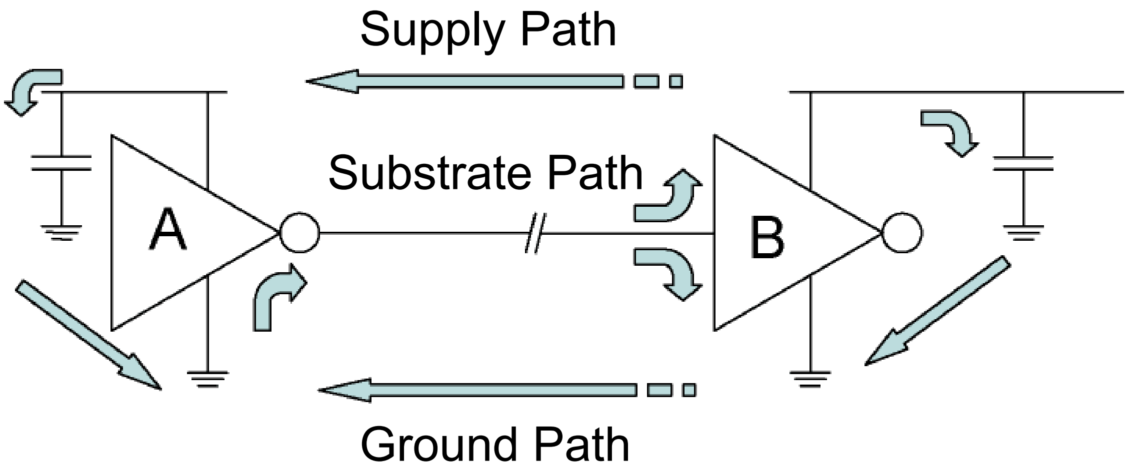


$$y_{11} = \sqrt{j\omega\, C_x / R}\, \coth \sqrt{j\omega\, R\, C_x}$$

$$y_{12} = -\sqrt{j\omega\, C_x / R}\, \operatorname{csch} \sqrt{j\omega\, R\, C_x}$$

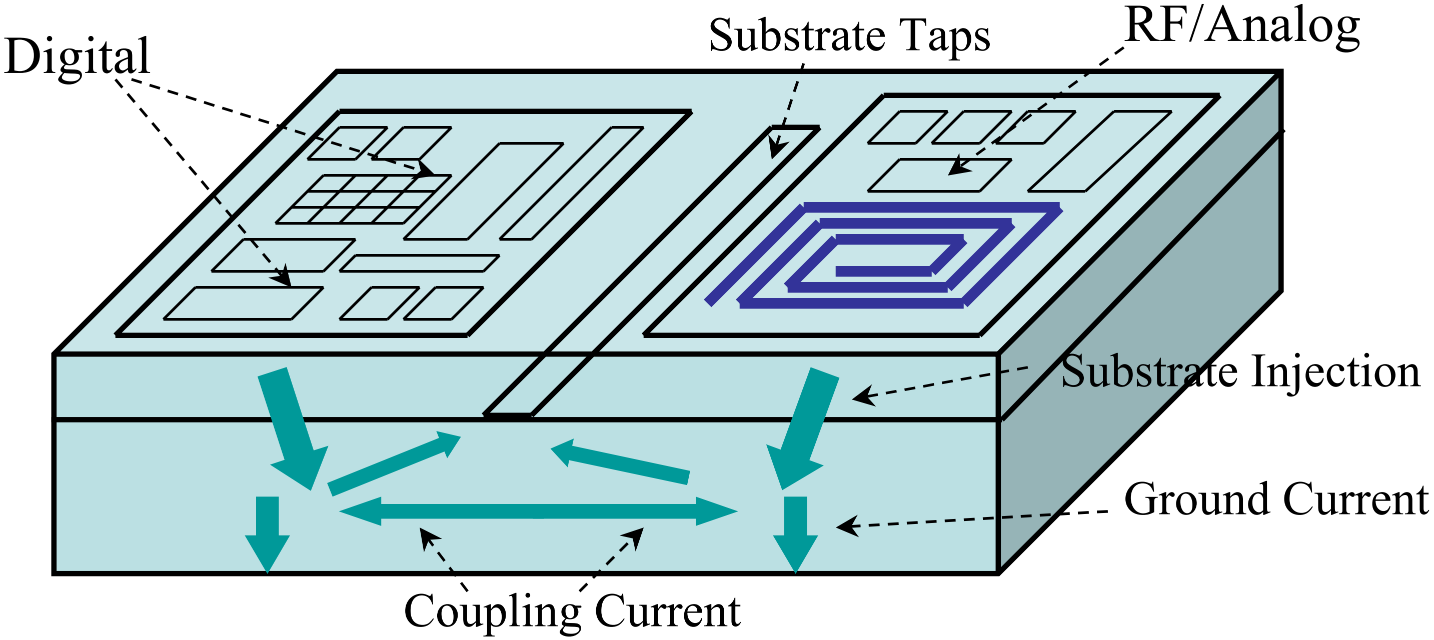
- High frequency resistors limited to thin-film or poly resistors with low capacitance
- Distributed capacitance important to model (RC line)
- MOS linear region devices make good variable resistors (should have accurate parasitics in FET model)
- Resistors less common due to RC pole limitations

IC Interconnect Extraction



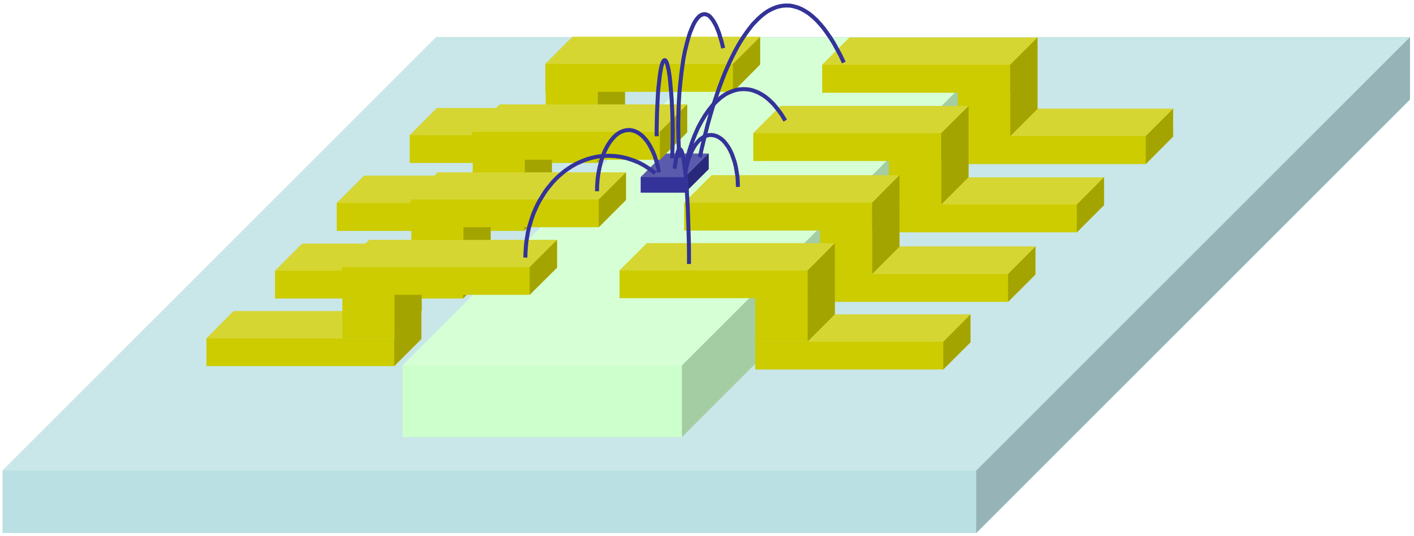
- Interconnect parasitics very important at RF and microwave frequencies
- Most parasitic interconnect extraction tools only compute capacitance and resistance
- Inductance extraction difficult due to the unknown and distributed “return current”
- Return current strong function of frequency: low frequency can even go off-chip!

Substrate Coupling



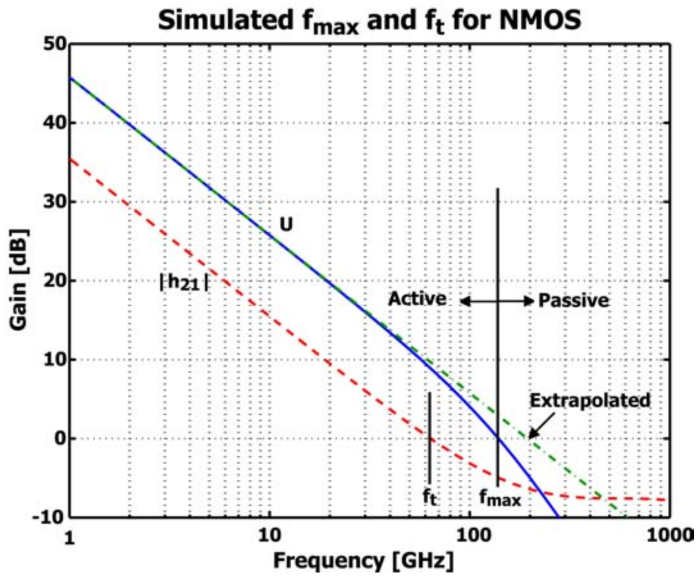
- Substrate coupling and loss important in mixed-signal ICs
- Digital circuits are pumping RF and microwave energy into substrate
- Quasi-static simulation is often performed, neglecting inductance effects
- Loss sets quality factor of passives and $f_{\max}$ of actives

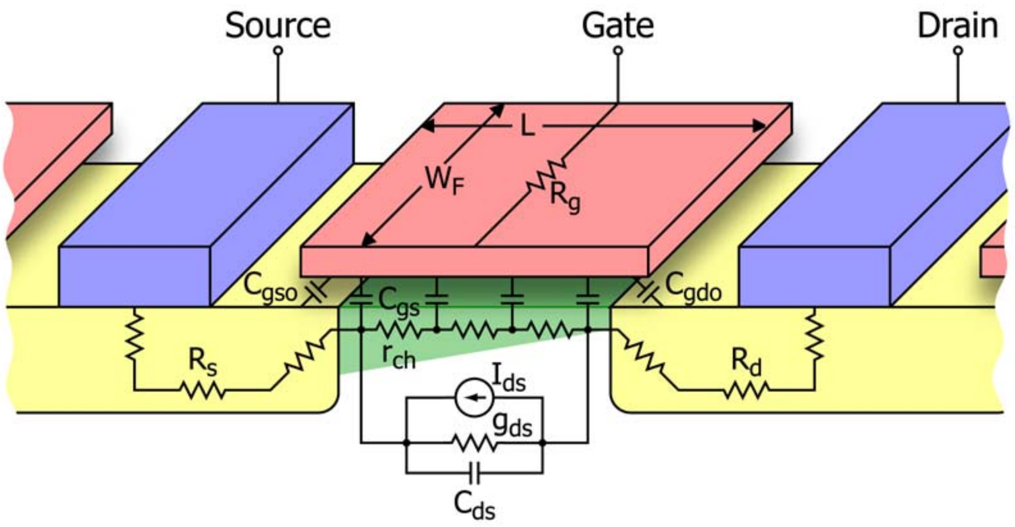
Package and Board Level Parasitics

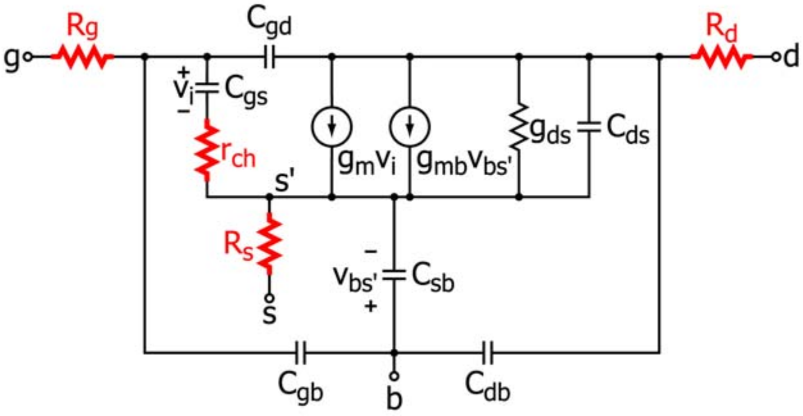


- Package parasitics important to model for RF signals going off-chip
- Package often limits isolation in circuits (accurate coupling)
- Co-simulation of chip + package + board difficult due to change of problem scale
- Higher frequency packages use flip-chip technology
- Many passive elements can be placed into package or board

Active Device Limitations







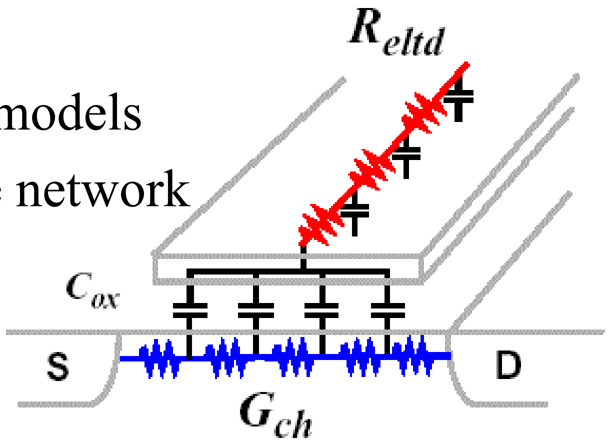
$$f_t \approx \frac{g_m}{2\pi C_{gg}}$$

$$f_{max} \approx \frac{f_t}{2\sqrt{R_g(g_m C_{gd}/C_{gg}) + (R_g + r_{ch} + R_s)g_{ds}}}$$

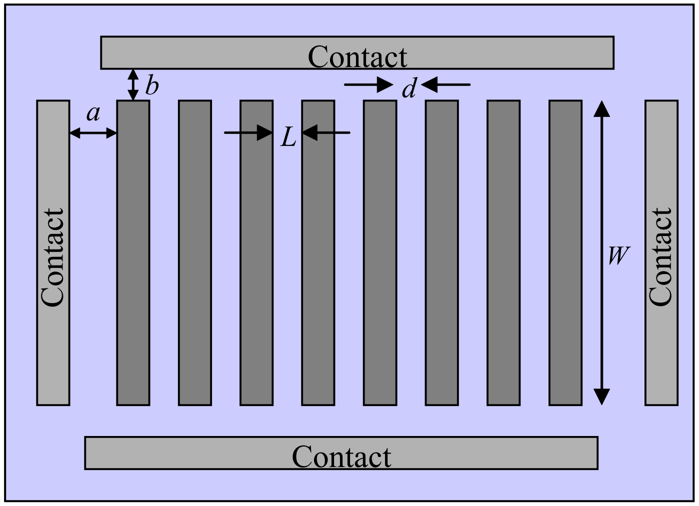
Test for passivity : $U(f) < 1,\ \forall f > f_{max}$

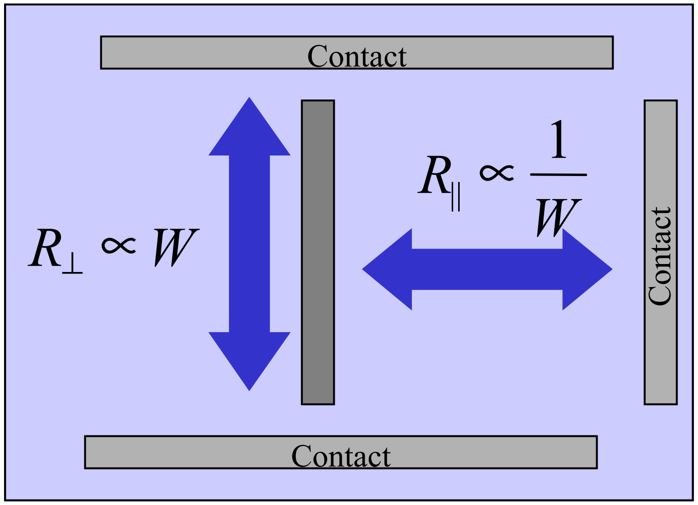
Empirical vs. Physical Models

- Empirical approach:
  - A curve fitting problem exercise to all available measurement data
  - The table lookup is the extreme case of empirical compact model
    - Expansive in data collection
    - Cannot be used to calculate statistical variation
- BSIM4 RF relevant features:
  - Gate resistance is included in the core model
  - Improved non-quasi-static AC model
  - New noise-partition and holistic thermal noise models
  - A flexible and configurable substrate resistance network
  - Layout-dependent parasitic model

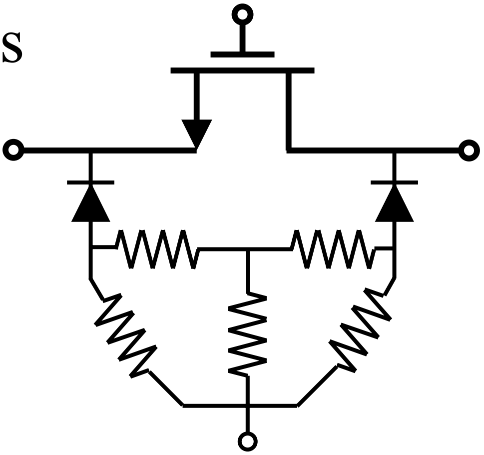


FET Substrate Resistance





- Substrate limits high frequency gain of amplifiers
- Resistance adds excess thermal noise to circuit
- Coupling causes unwanted feedback and digital noise leakage into sensitive analog circuitry
- Scaling is non-trivial due to complex layout
- Need scaling equations for substrate network



FET Distortion and Intermodulation

- Many RF and microwave circuits are non-linear or weakly non-linear
- Accurate distortion requires high accuracy in C-V and I-V curve *and* derivatives
- Device formulation should be as physical as possible to avoid numerical or unphysical distortion (symmetric MOSFET)

Conclusion

- Passive devices play critical role at RF and microwave frequencies
- Accurate parasitic extraction needed for both active and passive devices
- Measurements difficult to perform at these frequencies … need good analytical and numerical framework
- Accurate substrate extraction and scaling is a recurring theme

Acknowledgements

- Agilent Technologies
- STMicroelectronics
- DARPA
- SRC
- CMC