

Workshop on Compact Modeling
The 6th International Conference on Modeling and Simulation of Microsystems

(San Francisco, California, USA. February 25–27, 2003)

Overview

Compact Models (CMs) for circuit simulation have been at the heart of CAD tools for circuit design over the past decades, and are playing an ever increasingly important role in the very-deep-submicron/system-on-chip (VDSM/SOC) era. Although not highly “visible” to circuit designers and technology developers, a compact model plays the key role in accuracy and efficiency of the circuit simulator being used by designers as well as a bridge to the technology to which the design is to be fabricated. As the role CM is played in circuit simulation, CM developers play the similar role in bridging the circuit designers and technology developers. As the mainstream MOS technology is scaled into the VDSM regime, development of a truly physical and predictive compact model for circuit simulation that covers geometry, bias, temperature, DC, AC, RF, and noise characteristics becomes a major challenge. This demands that CM developers work more closely with the technology people and the design community.

Objective

Workshop on Compact Modeling (WCM) is one of the first of its kind in bringing people in the CM field together. The *objective* of WCM is to create a truly open forum for discussion among experts in the field as well as feedback from technology developers, circuit designers, and CAD tool vendors. The creation of WCM is a natural response of the CM community to the increasing demand in the field, and it will position itself as a premier forum for CM developers in information exchange and promotion of modeling diversity. Ultimately, the result of such a forum will benefit not only the model developers, but also as a service to the entire technology, modeling, and design communities.

Scope

The *scope* of WCM covers compact models for circuit simulation, which is centered at the mainstream MOS intrinsic models and extended to SOI, bipolar, interconnect, extrinsic, statistical, numerical-based, and reliability models. The key application is for circuit simulation and, hence, numerical simulation and pure theoretical and experimental work will not be within the scope of WCM.

Topics

The *topics* for WCM are largely categorized into the following areas:

- Bulk MOS intrinsic models
- SOI/double-gate MOS models
- Bipolar/HBT/SiGe models
- RF/noise/scalable capacitance/NQS models
- Statistical/predictive/process-based models
- Interconnection/passive device models

- Extrinsic/parasitic element models
- Reliability/hot carrier/tunneling models
- Atomic-level/quantum-mechanical compact models
- Numerical/TCAD/behavioral/table-based models
- Model parameter extraction and optimization
- Model–simulator interface and standardization

WCM-MSM2003

The second *Workshop on Compact Modeling (WCM-MSM2003)* will be held at *the 6th International Conference on Modeling and Simulation of Microsystems* in San Francisco, California, USA on February 25–27, 2003. It is planned to have an *Invited-Speaker Session*, an *Evening Forum* on “Model development – industry requirement dialogue”, contributed *Poster Session* as well as *Tutorial Session*. The topics are extended to the areas listed above, within the main theme – *compact models for circuit simulation*.

Invited Speakers

Invited speakers as well as panelists for the WCM Forum from all over the world (10 countries) are listed below (speakers underlined):

- Narain Arora, Cadence Design Systems, USA
- Peter Bendix, LSI Logic, USA
- Mansun Chan, Hong Kong University of Science and Technology, Hong Kong
- Robert Dutton, Stanford University, USA
- Jerry Fossum, University of Florida, USA
- Carlos Galup-Montoro and Marcio Schneider, Universidade Federal de Santa Catarina, Brazil
- Gennady Goldenblat and Xin Gu, Pennsylvania State University, USA
- Thomas Gneiting, Advanced Modeling Solutions, Germany
- Hermann Gummel, Averill Bell, and Kumud Singhal, Agere Systems, USA
- Chenming Hu*, Ali Niknejad, and Xuemei Xi, University of California at Berkeley, USA; (*also with Taiwan Semiconductor Manufacturing Company)
- Dirk Klaassen and Jeroen Paasschens, Philips Research Laboratories, The Netherlands
- Shiuh-Wuu Lee, Intel, USA
- Colin McAndrew*, Wladyslaw Grabinski**, and Laurent Lemaitre**, Motorola, *USA, **Switzerland
- Marek Mierzwiński, Tiburon Design Automation, USA
- Mitiko Miura-Mattausch, Hiroshima University, Japan
- Andrea Pacelli, State University of New York at Stony Brook, USA
- Mahesh Patil, Indian Institute of Technology – Bombay, India
- Greg Rollins, Mentor Graphics, USA
- Michael Schroter, University of Technology Dresden, Germany
- Hyungcheol Shin, Korea Advanced Institute of Science and Technology, Korea
- Bogdan Tudor, Synopsys, USA
- Eric Vittoz, Christian Enz, and Francois Krummenacher*, Swiss Center for Electronics and Microtechnology, *EPFL, Switzerland
- Simon Wong, Niranjana Talwalkar, and Patrick Yue, Stanford University, USA
- Cary Yang and Sang-Pil Sim, Santa Clara University, USA
- Xing Zhou, Nanyang Technological University, Singapore

Workshop Program

There are 22 invited papers, which are categorized in the following topic areas (speakers underlined):

Compact modeling and design:

- Implications of Gate Tunneling and Quantum Effects in the Gate-Channel Stack
Robert Dutton and Chang-Hoon Choi, Stanford University, USA
- A Basic Property of MOS Transistors and its Circuit Implications
Eric Vittoz, Christian Enz, and Francois Kruppenacher, Swiss Center for Electronics and Microtechnology, *EPFL, Switzerland*

Bulk MOS intrinsic models:

- USIM Design Considerations
Averill Bell, Kumud Singhal, and Hermann Gummel, Agere Systems, USA
- Theory, Development and Applications of the Advanced Compact MOSFET (ACM) Model
Carlos Galup-Montoro, M. C. Schneider, A. I. A. Cunha, and O. C. Gouveia-Filho**, Universidade Federal de Santa Catarina, *Escola Polit cnica/UFBA - Salvador, **CIEL/UFPR - Curitiba, Brazil*
- HiSIM: Accurate Charge Modeling Important for RF Era
Mitiko Miura-Mattausch, D. Navarro, H. Ueno, H. J. Mattausch, K. Morikawa, S. Itoh*, A. Kobayashi*, and H. Masuda*, Hiroshima University, *Semiconductor Technology Academic Research Center, Japan*
- An Advanced Surface-Potential-Plus MOSFET Model
Jin He, Xuemei Xi, Mansun Chan, Ali Niknejad, and Chenming Hu, University of California at Berkeley, USA, *Hong Kong University of Science and Technology, Hong Kong*
- A Technology-Based Compact Model for Predictive Deep-Submicron MOSFET Modeling and Characterization
Xing Zhou, Siau Ben Chiah, and Khee Yong Lim, Nanyang Technological University, *Chartered Semiconductor Manufacturing, Singapore*

SOI/double-gate MOS models:

- A Framework for Generic Physics Based Double-Gate MOSFET Modeling
Mansun Chan, Yuan Taur, Chung Hsun Lin**, Jin He**, Ali Niknejad**, and Chenming Hu**, Hong Kong University of Science and Technology, Hong Kong, *University of California at San Diego, **University of California at Berkeley, USA*
- A Physics-Based Compact Model for Nano-Scale DG and FD/SOI MOSFETs
Jerry Fossum, Lixin Ge, and Meng-Hsueh Chiang, University of Florida, USA

Bipolar models:

- BJT Modeling with VBIC, Basics and V1.3 Updates
Colin McAndrew, T. Bettinger, L. Lemaitre, and M. Tutt, Motorola, USA
- Compact Bipolar Transistor Modeling – Issues and Possible Solutions
Michael Schroter, University of Technology Dresden, Germany

RF/noise models:

- Noise Modelling with MOS Model 11 for RF-CMOS Applications
A. J. Scholten, L. F. Tiemeijer, R. van Langevelde, R. J. Havens, A. T. A. Zegers-van Duijnhoven, V. C. Venezia, and Dirk Klaassen, Philips Research Laboratories, The Netherlands
- Physical Modeling of Substrate Resistance in RF MOSFETs
Jeonghu Han, Minkyu Je, and Hyungcheol Shin, Korea Advanced Institute of Science and Technology, Korea

Interconnection/passive device models:

- Characterization and Modeling of Copper Interconnects for VLSI Design
Narain Arora, Cadence Design Systems, USA
- Compact Modeling for RF and Microwave Integrated Circuits
Ali Niknejad, Mansun Chan, Chenming Hu, Xuemei Xi, Jin He, Pin Su, Yu Cao, Hui Wan, Mohan Dunga, Chinh Doan, Sohrab Emami, and Chung-Hsun Lin, University of California at Berkeley, USA, *Hong Kong University of Science and Technology, Hong Kong*
- Vector-Potential Equivalent Circuit for Efficient Modeling of Interconnect Inductance
Andrea Pacelli, State University of New York at Stony Brook, USA
- Unified RLC Model for On-chip Interconnects
Sang-Pil Sim and Cary Yang, Santa Clara University, USA
- Compact Modeling of High Frequency Phenomena for On-chip Spiral Inductors
Niranjan Talwalkar, Patrick Yue, and Simon Wong, Stanford University, USA

Extrinsic/parasitic element models:

- Surface-Potential-Based Extrinsic MOSFET Model
Xin Gu, Gennady Gildenblat, Glen Workman, and Shye Shapira**, Pennsylvania State University, *Motorola, **Agere Systems, USA*

Model parameter extraction and optimization:

- A Unified Environment for the Modeling of Ultra Deep Submicron MOS Transistors
Thomas Gneiting, Advanced Modeling Solutions, Germany

Model-simulator interface and standardization:

- Standardization of Compact Device Modeling in High Level Description Language
Laurent Lemaitre, Colin McAndrew, and Wladyslaw Grabinski, Motorola, Switzerland, Motorola, *USA*
- Changing the Paradigm for Compact Model Integration in Circuit Simulators Using Verilog-A
Marek Mierzwinski and Robert Dutton, Tiburon Design Automation, *Stanford University, USA*

Forum and Evening Panel

Forum on *Model development – industry requirement dialogue*

Continued from the first successful Workshop on Compact Modeling (WCM-MSM2002) in San Juan, April 2002, this second Workshop (WCM-MSM2003) encompasses a broader range of topics, from intrinsic bulk MOS to bipolar and SOI/double-gate, as well as RF/interconnect/extrinsic/passive-element models, covering important issues on design considerations, parameter extraction, and simulator interface. To complement the invited technical presentations by experts from both academia and industry, a **Forum** on “model development – industry requirement dialogue” is organized, in which we are going to hear experts' views on the general topic:

The Role of Compact Model in the Fab and Fabless Business

An **Evening Panel** discussion will be followed by a panel of experts from major representative academic (Stanford, UC Berkeley), chip industry (Intel, LSI Logic, Philips), and EDA vendors (Cadence, Mentor Graphics, Synopsys). The Panel will discuss important topics that are in line with the theme of this Workshop:

- Key to bridging compact-model development to designers and simulator vendors
- Current needs and priorities in compact-model development
- Intrinsic model with respect to extrinsic, parasitic, passive, and interconnect models
- Model interface to simulators, extractors, and users

We are expected to hear “spirited difference of opinions” on how to define, develop, and deploy a good compact model that is central to the mutual benefit of the entire chip design, modeling, and manufacturing communities.

Moderator: *Narain Arora*, Cadence Design Systems, USA

Panelists:

- *Peter Bendix*, LSI Logic, USA
- *Robert Dutton*, Stanford University, USA
- *Dirk Klaassen*, Philips Research Laboratories, The Netherlands
- *Shiuh-Wuu Lee*, Intel, USA
- *Ali Niknejad*, University of California at Berkeley, USA
- *Greg Rollins*, Mentor Graphics, USA
- *Bogdan Tudor*, Synopsys, USA

Poster Session

Poster presentations in the scope of “compact models for circuit simulation” are solicited. A 5-minute **oral briefing** for each poster paper is planned before the poster presentation session.

Contributed poster papers are listed below (presenters underlined):

- A Physics-Based Analytical Surface Potential and Capacitance Model of MOSFET's Operation from the Accumulation to Depletion Region
Jin He, Xuemei Xi, Mansun Chan, and Chenming Hu, University of California at Berkeley, USA
- Modeling of Direct Tunneling Current in Multi-Layer Gate Stacks
Mohan V. Dunga, Xuemei Xi, Jin He, I. Polishchuk, Qiang Lu, Mansun Chan, Ali Niknejad, and Chenming Hu, University of California at Berkeley, USA
- Substrate Current in Surface-Potential-Based Compact MOSFET Models
X. Gu and G. Gildenblat, Pennsylvania State University, USA
- Application of Genetic Algorithm to Compact MOSFET Model Parameter Extraction
X. Cai, H. Wang, X. Gu, and G. Gildenblat, Pennsylvania State University, USA

- A Surface-Potential-Based Compact Model of NMOSFET Gate Tunneling Current
X. Gu, H. Wang, G. Gildenblat, G. Workman*, S. Veeraraghavan*, S. Shapira**, and K. Stiles**, *Pennsylvania State University*, **Motorola*, ***Agere Systems, USA*
- Gate Current Partitioning Scheme for Circuit Simulation
Q. Ngo, D. Navarro*, T. Mizoguchi*, S. Hosakawa*, H. Ueno*, M. Miura-Mattausch*, and C. Y. Yang, *Santa Clara University, USA*, **Hirohsima, Japan*
- Double-Gate CMOS Evaluation for 45nm Technology Node
Meng-Hsueh Chiang, Judy X. An, Zoran Krivokapic, and Bin Yu, *Advanced Micro Devices, USA*
- Primary Consideration on Compact Modeling of DG MOSFETs with Four-Terminal Operation Mode
T. Nakagawa, T. Sekigawa, T. Tsutsumi, E. Suzuki, and H. Koike, *National Institute of Advanced Industrial Science and Technology, Japan*
- A Compact Model Methodology for Device Design Uncertainty
Richard Williams, Josef Watts, Myung-hee Na, and Kerry Bernstein, *IBM, USA*
- Unified Length-/Width-Dependent Threshold Voltage Model with Reverse Short-Channel and Inverse Narrow-Width Effects
Siau Ben Chiah, Xing Zhou, and Khee Yong Lim*, *Nanyang Technological University*, **Chartered Semiconductor Manufacturing, Singapore*
- Unified Length-/Width-Dependent Drain Current Model for Deep-Submicron MOSFETs
Siau Ben Chiah, Xing Zhou, and Khee Yong Lim*, *Nanyang Technological University*, **Chartered Semiconductor Manufacturing, Singapore*
- An Interactive Website as a Tool for CAD of Power Circuits
Bartłomiej Świercz, Łukasz Starzak, Mariusz Zubert, and Andrzej Napieralski, *Technical University of Łódź, Poland*
- Multidimensional Model-Based Parameter Estimation Method for Compact Modeling of High-Speed Interconnects FET
Tom Dhaene, *University of Antwerp, Belgium*
- An Automatic Macro Program Developed for Characterization, Parameter Extraction and Statistic Analysis of Spiral Inductors
D. Y. Chiu, G. W. Huang, and K. M. Chen, *National Nano Device Laboratories, Taiwan*

Tutorial Session

Two tutorials are offered as listed below (speakers underlined):

- Modelling of Si and SiGe Bipolar Transistors with the Compact Model Mextram 504
Jeroen Paasschens and R. van der Toorn, *Philips Research Laboratories, The Netherlands*
- The Look-Up Table Approach and its Implementation in a Circuit Simulator
Mahesh Patil, *Indian Institute of Technology - Bombay, India*

Call for Participation

Workshop on Compact Modeling is initiated as a forum for model developers as well as interaction with the technology/design communities. It is mainly in the form of invited presentations for the specific topics in the compact modeling area. For WCM-MSM2003, the topics are extended to a larger scope, and invitations will be extended to experts in the related topic areas. Please visit the following website for updates:

WCM-MSM2003

<http://www.ntu.edu.sg/home/exzhou/WCM/WCM2003/wcm03.htm>
For WCM-related enquiries, please contact *Dr. Xing Zhou* (exzhou@ntu.edu.sg). For general MSM-related enquiries, please contact *Ms. Sarah Wenning* (wenning@cr.org).

WCM-MSM2003, being the second one, will prove to be interesting and useful for people in a broad spectrum of fields: compact model developers, process engineers, device physicists, and circuit designers, in a variety of disciplines: universities, research institutions, chip manufacturers, wafer fabs, fabless companies, consulting firms, parameter-extraction tool and circuit-simulator vendors.

All are invited to participate in this exciting event!

WCM websites:

<http://www.ntu.edu.sg/home/exzhou/WCM/>
<http://www.cr.org/MSM2003/WCM.html>
<http://www.nanotech2003.com/WCM2003.html>

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(San Francisco, California, USA. February 25–27, 2003)

PROGRAM

(*Note: For any changes/updates, please refer to website: <http://www.nanotech2003.com/2003program.html>*)

DAY 1

WCM-1: Tuesday, Feb. 25, 10:25 – 12:00

Session chair: *Xing Zhou, Nanyang Technological University, Singapore*

WCM Opening Remark: *Xing Zhou, Nanyang Technological University, SG*

- Implications of Gate Tunneling and Quantum Effects in the Gate-Channel Stack
Robert Dutton, Stanford University, US
- A Basic Property of MOS Transistors and its Circuit Implications
Eric Vittoz, Swiss Center for Electronics and Microtechnology, CH
- USIM Design Considerations
Averill Bell, Agere Systems, US

WCM-2: Tuesday, Feb. 25, 14:00 – 16:00

Session chair: *Robert Dutton, Stanford University, USA*

- Theory, Development and Applications of the Advanced Compact MOSFET (ACM) Model
Carlos Galup-Montoro, Universidade Federal de Santa Catarina, BR
- HiSIM: Accurate Charge Modeling Important for RF Era
Mitiko Miura-Mattausch, Hiroshima University, JP
- An Advanced Surface-Potential-Plus MOSFET Model
Xuemei Xi, University of California at Berkeley, US
- A Technology-Based Compact Model for Predictive Deep-Submicron MOSFET Modeling and Characterization
Xing Zhou, Nanyang Technological University, SG

Forum: Tuesday, Feb. 25, 16:30 – 17:50

Model development - industry requirement dialogue

Session chair: *Colin McAndrew, Motorola, USA*

Topic: *The Role of Compact Model in the Fab and Fabless Business*

Evening Panel: Tuesday, Feb. 25, 19:30 – 21:00

Moderator: *Narain Arora, Cadence Design Systems, USA*

Panelists: *Peter Bendix, LSI Logic, USA*

Robert Dutton, Stanford University, USA

Dirk Klaassen, Philips Research Laboratories, The Netherlands

Shiuh-Wuu Lee, Intel, USA

Ali Niknejad, University of California at Berkeley, USA

Greg Rollins, Mentor Graphics, USA

Bogdan Tudor, Synopsys, USA

DAY 2

WCM-3: Wednesday, Feb. 26, 8:30 – 10:00

Session chair: *Narain Arora, Cadence Design Systems, USA*

- A Framework for Generic Physics Based Double-Gate MOSFET Modeling
Mansun Chan, Hong Kong University of Science and Technology, HK
- A Physics-Based Compact Model for Nano-Scale DG and FD/SOI MOSFETs
Jerry Fossum, University of Florida, US
- BJT Modeling with VBIC, Basics and V1.3 Updates
Colin McAndrew, Motorola, US

WCM-4: Wednesday, Feb. 26, 10:30 – 12:00

Session chair: *Jerry Fossum, University of Florida, USA*

- Compact Bipolar Transistor Modeling – Issues and Possible Solutions
Michael Schroter, University of Technology Dresden, DE
- Noise Modelling with MOS Model 11 for RF-CMOS Applications
Dirk Klaassen, Philips Research Laboratories, NE
- Physical Modeling of Substrate Resistance in RF MOSFETs
Hyungcheol Shin, Korea Advanced Institute of Science and Technology, KR

WCM-5: Wednesday, Feb. 26, 14:00 – 15:30

Session chair: *Cary Yang, Santa Clara University, USA*

- Characterization and Modeling of Copper Interconnects for VLSI Design
Narain Arora, Cadence Design Systems, US
- Compact Modeling for RF and Microwave Integrated Circuits
Ali Niknejad, University of California at Berkeley, US
- Vector-Potential Equivalent Circuit for Efficient Modeling of Interconnect Inductance
Andrea Pacelli, State University of New York at Stony Brook, US

Poster Oral Briefing: Wednesday, Feb. 26, 16:00 – 17:15

Session chair: *Mahesh Patil, Indian Institute of Technology - Bombay, India*

- A Physics-Based Analytical Surface Potential and Capacitance Model of MOSFET's Operation from the Accumulation to Depletion Region
Jin He, University of California at Berkeley, US
- Modeling of Direct Tunneling Current in Multi-Layer Gate Stacks
Mohan V. Dunga, University of California at Berkeley, US
- Substrate Current in Surface-Potential-Based Compact MOSFET Models
X. Gu, Pennsylvania State University, US
- Application of Genetic Algorithm to Compact MOSFET Model Parameter Extraction
X. Gu, Pennsylvania State University, US
- A Surface-Potential-Based Compact Model of NMOSFET Gate Tunneling Current
X. Gu, Pennsylvania State University, US
- Gate Current Partitioning Scheme for Circuit Simulation
Q. Ngo, Santa Clara University, US
- Double-Gate CMOS Evaluation for 45nm Technology Node
Judy An, Advanced Micro Devices, US
- Primary Consideration on Compact Modeling of DG MOSFETs with Four-Terminal Operation Mode

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- *T. Nakagawa, National Institute of Advanced Industrial Science and Technology, JP*
- A Compact Model Methodology for Device Design Uncertainty
Richard Williams, IBM, US
- Unified Length-/Width-Dependent Threshold Voltage Model with Reverse Short-Channel and Inverse Narrow-Width Effects
Siau Ben Chiah, Nanyang Technological University, SG
- Unified Length-/Width-Dependent Drain Current Model for Deep-Submicron MOSFETs
Siau Ben Chiah, Nanyang Technological University, SG
- An Interactive Website as a Tool for CAD of Power Circuits
Andrzej Napieralski, Technical University of Łódź, PL
- Multidimensional Model-Based Parameter Estimation Method for Compact Modeling of High-Speed Interconnects FET
Tom Dhaene, University of Antwerp, BE
- An Automatic Macro Program Developed for Characterization, Parameter Extraction and Statistic Analysis of Spiral Inductors
D. Y. Chiu, National Nano Device Laboratories, TW

Poster Session: Wednesday, Feb. 26, 18:00 – 19:30

DAY 3

WCM-6: Thursday, Feb. 27, 8:30 – 10:00

Session chair: *Mansun Chan, Hong Kong University of Science and Technology, HK*

- Unified RLC Model for On-chip Interconnects
Sang-Pil Sim, Santa Clara University, US
- Compact Modeling of High Frequency Phenomena for On-chip Spiral Inductors
Simon Wong, Stanford University, US
- Surface-Potential-Based Extrinsic MOSFET Model
Xin Gu, Pennsylvania State University, US

WCM-7: Thursday, Feb. 27, 10:30 – 12:00

Session chair: *Dirk Klaassen, Philips Research Laboratories, The Netherlands*

- A Unified Environment for the Modeling of Ultra Deep Submicron MOS Transistors
Thomas Gneiting, Advanced Modeling Solutions, DE
- Standardization of Compact Device Modeling in High Level Description Language
Laurent Lemaitre, Motorola, CH
- Changing the Paradigm for Compact Model Integration in Circuit Simulators Using Verilog-A
Marek Mierzwinski, Tiburon Design Automation, US

Tutorials: Thursday, Feb. 27, 14:00 – 16:30

- Modelling of Si and SiGe Bipolar Transistors with the Compact Model Mextram 504
Jeroen Paasschens, Philips Research Laboratories, NE
- The Look-Up Table Approach and its Implementation in a Circuit Simulator
Mahesh Patil, Indian Institute of Technology - Bombay, IN