

# Submicron Circuit Design with BSIM3 or BSIM4

**Mansun Chan**

**E-mail: [mchan@eecs.berkeley.edu](mailto:mchan@eecs.berkeley.edu)**

**Department of Electrical Engineering & Computer Science  
University of California at Berkeley**

**Department of Electrical & Electronic Engineering  
Hong Kong University of Science & Technology**



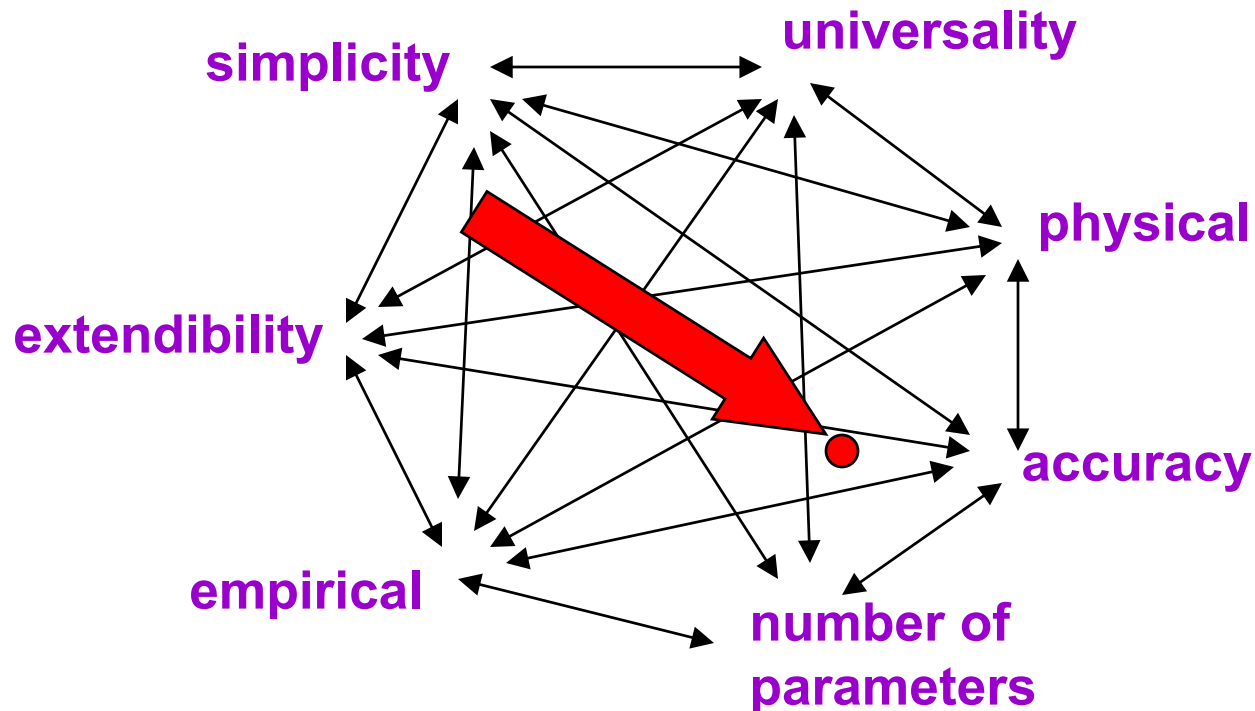
# Outline

- Modeling Tradeoffs and BSIM approaches
- The Meyer's model and its deficiency
- Formulation of the basic BSIM model
- Simplified BSIM3 model for hand calculation
- Additional Features in BSIM4
- Summary



# Modeling Tradeoff

- Ultimate goal of model: **Accurate and Simple**
- Modeling tradeoff polygon



# Various Modeling Approaches

## ■ Charge based model

- terminal charges are associated to terminal voltages
- most compatible with the conventional design methodology
- simple, flexible but maybe more empirical

## ■ Surface potential based model

- more physically and ensure smooth transition between operation regions
- usually more complex and less flexible

## ■ Conductance based model

- good for circuit design with simple and predictable behavior
- need to improve on accuracy
- still a bit primitive for predictive purpose



# Positioning of BSIM Models

## ■ Physical based

- basic derivation is from physical device parameters
- important for predictive property

## ■ Traditional design compatibility

- most popular model among circuit designer is still the level 1 (basic Meyer) model
- BSIM was first intended to be compatible with the level 1 model

## ■ Flexibility to fit most existing technology

- modular approach for flexible addition of new and complex technology modules quickly
- capability to fit a wide range of technologies (good or bad)
- by using some empirical fitting and tuning parameters



# Some facts in BSIM development

- Starts out as a simple physical model with a small number of parameters
- Closely follow process development with lots of advanced features such as
  - Super steep retrograde well
  - Pocket implant
  - Gate current model
  - GIDL/GISL
- Allow early adoptions of new process modules
- Under the guideline of industrial partners in the direction of development



# Preliminary solutions to Charge model

■ A new capacitor model (BSIM4 CapMod=3) has been formulated with the following features

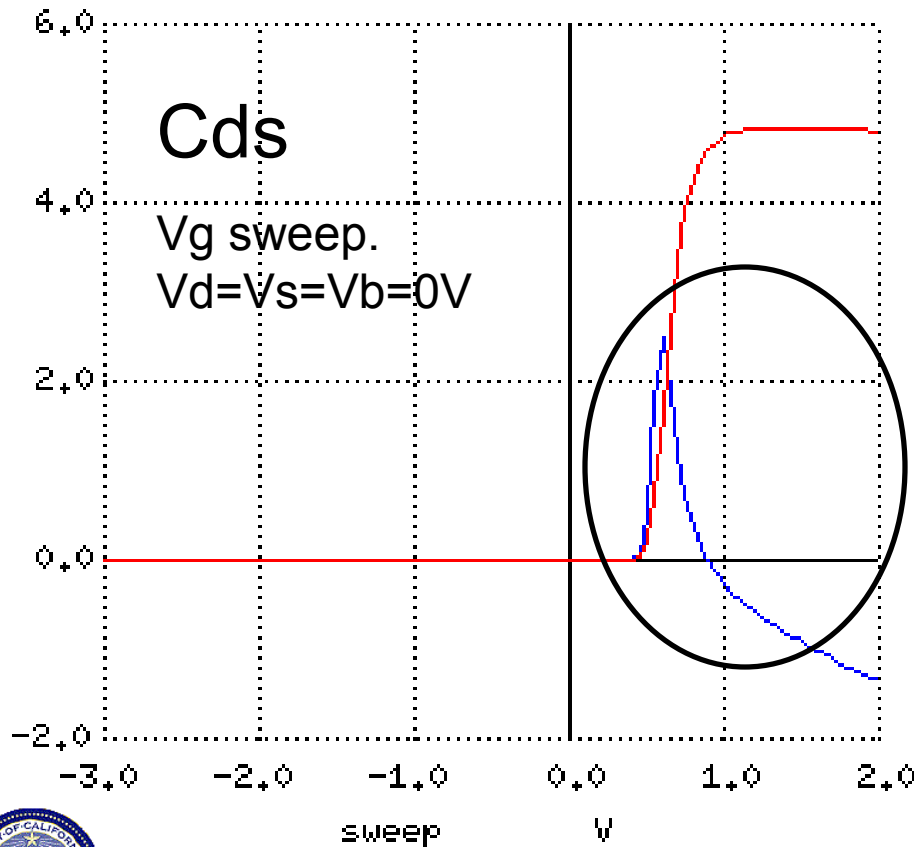
- No asymmetry or negative resistance problem
- About 1,200 lines of code
- About 50% slower than CapMod=2) for single transistor voltage sweep
- Share most parameters with other parts of BSIM model, but used very few internal results from other part of BSIM
- Quantum effects
- Embedded surface potential
- Polysilicon depletion effects
- 2 new parameters for retrograde doping
- Built-in infrastructure for possible expansion into I-V and parasitic model



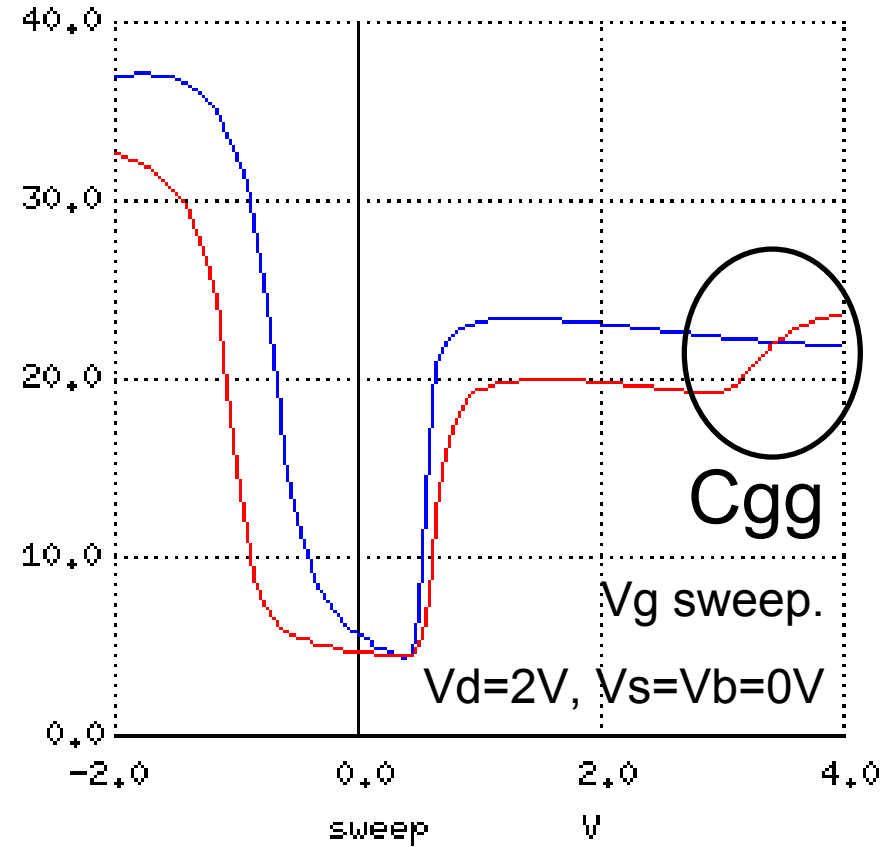
# Preliminary result from CapMod 3

CapMod=3 (red) vs. CapMod=2 (blue)

fV — @m20[ods] — @m19[ods]



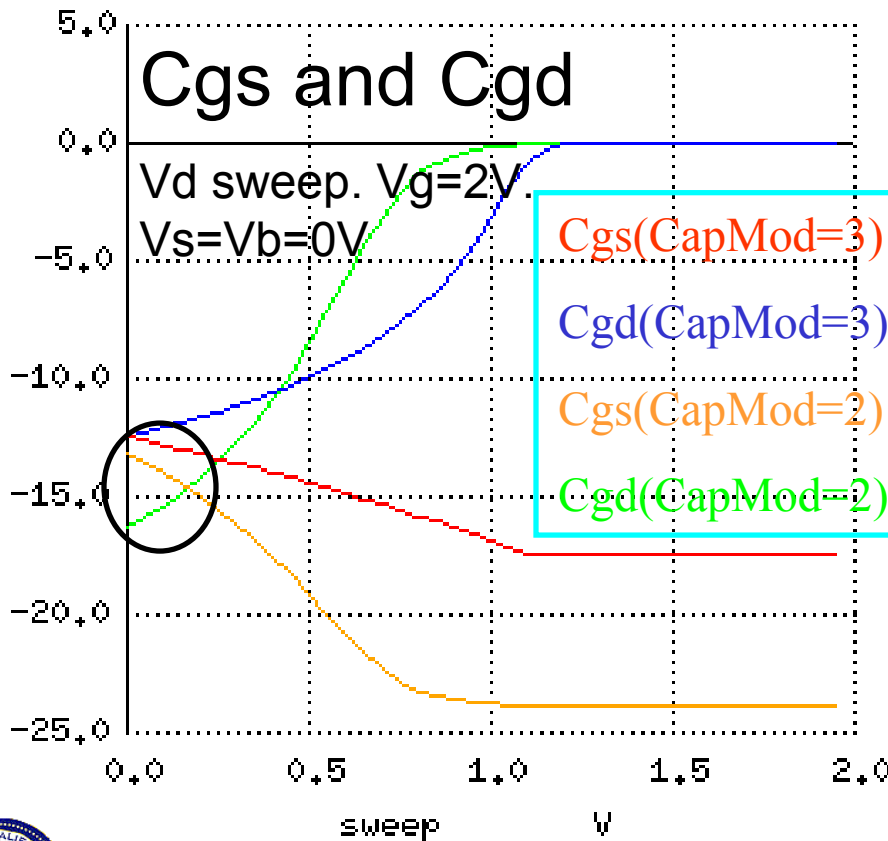
fV — @m20[ogg] — @m19[ogg]



# Preliminary result from CapMod 3

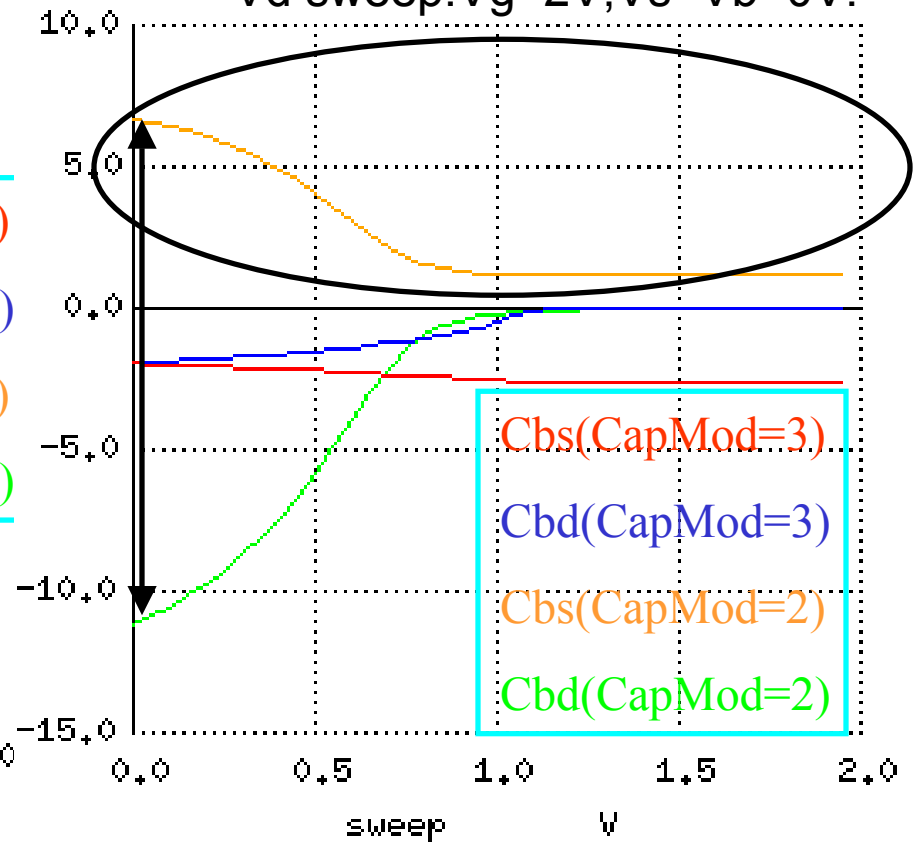
CapMod=3 (red) vs. CapMod=2 (blue)

fV — @m19[logst] — @m19[logd]  
 — @m20[logst] — @m20[logd]



## Cbs and Cbd

Vd sweep. Vg=2V, Vs=Vb=0V.

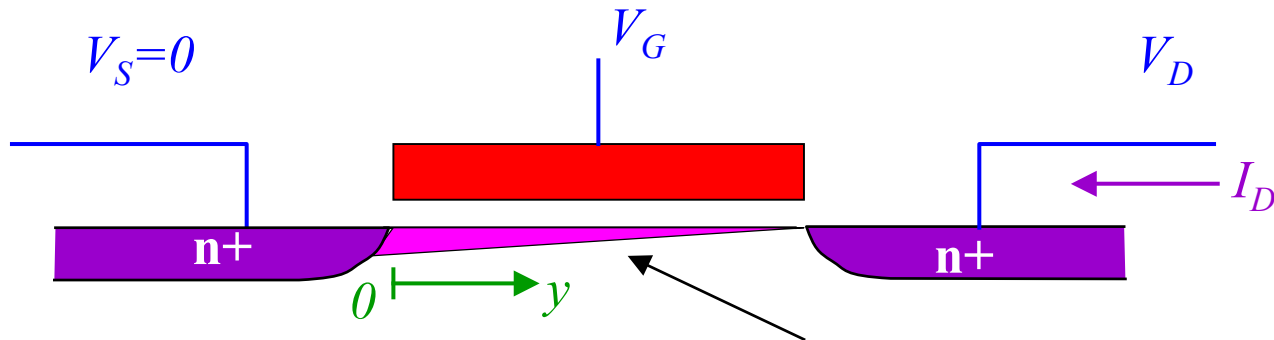


# The Meyer's Model

- Still the most widely used model in among circuit designers
- Simplicity of the model for hand calculations is the most important factor for its wide spread usage
- Still being use even for submicron devices with modified parameter extraction technique with calculated design margins
- Provide an entry point to understand the BSIM models



# The Basic of the Meyer's Model [1]



anywhere along the conducting channel:

$$I(y) = I_D = WQ_n(y)v(y) \quad \dots\dots\dots (1)$$

free carrier  
(inversion charge) density

velocity of carriers

$$Q_n \approx C_{ox}(V_G - V_T - V(y))$$

$$v(y) \approx \mu \vec{E} = \mu \frac{dV(y)}{dy}$$



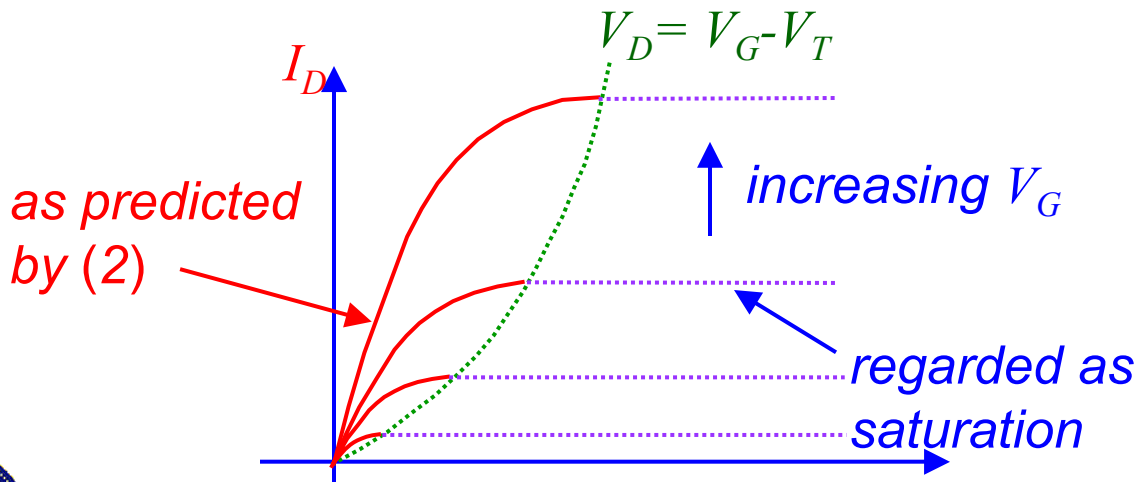
# The Basic of the Meyer's Model [2]

$$\int_0^L I_D dy = \mu W C_{ox} \int_0^{V_{DS}} (V_G - V_T - V(y)) dV \quad \dots\dots\dots (2)$$

$$\Rightarrow I_D = W C_{ox} \left[ (V_G - V_T) - \frac{V_{DS}}{2} \right] \mu \frac{V_{DS}}{L} \quad \text{for } V_{DS} < V_G - V_T$$

average free carrier density in the mid-potential point of the channel

velocity of carriers with average E-field proportional to  $V_{DS}$



$$I_{Dsat} \approx \frac{\mu W C_{ox}}{2L} (V_G - V_T)^2$$

for  $V_{DS} > V_G - V_T$



# Most important Addition in BSIM [1]

## ■ Mobility degradation in BSIM

- mobMod = 1

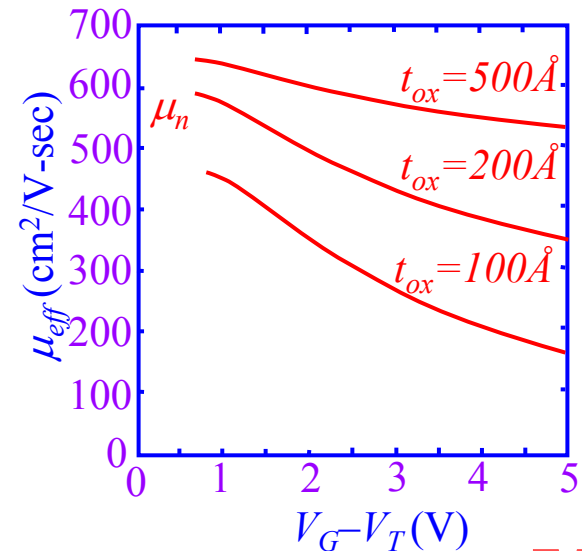
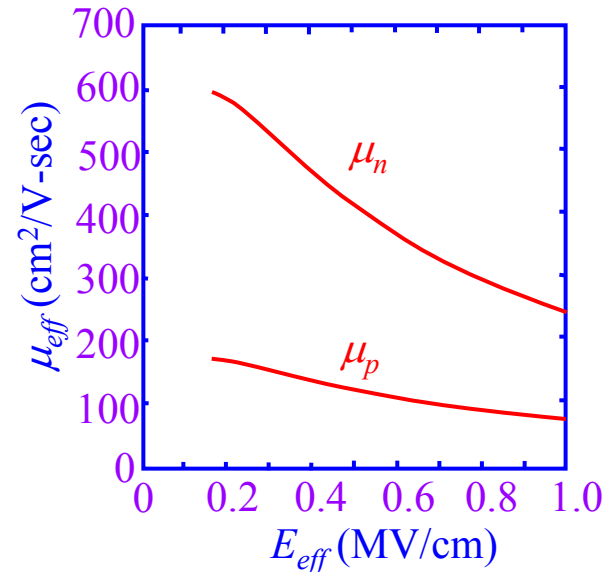
$$\mu_{\text{eff}} = \frac{\mu_0}{1 + (U_A + U_C V_{BS}) \left( \frac{V_G + V_T}{t_{ox}} \right) + U_B \left( \frac{V_G + V_T}{t_{ox}} \right)^2}$$

- mobMod = 2

$$\mu_{\text{eff}} = \frac{\mu_0}{1 + (U_A + U_C V_{BS}) \left( \frac{V_G - V_T}{t_{ox}} \right) + U_B \left( \frac{V_G - V_T}{t_{ox}} \right)^2}$$

- mobMod = 3

$$\mu_{\text{eff}} = \frac{\mu_0}{1 + \left[ U_A \left( \frac{V_G + V_T}{t_{ox}} \right) + U_B \left( \frac{V_G + V_T}{t_{ox}} \right)^2 \right] (1 + U_C V_{BS})}$$



# Most important Addition in BSIM [2]

## Carrier velocity saturation

$$v = \frac{\mu_{\text{eff}} E}{1 + E/E_{\text{sat}}} \quad \text{for } E < E_{\text{sat}}$$

$$= v_{\text{sat}} \quad \text{for } E > E_{\text{sat}}$$

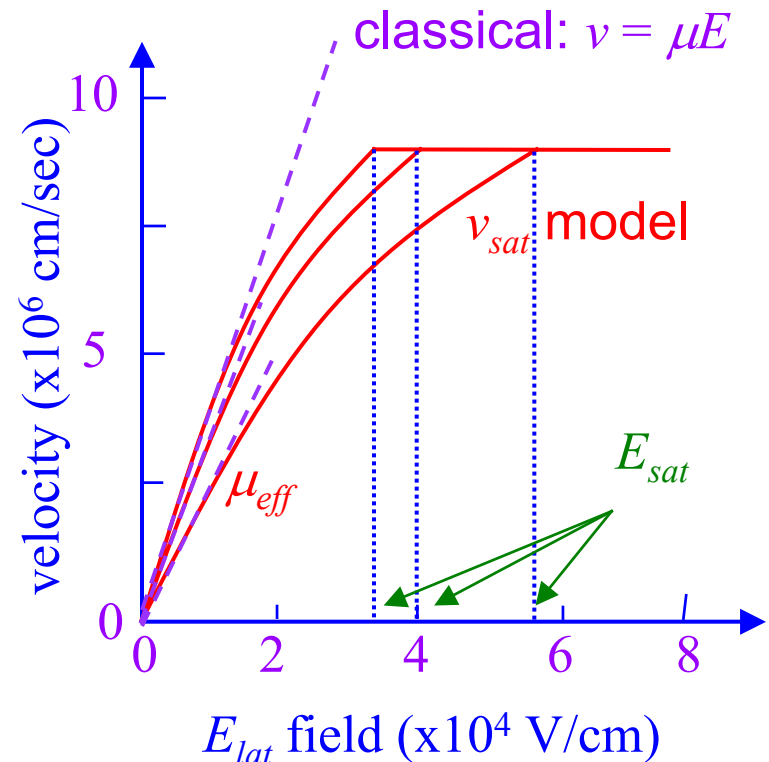
where  $E_{\text{sat}} = \frac{2v_{\text{sat}}}{\mu_{\text{eff}}}$

## New set of equations

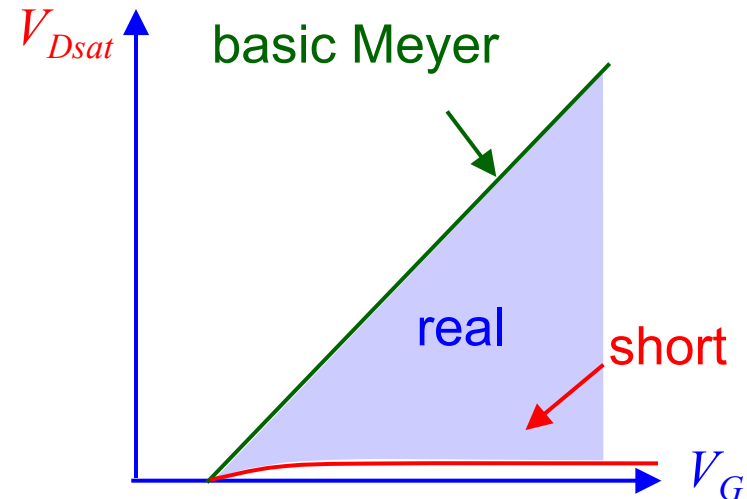
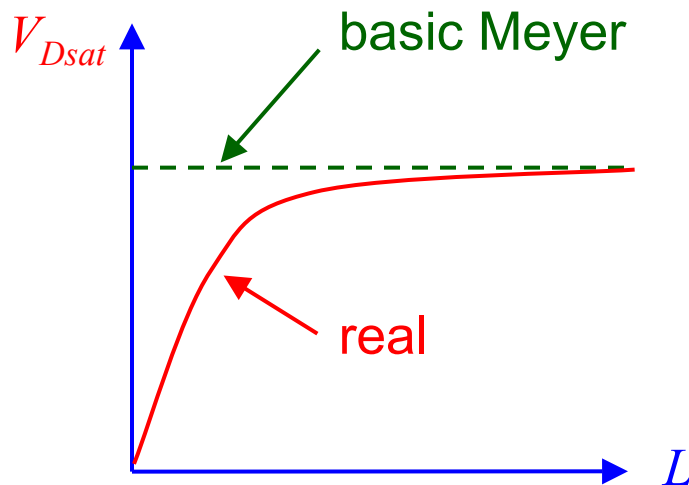
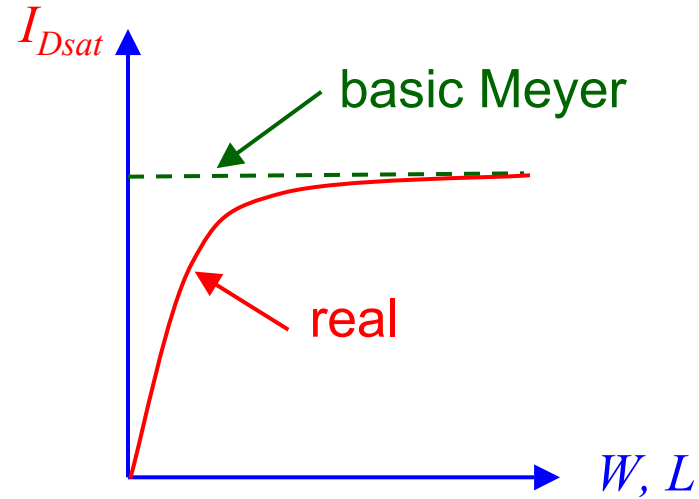
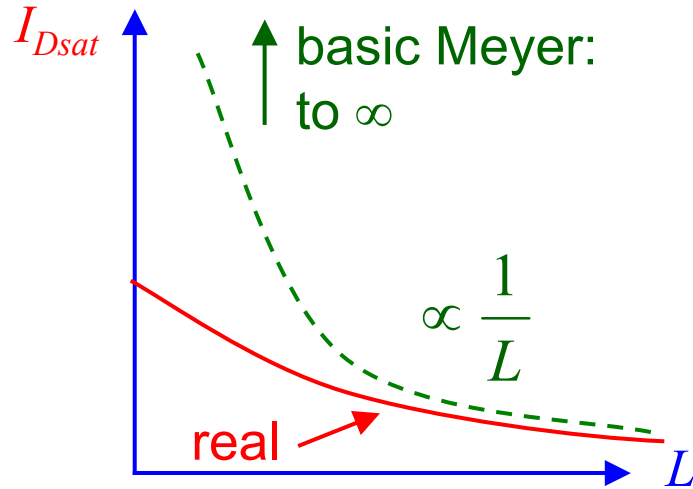
$$I_{\text{Dlin}} = C_{\text{ox}} \frac{W}{L} \left( V_G - V_T - \frac{V_{\text{DS}}}{2} \right) V_{\text{DS}} \frac{\mu_{\text{eff}}}{1 + V_{\text{DS}}/E_{\text{sat}} L}$$

$$I_{\text{Dsat}} = WC_{\text{ox}} (V_G - V_T - V_{\text{Dsat}}) v_{\text{sat}}$$

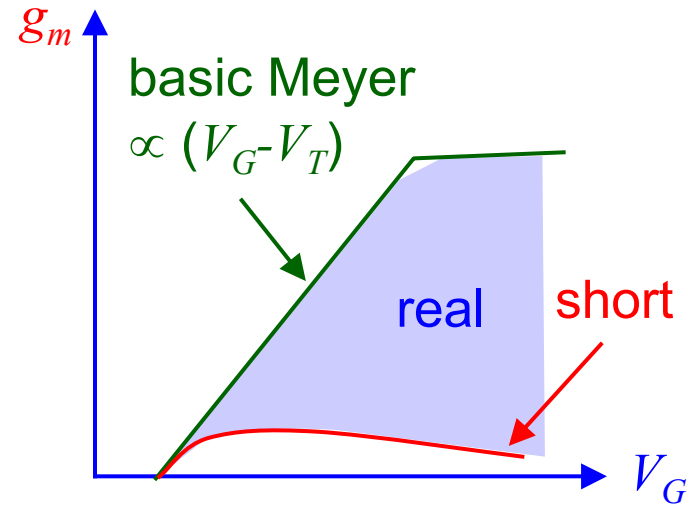
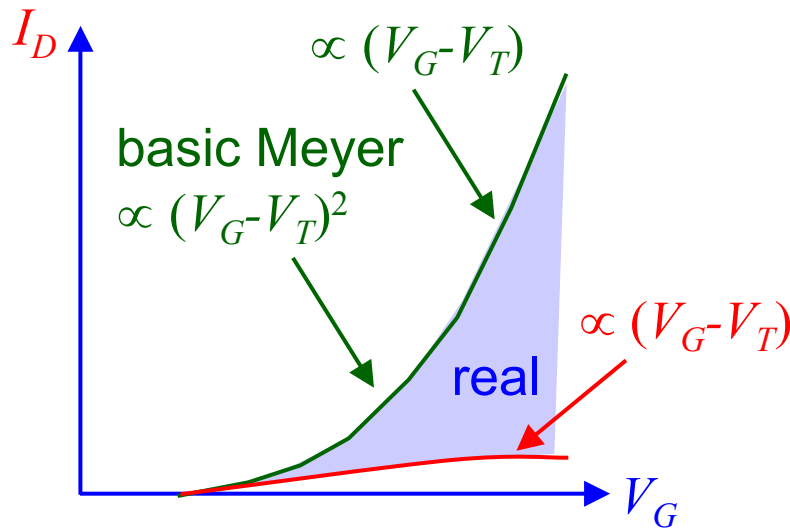
where  $V_{\text{Dsat}} = \frac{(V_G - V_T) E_{\text{sat}} L}{V_G - V_T + E_{\text{sat}} L}$



# Correction to the basic Meyer Model [1]



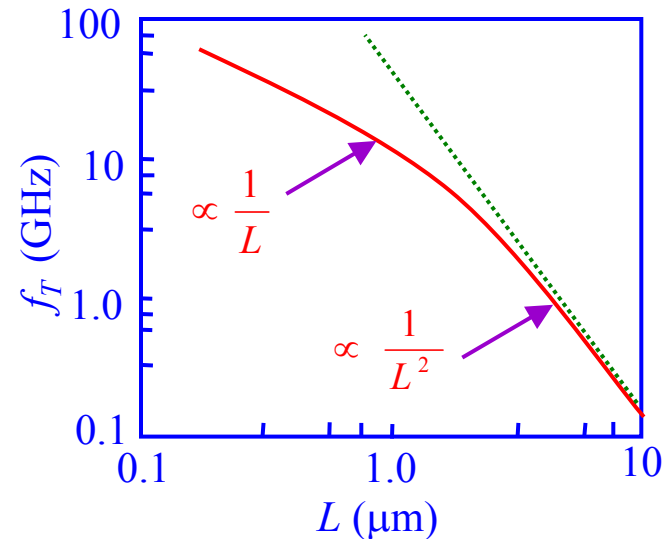
# Correction to the basic Meyer Model [2]



$$f_T = \frac{g_m}{2\pi C_{in}}$$

$$= \frac{\mu}{2\pi L_{eff}^2} (V_G - V_T) \text{ basic Meyer}$$

$$f_T = \frac{v_{sat}}{L_{eff}} \left( 1 - \frac{\partial V_{Dsat}}{\partial V_G} \right) \text{ corrected model}$$



# Basic Set of Parameters

## ■ Threshold voltage

$V_{th0}$ : long channel  $V_T$  at  $V_{BS}=0V$

$K1$ : first order body effect  $\gamma$

$K2$ : second order body effect

$K3, K3B$ : body effect in narrow width devices

$D_{VT0W}, D_{VT1W}, D_{VT2W}, D_{VT0}, D_{VT1}, D_{VT2}$ : narrow-width and short channel non-ideality effect

## ■ mobility degradation

$\mu_0$ : low field mobility

$UA$ : 1<sup>st</sup> order mobility degradation coefficient

$UB$ : 2<sup>nd</sup> order  $\mu$  degradation coefficient

$UC$ : body factor on  $\mu$  degradation

## ■ velocity saturation model

$v_{sat}$ : saturation velocity

$A1$ : first non-saturation parameter

$A2$ : second non-saturation parameter



# Example Calculation

## Given data

$$t_{ox}=200\text{\AA}, W=50\mu\text{m}, L=0.5\mu\text{m}, V_G=3\text{V}, V_T=0.7\text{V}, V_D=1.5\text{V}$$

$$\mu_{eff} = \frac{\mu_0}{1 + U_A \left( \frac{V_G + V_T}{t_{ox}} \right) + U_B \left( \frac{V_G + V_T}{t_{ox}} \right)^2} = 466 \text{cm}^2/\text{V} - \text{sec}$$

using  $U_0=670 \text{ cm}^2/\text{V} - \text{sec}$ ,  $U_A= 2.25 \times 10^{-9} \text{ m/V}$  and  $U_B=5.87 \times 10^{-19} (\text{m/V})^2$

$$\text{from } v_{sat}=8 \times 10^4 \text{ m/sec} \quad E_{sat} = \frac{2v_{sat}}{\mu_{eff}} \approx 3.43 \times 10^4 \text{ Vcm}^{-1}$$

$$V_{Dsat} = \frac{(V_G - V_T) E_{sat} L}{V_G - V_T + E_{sat} L} = 0.98 \text{V}$$

$$V_D = 1.5 \text{V} > V_{Dsat} \Rightarrow I_D = WC_{ox} v_{sat} (V_G - V_T - V_{Dsat}) = 9 \text{mA}$$

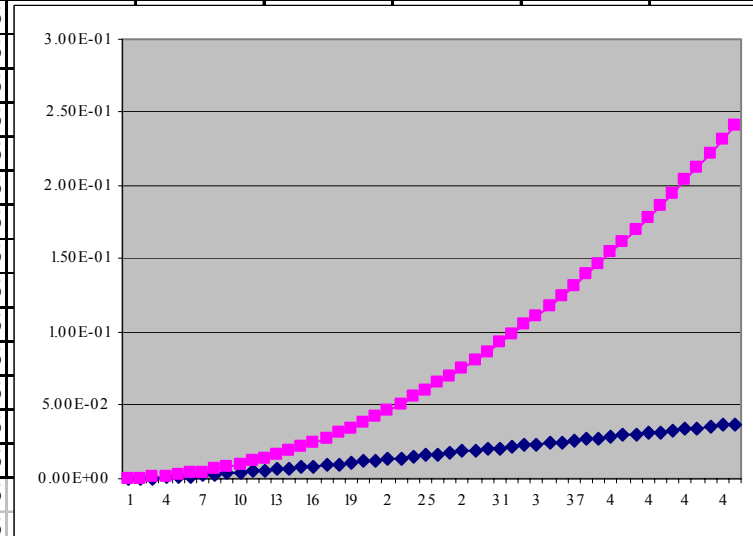
- note: if  $V_D < V_{Dsat}$ , use linear region equation

$$I_D = C_{ox} \frac{W}{L} \left( V_G - V_T - \frac{V_{DS}}{2} \right) V_{DS} \frac{\mu_{eff}}{1 + V_{DS}/E_{sat} L}$$



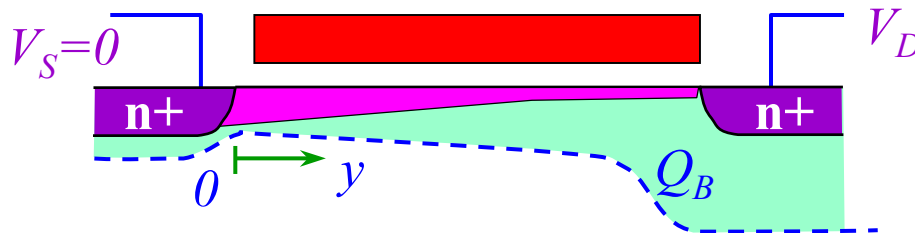
# Example calculation with EXCEL

L (cm)	W (cm)	Tox (cm)	Cox(F)	VT (V)	u0 (cm <sup>2</sup> /V)	VG (V)	VD (V)	mobility (cm <sup>2</sup> /V·s)	Esat(V/cm)	EsatL (V)	Vdsat	Idsat(S)	Idsat (L)
6.00E-05	6.00E-03	1.20E-06	2.88E-07	0.7	6.70E+02	0.8	5	4.97E+02	3.22E+04	1.93E+00	9.51E-02	6.79E-05	9.635E-05
6.00E-05	6.00E-03	1.20E-06	2.88E-07	0.7	6.70E+02	0.9	5	4.88E+02	3.28E+04	1.97E+00	1.82E-01	2.55E-04	0.0003854
6.00E-05	6.00E-03	1.20E-06	2.88E-07	0.7	6.70E+02	1	5	4.80E+02	3.33E+04	2.00E+00	2.61E-01	5.40E-04	0.0008672
6.00E-05	6.00E-03	1.20E-06	2.88E-07	0.7	6.70E+02	1.1	5	4.72E+02	3.39E+04	2.03E+00	3.34E-01	9.08E-04	0.0015417
6.00E-05	6.00E-03	1.20E-06	2.88E-07	0.7	6.70E+02	1.2	5	4.64E+02	3.45E+04	2.07E+00	4.03E-01	1.34E-03	0.0024089
6.00E-05	6.00E-03	1.20E-06	2.88E-07	0.7	6.70E+02	1.3	5	4.57E+02	3.50E+04	2.10E+00	4.67E-01	1.84E-03	0.0034688
6.00E-05	6.00E-03	1.20E-06	2.88E-07	0.7	6.70E+02	1.4	5	4.49E+02	3.57E+04	2.14E+00	5.27E-01	2.38E-03	0.0047214
6.00E-05	6.00E-03	1.20E-06	2.88E-07	0.7	6.70E+02	1.5	5	4.41E+02	3.63E+04	2.18E+00	5.85E-01	2.97E-03	0.0061667
6.00E-05	6.00E-03	1.20E-06	2.88E-07	0.7	6.70E+02	1.6	5	4.34E+02	3.69E+04	2.21E+00	6.40E-01	3.59E-03	0.0078047
6.00E-05	6.00E-03	1.20E-06	2.88E-07	0.7	6.70E+02	1.7	5						
6.00E-05	6.00E-03	1.20E-06	2.88E-07	0.7	6.70E+02	1.8	5						
6.00E-05	6.00E-03	1.20E-06	2.88E-07	0.7	6.70E+02	1.9	5						
6.00E-05	6.00E-03	1.20E-06	2.88E-07	0.7	6.70E+02	2	5						
6.00E-05	6.00E-03	1.20E-06	2.88E-07	0.7	6.70E+02	2.1	5						
6.00E-05	6.00E-03	1.20E-06	2.88E-07	0.7	6.70E+02	2.2	5						
6.00E-05	6.00E-03	1.20E-06	2.88E-07	0.7	6.70E+02	2.3	5						
6.00E-05	6.00E-03	1.20E-06	2.88E-07	0.7	6.70E+02	2.4	5						
6.00E-05	6.00E-03	1.20E-06	2.88E-07	0.7	6.70E+02	2.5	5						
6.00E-05	6.00E-03	1.20E-06	2.88E-07	0.7	6.70E+02	2.6	5						
6.00E-05	6.00E-03	1.20E-06	2.88E-07	0.7	6.70E+02	2.7	5						
6.00E-05	6.00E-03	1.20E-06	2.88E-07	0.7	6.70E+02	2.8	5						
6.00E-05	6.00E-03	1.20E-06	2.88E-07	0.7	6.70E+02	2.9	5						
6.00E-05	6.00E-03	1.20E-06	2.88E-07	0.7	6.70E+02	3	5						
6.00E-05	6.00E-03	1.20E-06	2.88E-07	0.7	6.70E+02	3.1	5						
6.00E-05	6.00E-03	1.20E-06	2.88E-07	0.7	6.70E+02	3.2	5						
6.00E-05	6.00E-03	1.20E-06	2.88E-07	0.7	6.70E+02	3.3	5	3.25E+02	4.92E+04	2.95E+00	1.38E+00	1.68E-02	0.0651356



# Bulk Charge Effects [1]

## Non-uniform substrate charge



$$Q_n = C_{ox} (V_{GS} - V_T(y) - V(y))$$

## To avoid complex mathematical formulation, a fitting approach is used by introducing an $A_{bulk}$ parameter

$$I_D = C_{ox} \frac{W}{L} \left( V_G - V_T - \frac{A_{bulk} V_{DS}}{2} \right) V_{DS} \frac{\mu_{eff}}{1 + V_{DS}/E_{sat} L}$$

$$V_{Dsat} = \frac{(V_G - V_T) E_{sat} L}{V_G - V_T + A_{bulk} E_{sat} L}$$

$$I_{Dsat} = WC_{ox} v_{sat} (V_G - V_T - A_{bulk} V_{Dsat}) v_{sat}$$



# Bulk Charge Effects [2]

## ■ $A_{bulk}$ expression

$$A_{bulk} = \left\{ 1 + \frac{K1}{2\sqrt{\phi_S - V_{BS}}} \left[ \frac{A_0 L}{L + 2\sqrt{x_j X_{dep}}} \left( 1 - A_{GS} (V_G - V_T) \left( \frac{L}{L + 2\sqrt{x_j X_{dep}}} \right)^2 + \frac{B_0}{W + B_1} \right) \right] \right\} \frac{1}{1 + K_{ETA} V_{BS}}$$

parameters:  $A_0$ ,  $A_{GS}$ ,  $B_0$ ,  $B_1$ ,  $K_{ETA}$

## ■ why empirical approach?

- device is never ideal due to edge effects and non-uniform lateral doping
- flexibility is required to fit a wide range of technologies

## ■ for near ideal device

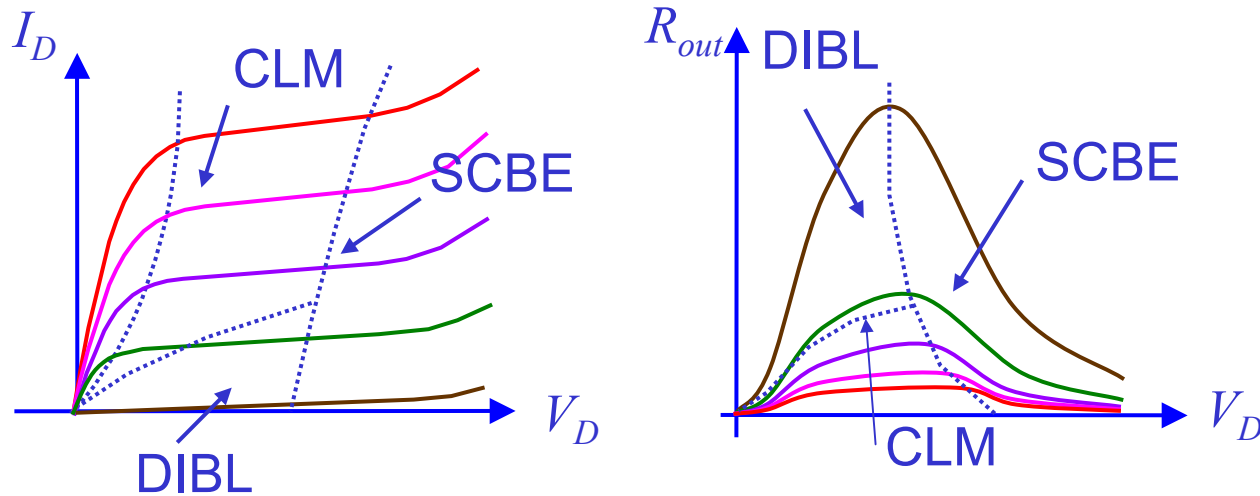
$$A_{GS}=0, B_0=0 \text{ and } B_1=0 \quad A_{bulk} = \left\{ 1 + \frac{K1}{2\sqrt{\phi_S - V_{BS}}} \left[ \frac{A_0 L}{L + 2\sqrt{x_j X_{dep}}} \right] \right\} \frac{1}{1 + K_{ETA} V_{BS}}$$



# Output resistance model [1]

## 3 Effects to account for

- Channel Length Modulation (CLM)
- Drain Induced Barrier Lowering (DIBL)
- Substrate Current induced Body Effect (SCBE)

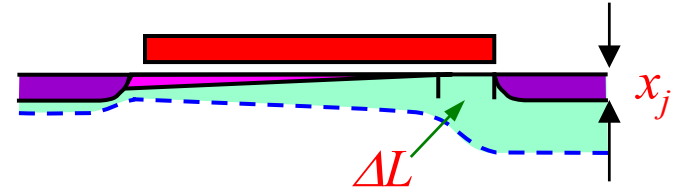


## CLM is the dominating effect



# Output resistance model [2]

## Channel Length Modulation



$$\Delta L = l_1 \ln \left[ \frac{V_D - V_{Dsat}}{E_{sat} l_1} \right] \quad \text{where } l_1 \text{ is a fitting parameter} = 0.22 t_{ox}^{1/3} x_j^{1/2}$$

## $R_{out}$ as a result of CLM

$$\frac{1}{R_{out}} = \frac{dI_{Dsat}}{d\Delta L} \frac{d\Delta L}{dV_D} \Rightarrow R_{out} = \frac{V_D - V_{Dsat0}}{P_{CLM} I_{Dsat0} l_1} \left( L + \frac{V_G - V_T}{E_{sat}} \right)$$

## Incorporate into current equation

$$I_{Dsat}(V_D) = I_{Dsat0} \left[ 1 + \frac{(V_D - V_{Dsat0})}{V_{ACLM}} \right]$$

where  $V_{ACLM} = R_{out(CL M)} I_{Dsat0}$



# Output resistance model [3]

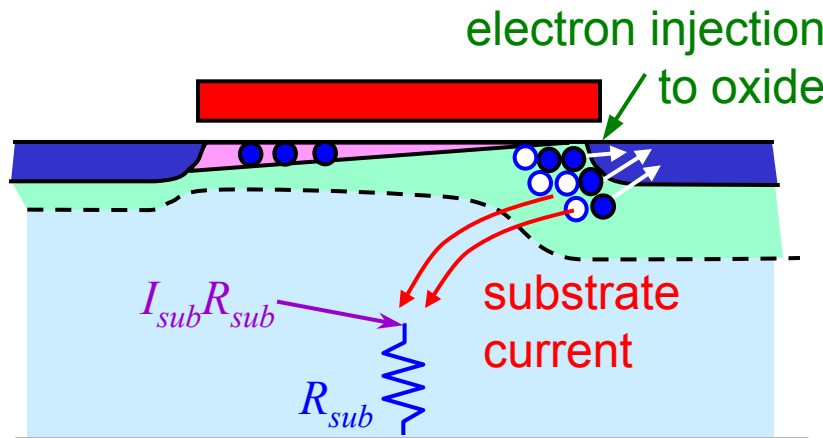
## DIBL

$$\frac{1}{R_{out}} = \frac{dI_{Dsat}}{dV_T} \frac{dV_T}{dV_D} \Rightarrow R_{out(DIBL)} = \frac{(V_G - V_T)}{\theta_{rout}(1 + P_{DIBLCB} V_{BS})} \left[ 1 + \frac{V_{Dsat}}{(V_{Dsat} + V_G - V_T)} \right]$$

with  $\theta_{rout} = P_{DIBLC1} \left( e^{-L/2l_2} + 2e^{-L/l_2} \right) + P_{DIBLC2}$

where  $l_2$  is another fitting parameter =  $\sqrt{\frac{\epsilon_{Si} t_{ox} x_{Dmax}}{\epsilon_{ox}}}$

## SCBE



$$I_{sub} = \frac{A}{B} (V_D - V_{Dsat}) I_D e^{\frac{-Bl_1}{V_D - V_{Dsat}}}$$

where

	NMOS	PMOS
$B$ ( $Vcm^{-1}$ )	$1.7 \times 10^6$	$3.7 \times 10^6$
$A/B$ ( $V^{-1}$ )	1.2	2.2

and  $l_1 = 0.22 t_{ox}^{1/3} x_j^{1/2}$



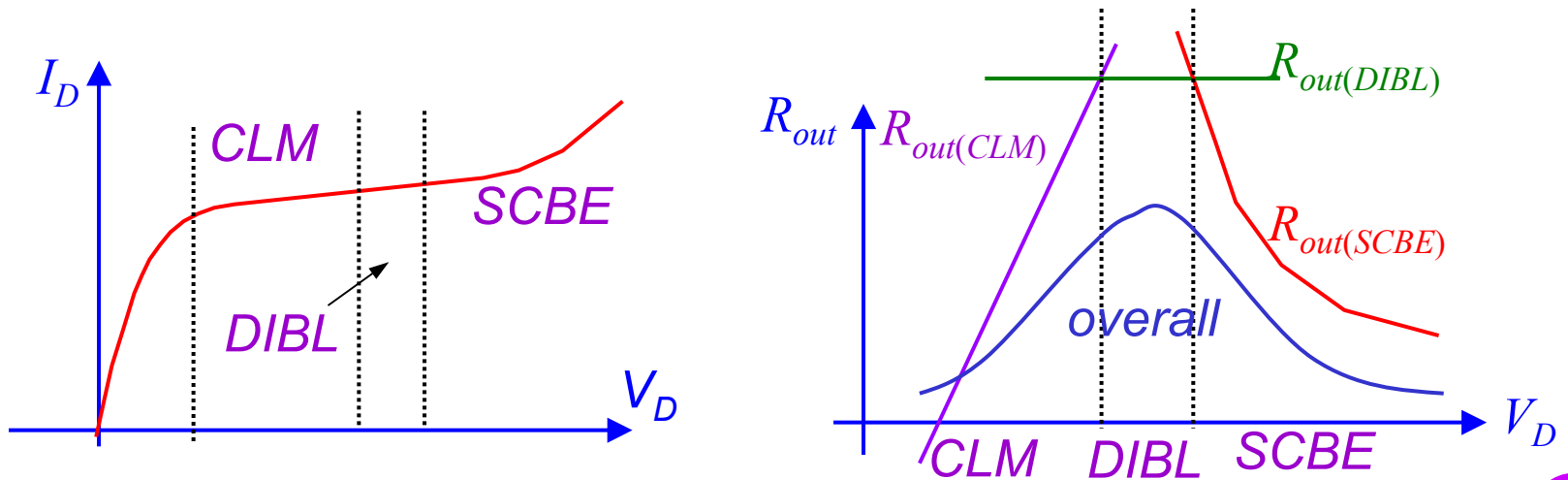
# Output resistance model [4]

$$\frac{1}{R_{out}} = \frac{dI_{Dsat}}{dV_T} \frac{dV_T}{dV_{BS}} \frac{dV_{BS}}{dI_{sub}} \frac{dI_{sub}}{dV_D}$$

$$\Rightarrow R_{out} \approx \left[ I_D \frac{A}{B} \left( 1 + g_m \frac{K1R_{sub}}{2\sqrt{2\phi_B - V_{BS}}} \left( 1 + \frac{Bl_1}{V_D - V_{Dsat}} \right) \right) \exp\left( -\frac{Bl_1}{V_D - V_{Dsat}} \right) \right]^{-1}$$

## Overall $R_{out}$ model

$$I_{Dsat}(V_D) = I_{Dsat0} \left[ 1 + \frac{(V_D - V_{Dsat0})}{V_{ACLM}} \right] \left[ 1 + \frac{(V_D - V_{Dsat0})}{V_{ADIBL}} \right] \left[ 1 + \frac{(V_D - V_{Dsat0})}{V_{ASCBE}} \right]$$



# Smoothing Functions [1]

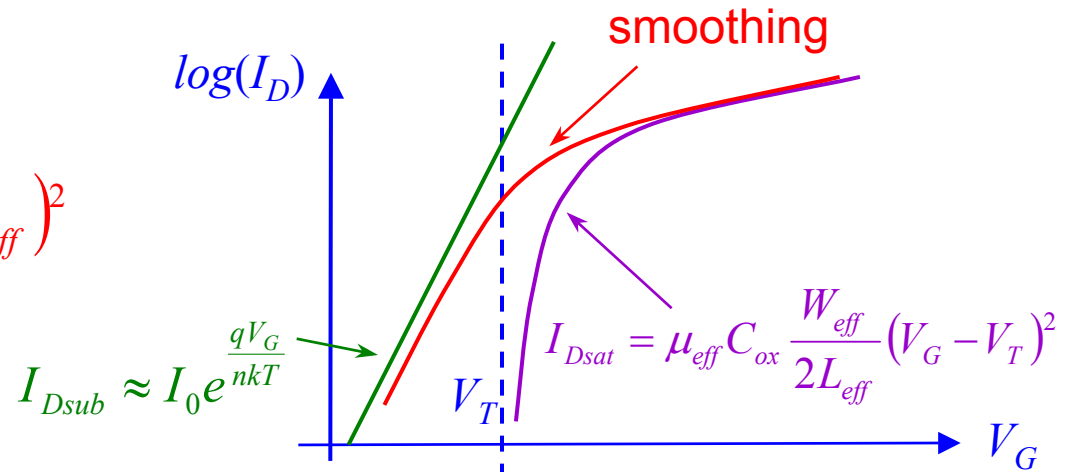
- Ensure fast convergent by having all current and derivatives continuous
- Smoothing function in  $V_{GS}$  domain ( $V_{GS\text{eff}}$ )

$$V_{GS\text{eff}} = \frac{2nV_{th} \ln \left[ 1 + \exp \left( \frac{V_{GS} - V_T}{2nV_{th}} \right) \right]}{1 + 2nC_{ox} \sqrt{\frac{2\phi_s}{q\epsilon_{Si}N_{CH}}} \exp \left( -\frac{V_{GS} - V_T - 2V_{off}}{2nV_{th}} \right)}$$

$V_{off}$ : required for non ideal device effects

and

$$I_{D\text{sat}/\text{sub}} = \mu_{\text{eff}} C_{ox} \frac{W_{\text{eff}}}{2L_{\text{eff}}} (V_{G\text{Teff}})^2$$



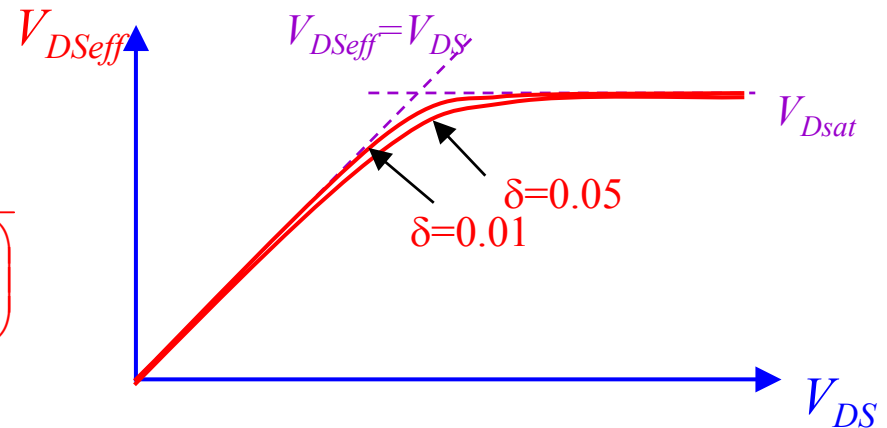
# Smoothing Functions [2]

## Smoothing function in $V_{DS}$ domain ( $V_{DSeff}$ )

$$V_{DSeff} = V_{Dsat} - \frac{1}{2} \left( V_{Dsat} - V_{DS} - \delta + \sqrt{(V_{Dsat} - V_{DS} - \delta)^2 + 4\delta V_{Dsat}} \right)$$

- Where  $\delta$  is a fitting parameter to adjust the abruptness of the transition

$$I_{DS} \approx WC_{ox} \left( V_{GSeff} - \frac{\alpha}{2} V_{DSeff} \right) \frac{\mu V_{DSeff}}{L \left( 1 + \frac{V_{DSeff}}{E_{sat} L} \right)}$$



## Similar approach in $V_{BS}$ domain ( $V_{BSeff}$ )

$$V_{BSeff} = V_{BC} + \frac{1}{2} \left( V_{BS} - V_{BC} - \delta_1 + \sqrt{(V_{BS} - V_{BC} - \delta_1)^2 - 4\delta_1 V_{BC}} \right) \quad \text{with} \quad \delta_1 = 0.001$$



# Simplified Strong Inversion Equations [1]

■ **Define:**  $u_d = \frac{UA}{t_{ox}}$  mobility degradation coefficient

$$u_d \approx 0.5\text{V}^{-1} \quad \text{for } t_{ox}=10\text{nm}$$

$E_c = \frac{2v_{sat}}{U_0}$  critical  $E$ -field for velocity saturation

$$E_c \approx 2 \times 10^4 \text{V/cm} \quad (\text{typical value})$$

## ■ Assumptions:

- $V_T$  is given from the process
- mobility model of mobmod = 2 is used
- bulk charge effect not significant in short channel devices
- Channel Length Modulation is the main contribution to  $R_{out}$



# Simplified Strong Inversion Equations [2]

■ Current Equations in strong inversion becomes

$$V_{Dsat} = (V_G - V_T) \left[ \frac{1 + u_d(V_G - V_T)}{1 + \left(u_d + \frac{1}{E_c L}\right)(V_G - V_T)} \right]$$

$$I_{Dlin} = \mu_0 C_{ox} \frac{W}{L} \left( V_G - V_T - \frac{V_D}{2} \right) V_D \left[ \frac{1}{1 + u_d(V_G - V_T) + \left(\frac{V_D}{E_c L}\right)} \right] = I_{Dlin(long)} \left[ \frac{1}{1 + u_d(V_G - V_T) + \left(\frac{V_D}{E_c L}\right)} \right]$$

$$I_{Dsat} = \mu_0 C_{ox} \frac{W}{2L} \left[ \frac{(V_G - V_T)^2}{1 + \left(u_d + \frac{1}{E_c L}\right)(V_G - V_T)} \right] = I_{Dsat(long)} \left[ \frac{1}{1 + \left(u_d + \frac{1}{E_c L}\right)(V_G - V_T)} \right]$$



# Simplified Strong Inversion Equations [3]

## Equations of derivatives

$$g_{msat} = \frac{I_{Dsat}}{(V_G - V_T)} \left[ 1 + \frac{I_{Dsat}}{I_{Dsat(long)}} \right] = \frac{I_{Dsat}}{(V_G - V_T)} \left[ 1 + \frac{1}{1 + \left( u_d + \frac{1}{E_C L} \right) (V_G - V_T)} \right]$$

$$r_{out} = \frac{2\{(V_D - V_{Dsat}) + [1 + u_d(V_G - V_T)](V_G - V_T)\}L^2}{\mu_0 C_{ox} W l P_{CLM} [1 + u_d(V_G - V_T)](V_G - V_T)^2} = \frac{\{(V_D - V_{Dsat}) + [1 + u_d(V_G - V_T)](V_G - V_T)\}L}{I_{Dsat(long)} l P_{CLM} [1 + u_d(V_G - V_T)]}$$

with  $l = \sqrt{3t_{ox}x_j}$

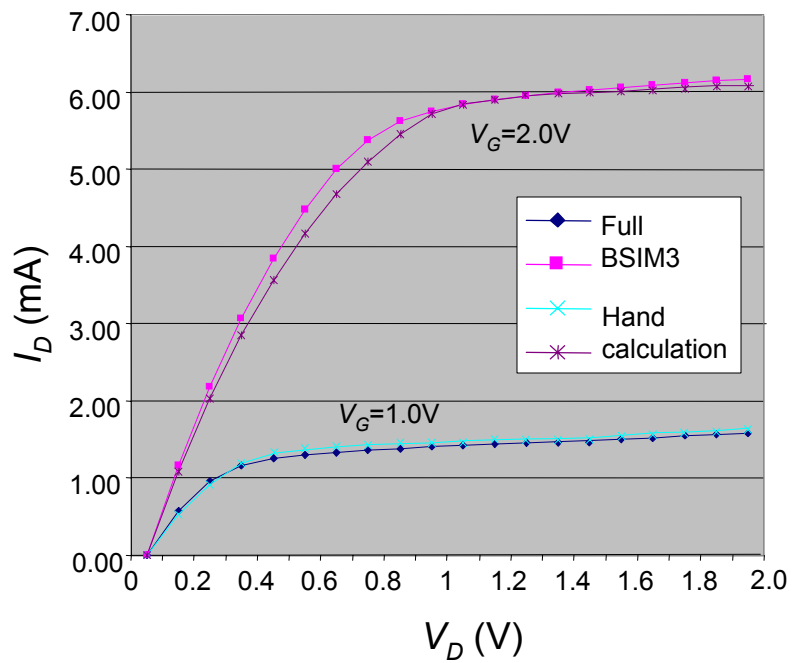
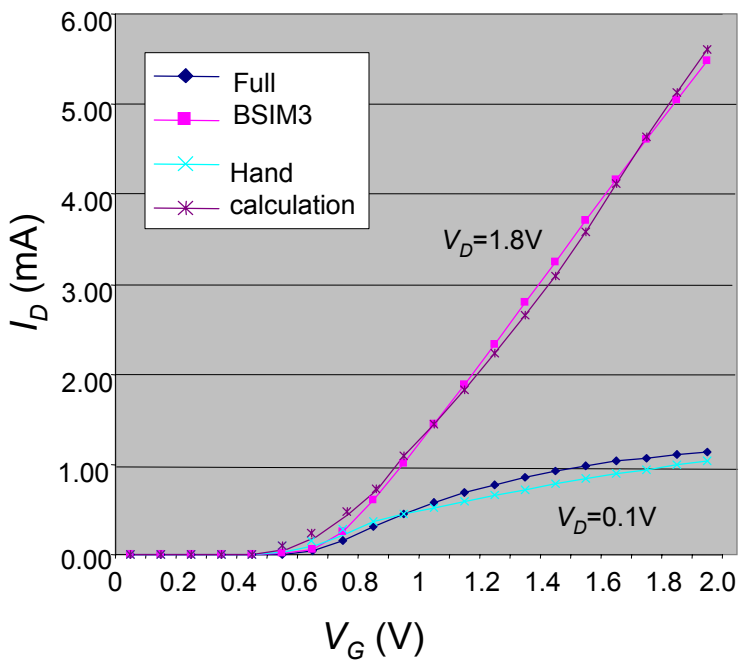
## Parameters used:

*W, L, TOX, U0, UA, VSAT, VTH0, PCLM, XJ*



# Simplified Strong Inversion Equations [4]

## Comparison between full and simplified model



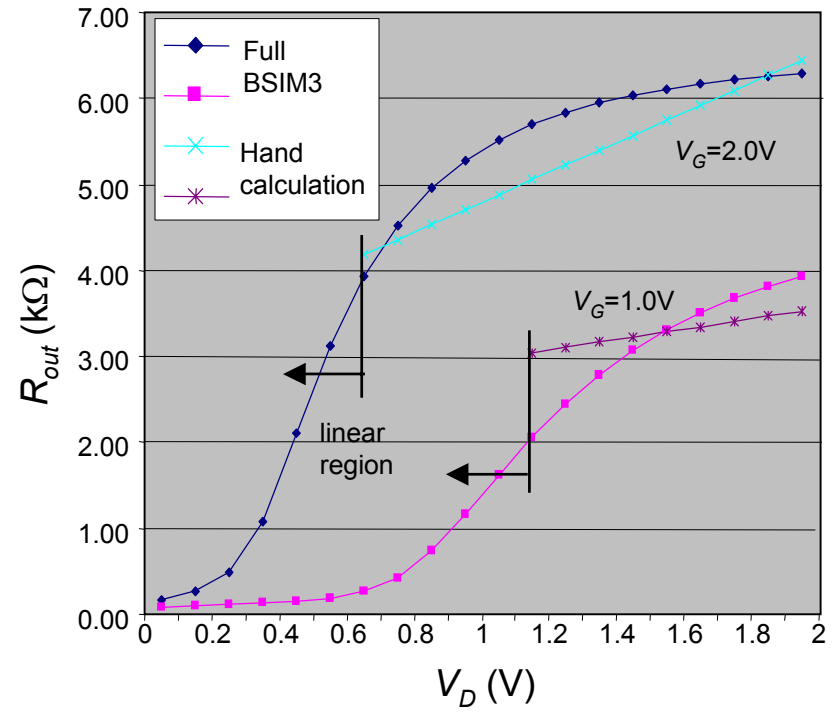
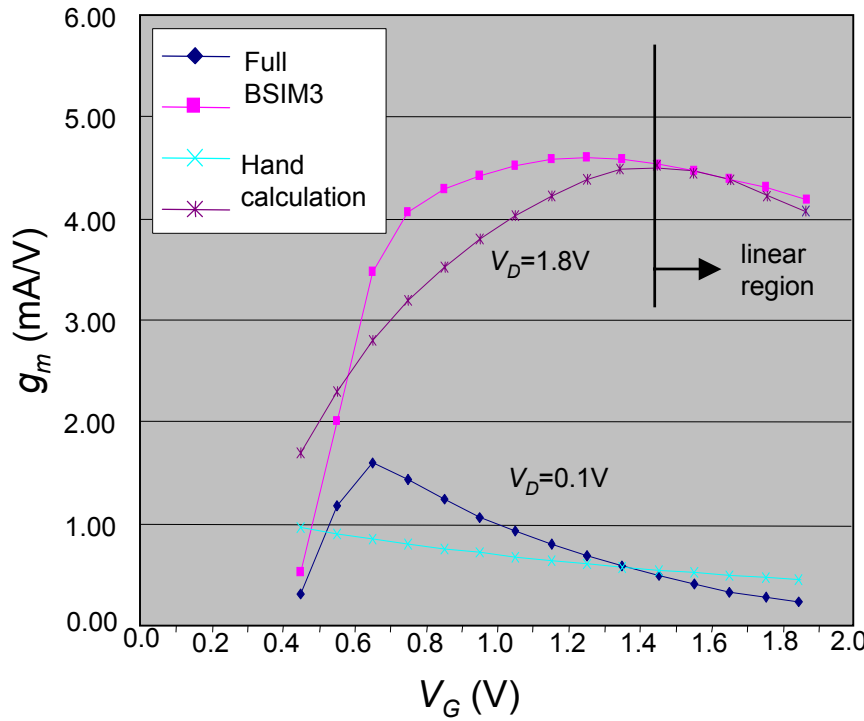
## Parameter detail: TSMC 0.18 $\mu$ m process

$t_{ox}$ : 4.1nm,  $W=10\mu$ m,  $V_{T0}=0.39V$



# Simplified Strong Inversion Equations [5]

## Comparison of first derivative simplification



# Other features included in BSIM3v3

- Short/Narrow Channel Effects on Threshold Voltage
- Non-Uniform Vertical Doping Effects
- Non-Uniform Lateral Doping Effects
- Quantum Mechanic Charge Thickness Model
- Unified Flicker Noise Model
- Polysilicon Depletion Effects
- Non-quasitic Effects



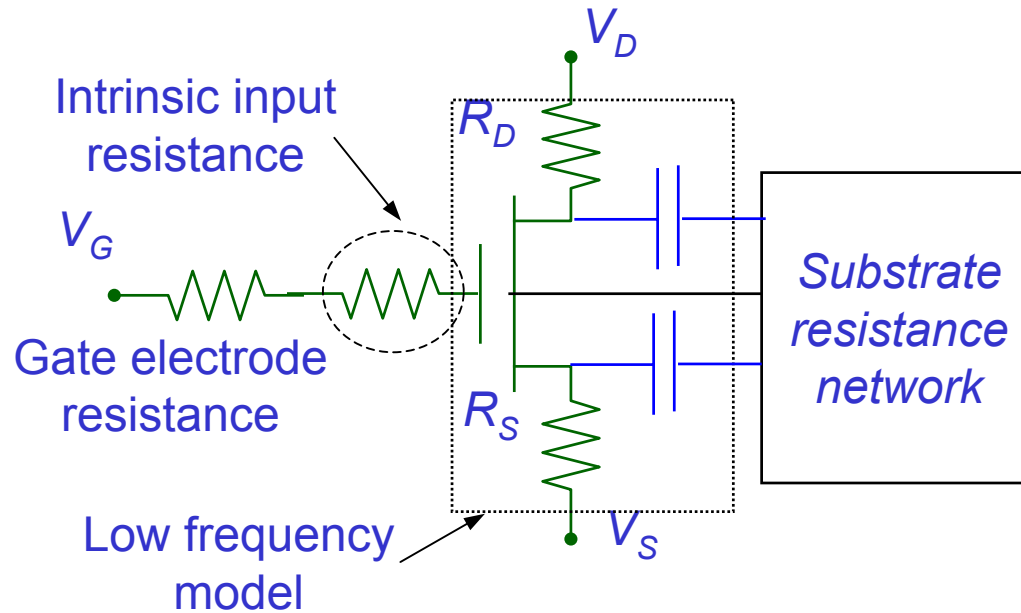
# Additional Features of BSIM4

- Bug-fixes of former BSIM3 model
- Intrinsic input resistance model
- Extrinsic gate resistance model
- New Non-Quasi-Static (NQS) model
- Holistic and noise-partition thermal noise model
- Substrate resistance network
- Improved Flicker noise model
- Geometry calculation (Layout-dependent parasitics) model
- Asymmetrical S/D junction diode model
- Gate-Induced Drain Leakage (GIDL) model
- Gate dielectric tunneling current model



# RF Model in BSIM4

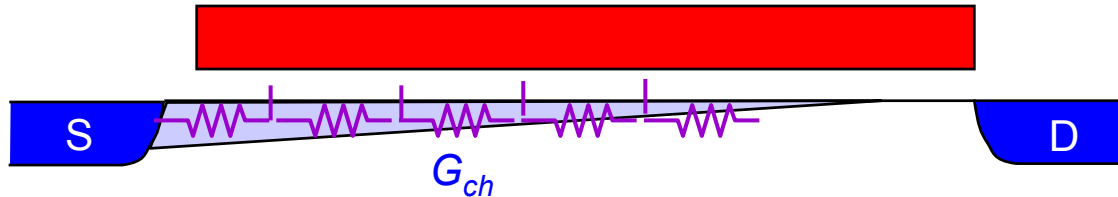
- Require low frequency,  $R_G$  and  $R_{sub}$  model



- Note that it is a RC effect more than NQS effects



# Intrinsic gate resistance model



**in strong inversion**

$$R_{ii}(inv) = \frac{R_{ch}}{\eta} = \frac{V_{DS}}{\eta I_{DS}} \quad \text{in triode region} \quad \eta \approx 14 \quad \text{as determined by 2-D simulation}$$
$$= \frac{V_{DSat}}{\eta I_{DS}} \quad \text{in saturation}$$

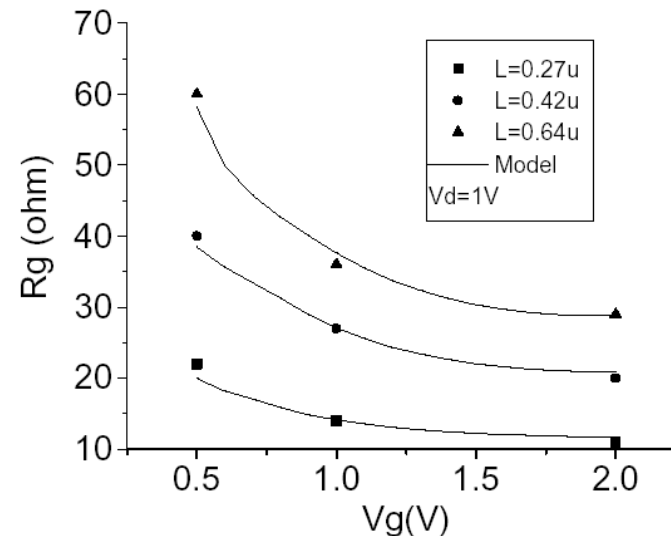
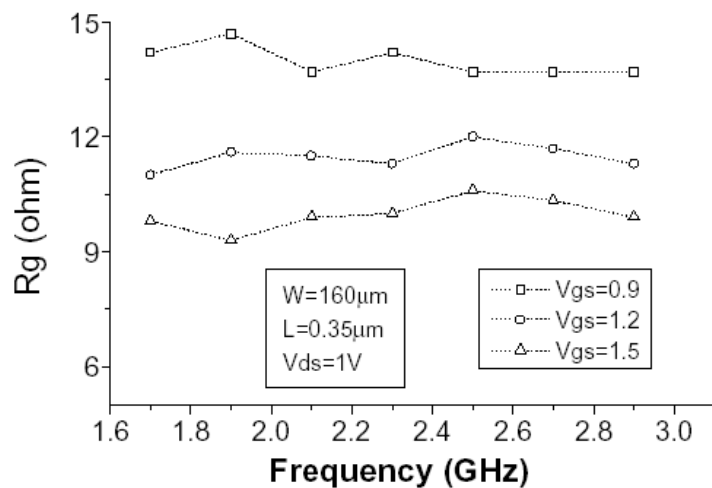
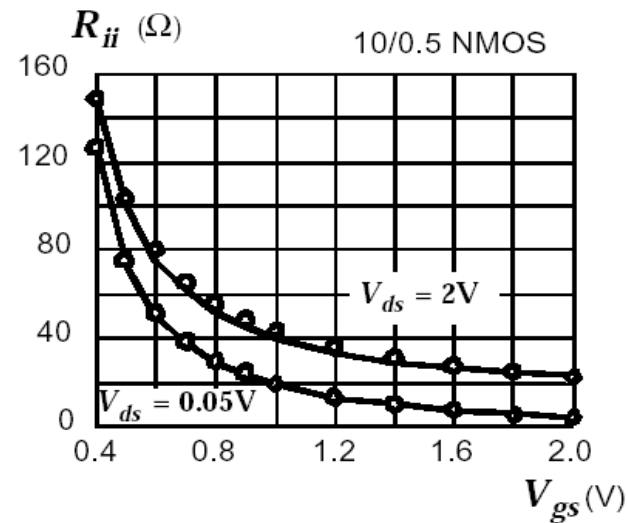
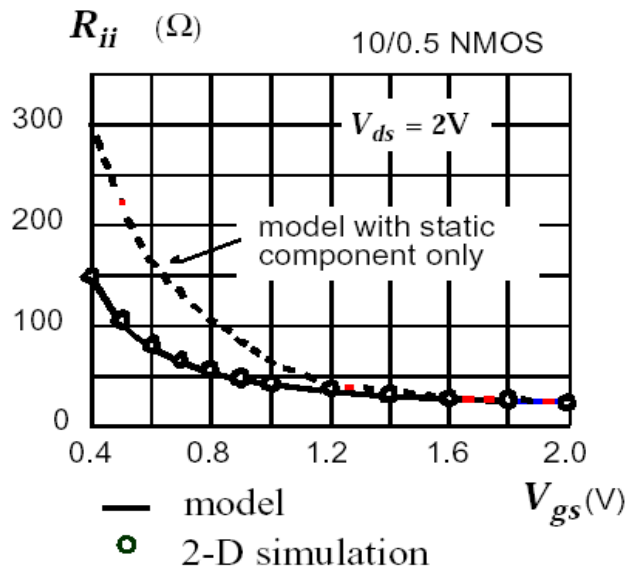
**in subthreshold**

$$R_{ii}(sub) = \left( \frac{kT}{q} \mu_{eff} C_{ox} \frac{W_{eff}}{L_{eff}} \right)^{-1}$$

**combine:**  $R_{ii} = R_{ii}(inv) // R_{ii}(sub)$

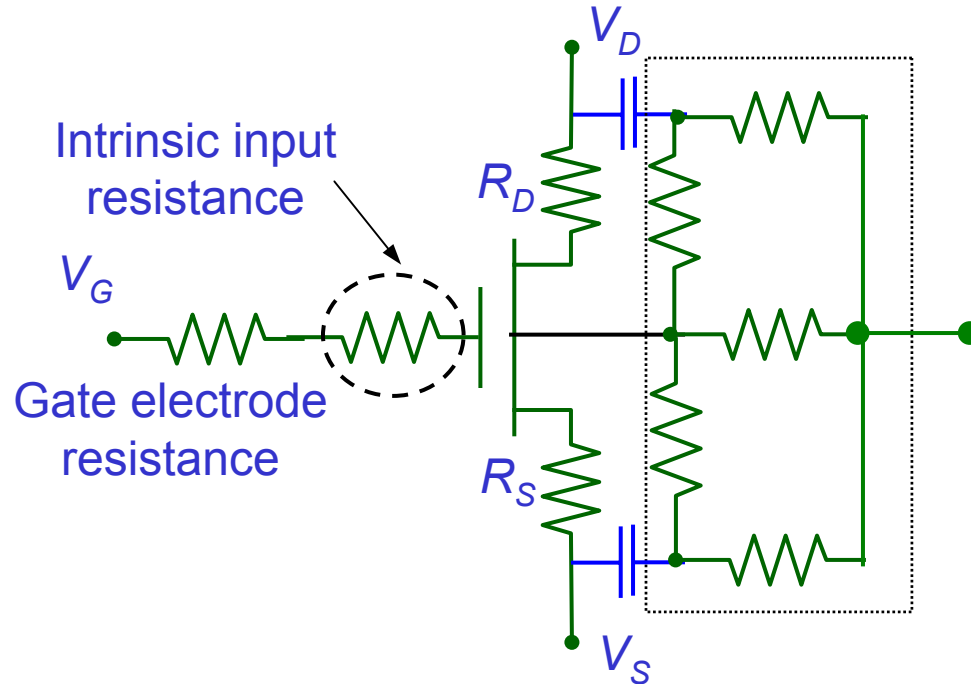


# Intrinsic gate resistance verification



# Substrate Network

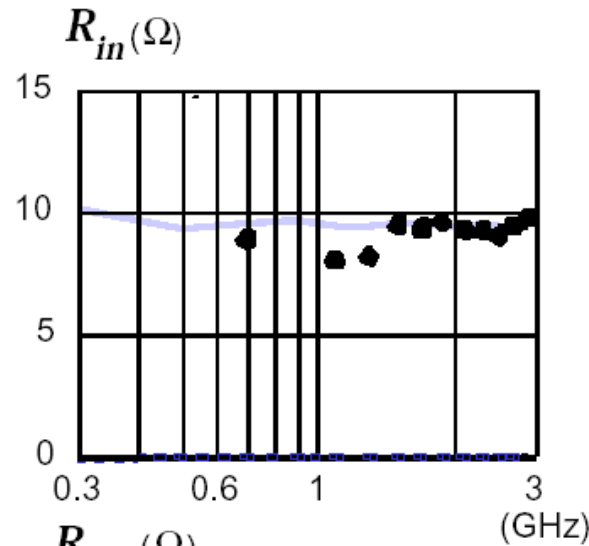
- Responsible for  $R_{out}$  roll-off at high frequency



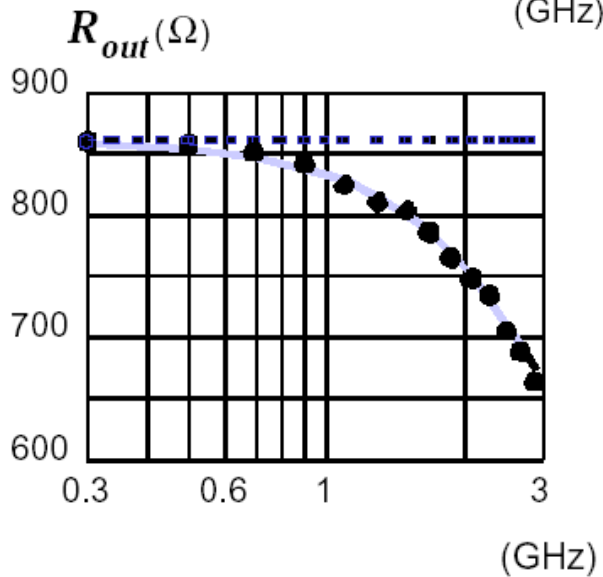
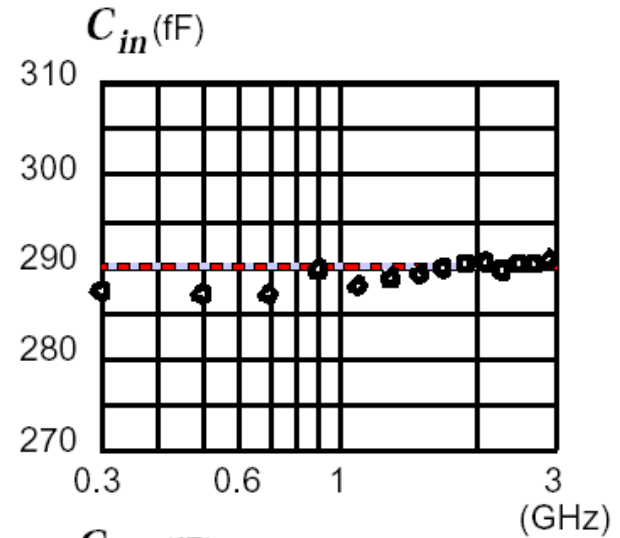
- In practice, 2-3 resistors are sufficient for accurate modeling



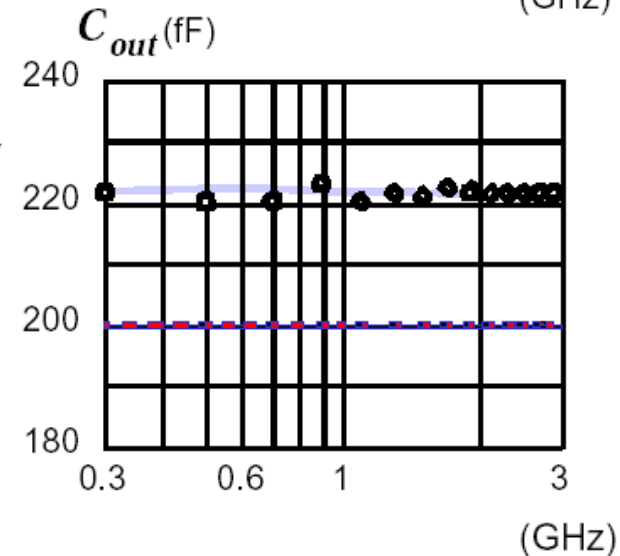
# Verification of Substrate Network



● Measured  
 - - - BSIM3v3  
 — BSIM RF  
 $R_g = 9.5 \Omega$   
 $R_{Subd,s} = 50 \Omega$

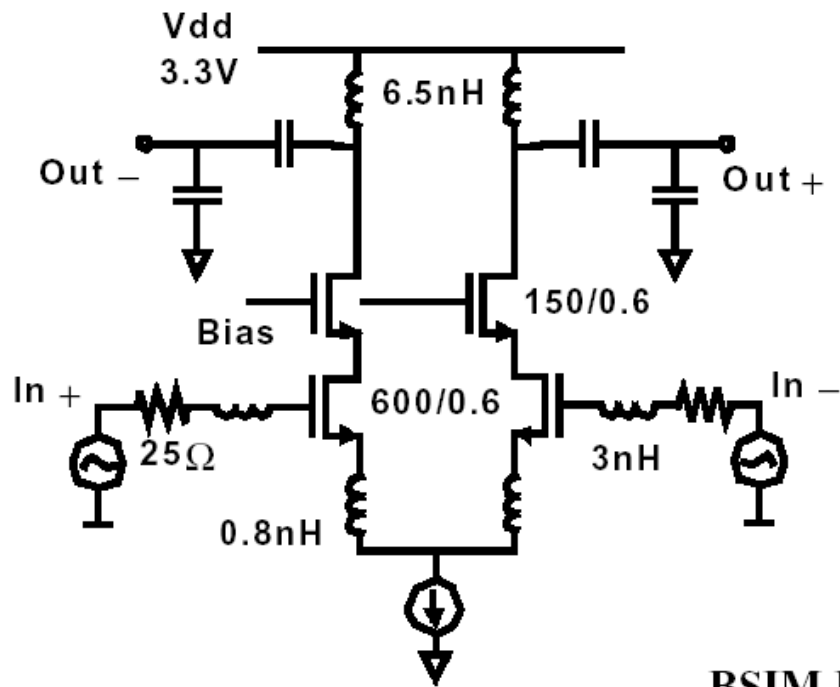


24-finger  
 240/0.35 NMOS  
 $V_{gs} = 0.9 \text{ V}$   $V_{ds} = 2 \text{ V}$

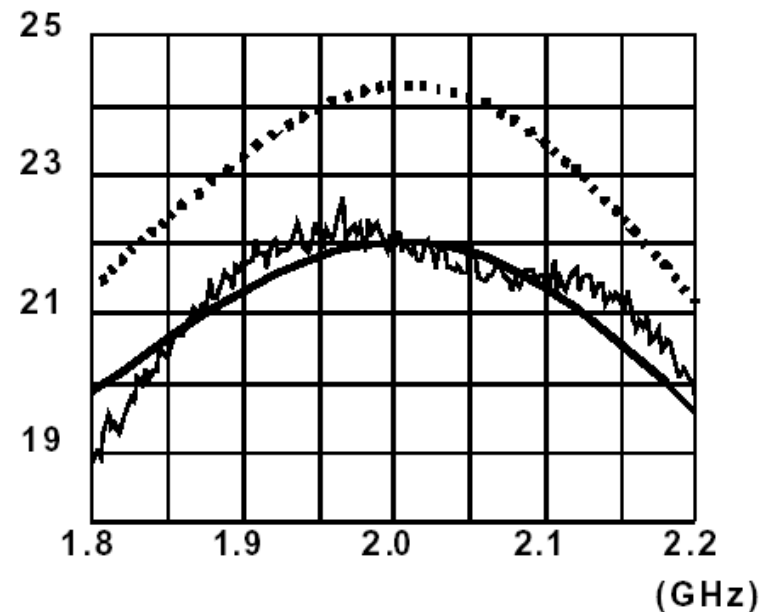


# Circuit Level Verification of RF Model

## LNA design with $0.6\mu\text{m}$ CMOS technology



Voltage Gain (dB)

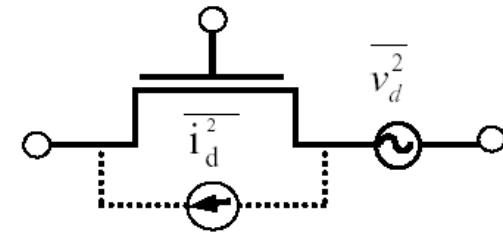
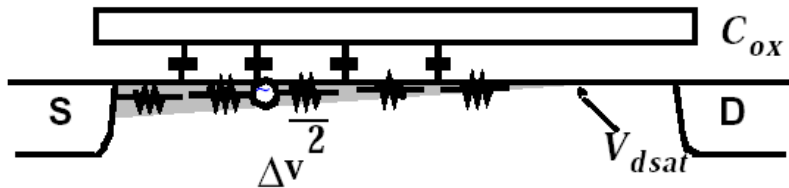


— BSIM RF  
..... BSIM3v3  
— measured



# Holistic Thermal Noise Model [1]

- Combine channel thermal noise model and noise partition model to unifies the induced gate noise and channel noise



$$\overline{v_d^2} = \int \overline{\Delta v_d^2} = 4kTB \int dR$$

$$= 4kTB \frac{V_d}{I_d}$$

$$\overline{i_d^2} = \overline{v_d^2} g_{ds}^2$$

$$= 4kTB \frac{V_d}{I_d} g_{ds}^2$$

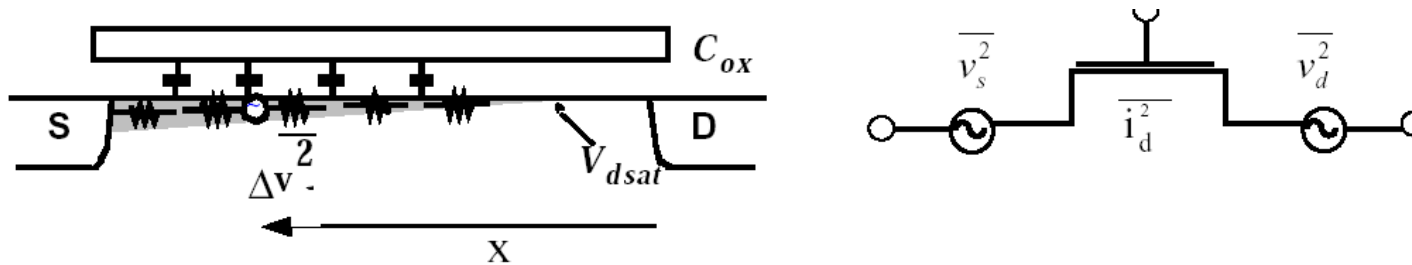
$$\frac{V_d}{I_d} \equiv \frac{V_{dsat}}{I_{ds}} \quad \text{in saturation}$$

$$\equiv \frac{V_{ds}}{I_{ds}} \quad \text{in triode}$$



# Holistic Thermal Noise Model [2]

## Channel noise amplification by front/back gate



$$\Delta i_d = \Delta v (g_{ds} + g_{mx} + g_{mbx})$$

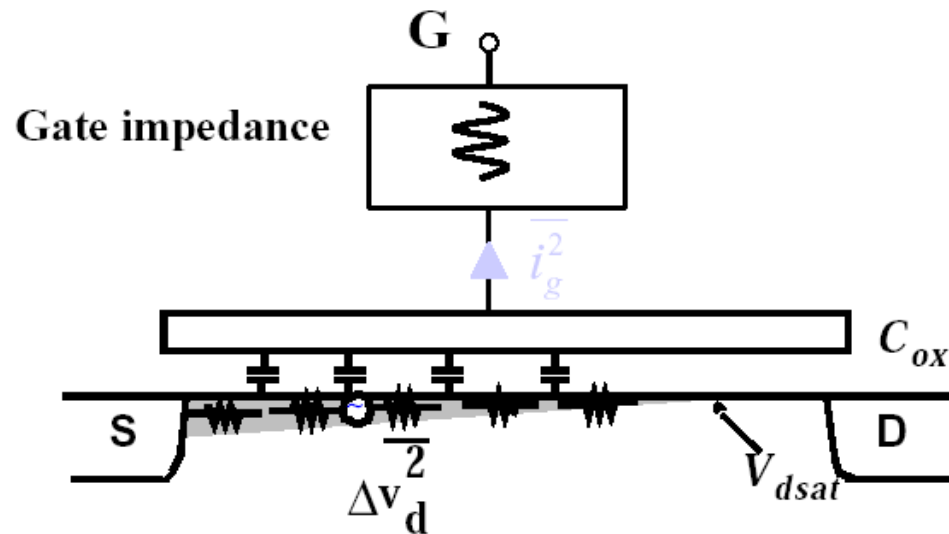
$$\overline{i_d^2} = \overline{v_d^2} (\beta g_m + \beta g_{mb} + g_{ds})^2$$

$$= 4kTB \frac{V_d}{I_d} (\beta g_m + \beta g_{mb} + g_{ds})^2$$



# Holistic Thermal Noise Model [3]

## ■ Unification of channel noise and induced gate noise

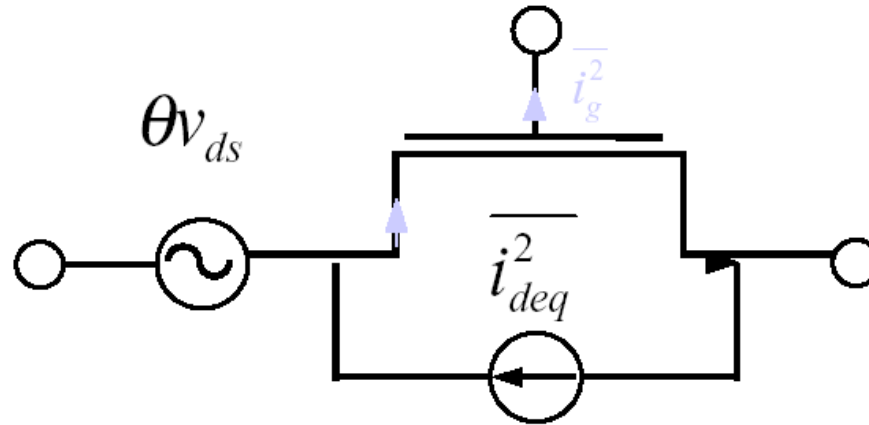


- At high frequencies, the elemental channel resistance noise source will generate significant noise current through the gate capacitance.
- The induced gate noise is correlated with the channel noise



# Holistic Thermal Noise Model [3]

## ■ Noise Partition Model



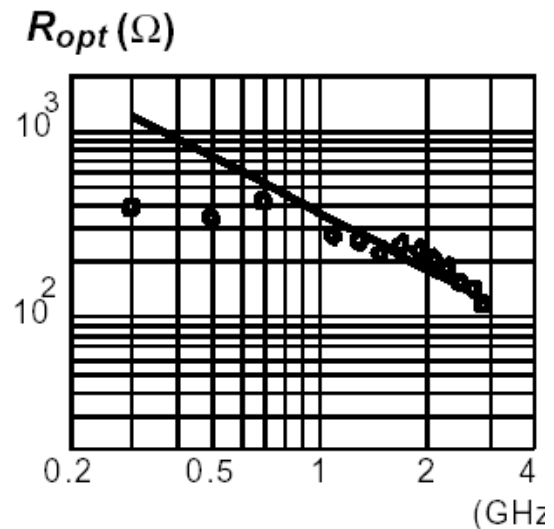
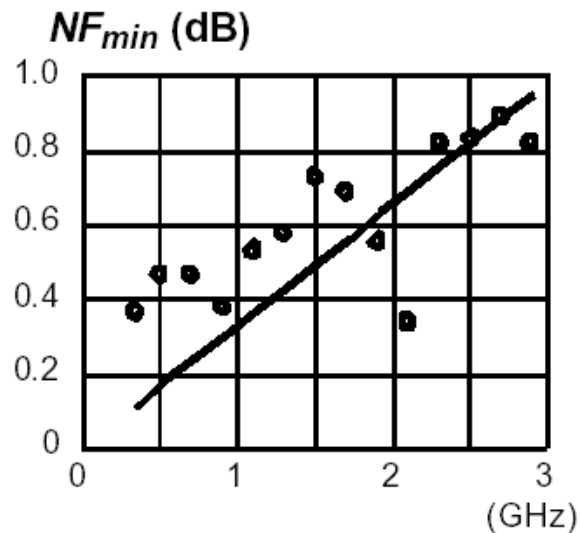
$$\overline{v_d^2} = 4kTB \frac{V_d}{I_d}$$

$$\overline{i_{d,new}^2} = \overline{i_d^2} - 4kTB\theta^2 (g_m + g_{mb} + g_{ds})^2 \left(\frac{V_d}{I_d}\right)$$

The total noise can be partitioned into two parts to model induced gate noise



# Verification of Holistic Noise Model [1]

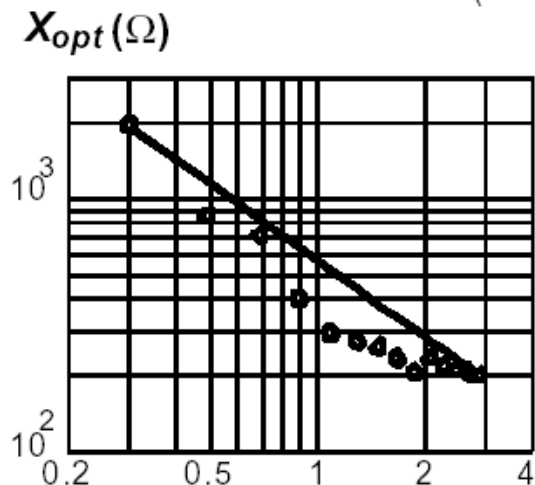
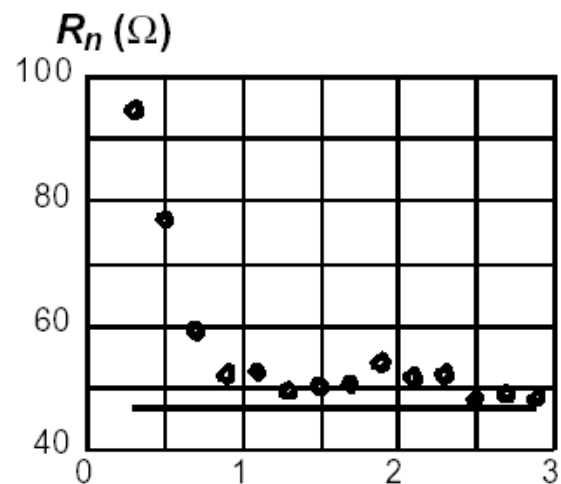


○ measurement  
— BSIM RF

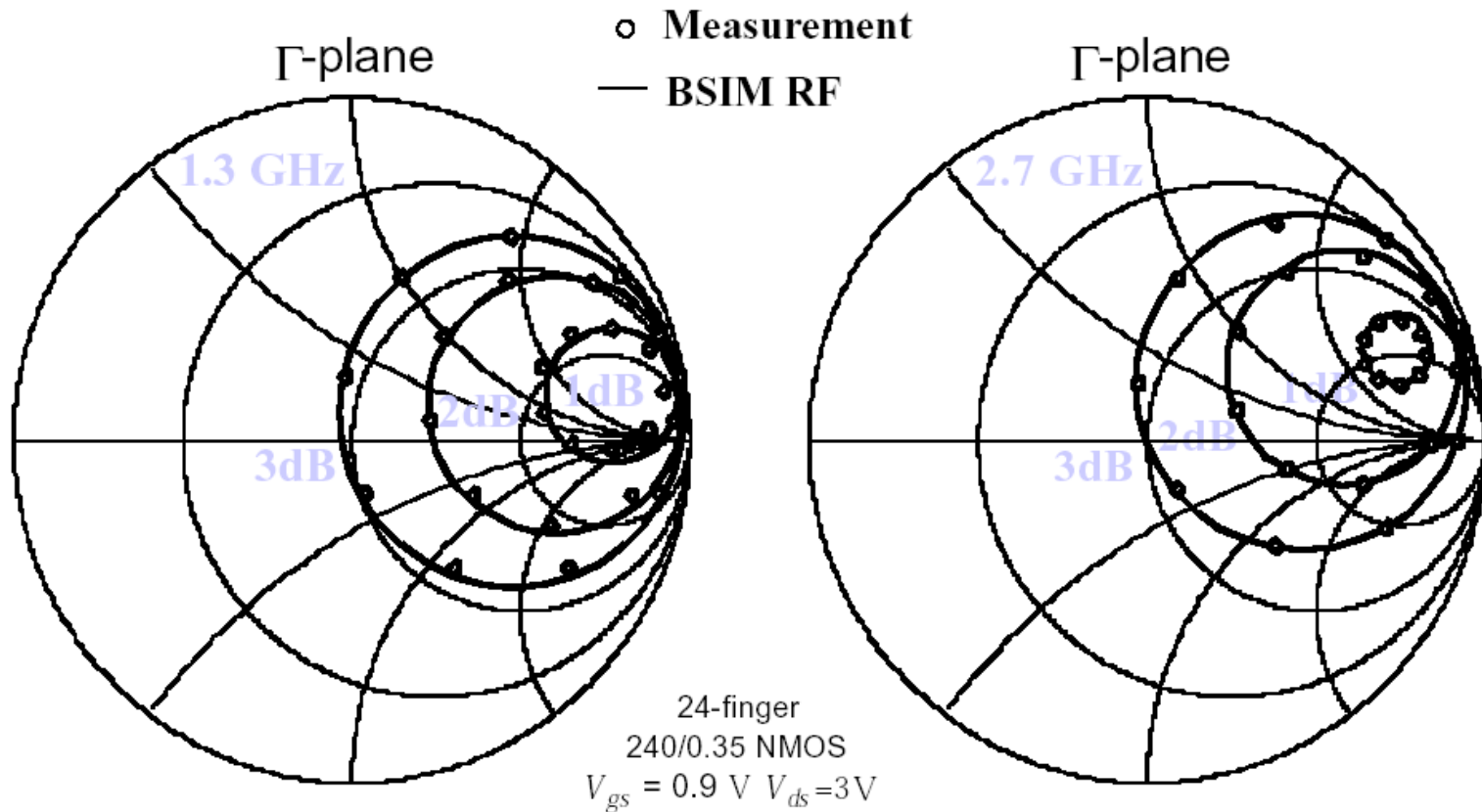
$R_g = 9.5 \Omega$   
 $R_{subd} = 50 \Omega$

..

24-finger  
240/0.35 NMOS  
 $V_{gs} = 0.9 \text{ V}$   $V_{ds} = 3 \text{ V}$

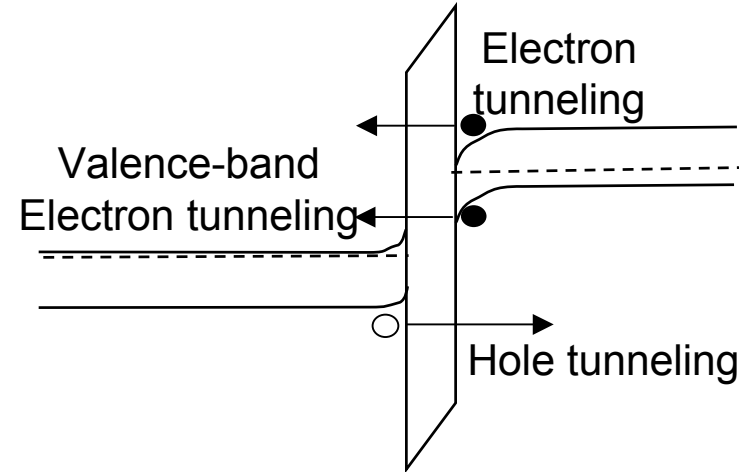
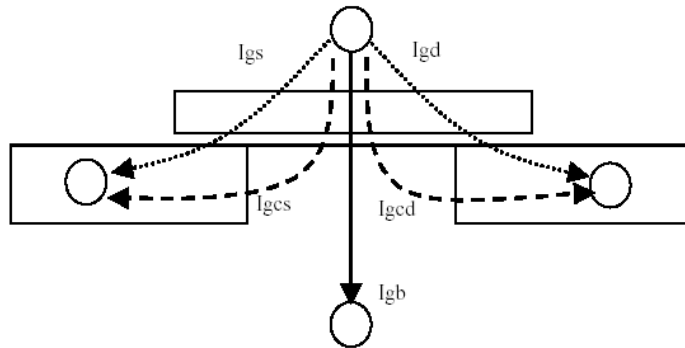


# Verification of Holistic Noise Model [2]

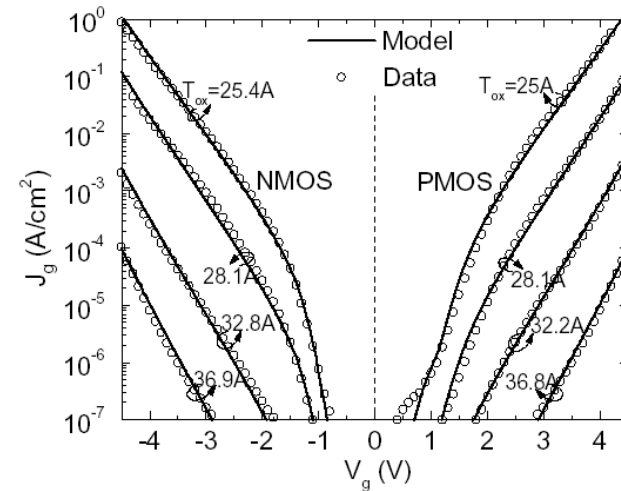
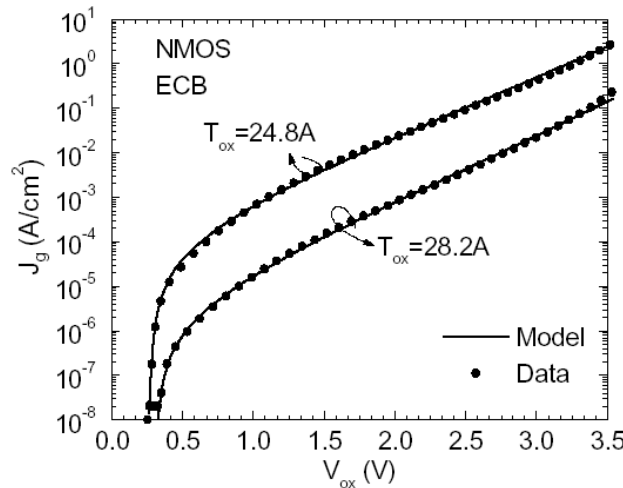


# Gate Tunneling Model

## Gate current flow

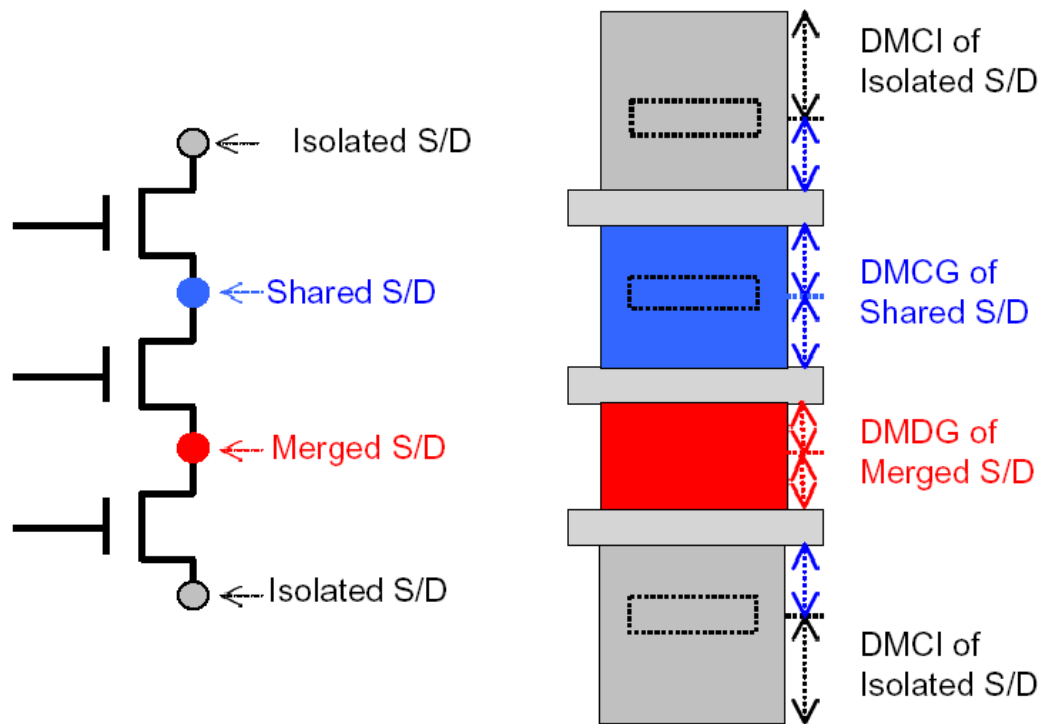


## Verification



# Layout dependent parasitic model [1]

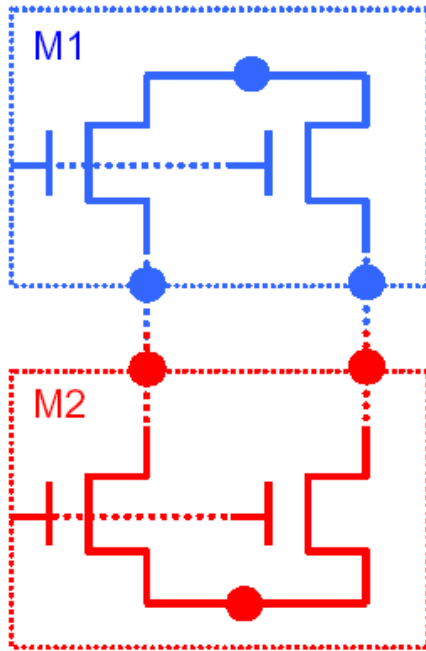
- Series/cascode connections: isolated, shared, and merged



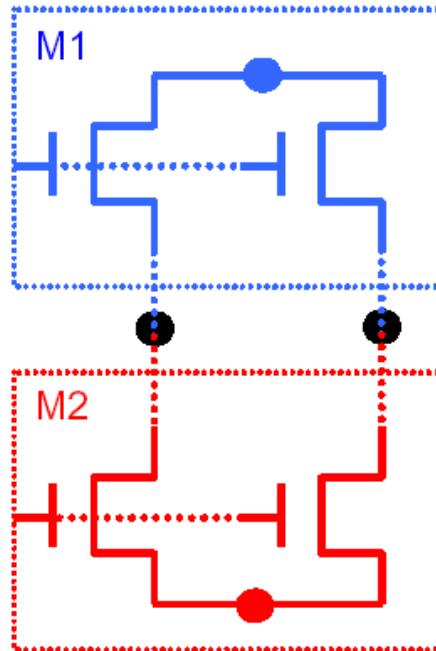
# Layout dependent parasitic model [2]

## ■ Example: Combination of Series/Parallel Connections

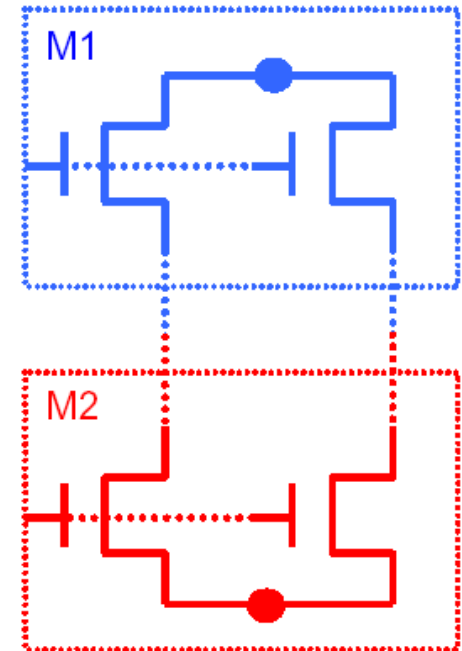
M1 & M2 isolated



M1 & M2 shared



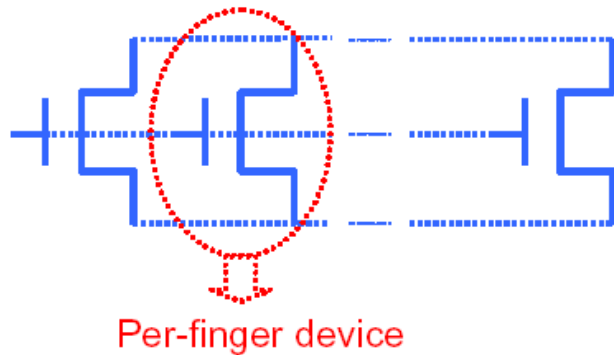
M1 & M2 merged



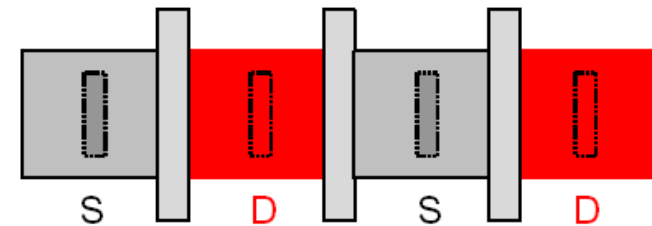
# Layout dependent parasitic model [3]

## Multi-finger/parallel devices:

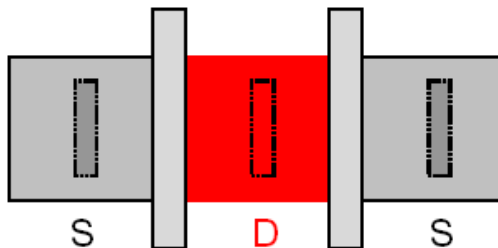
$NF$  (number of fingers) per-finger devices in parallel



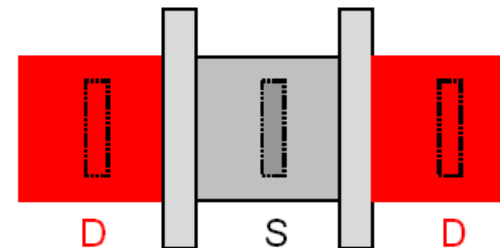
$NF=Odd$ , MINSD is not needed



$NF=Even$ , MINSD==0



$NF=Even$ , MINSD==1



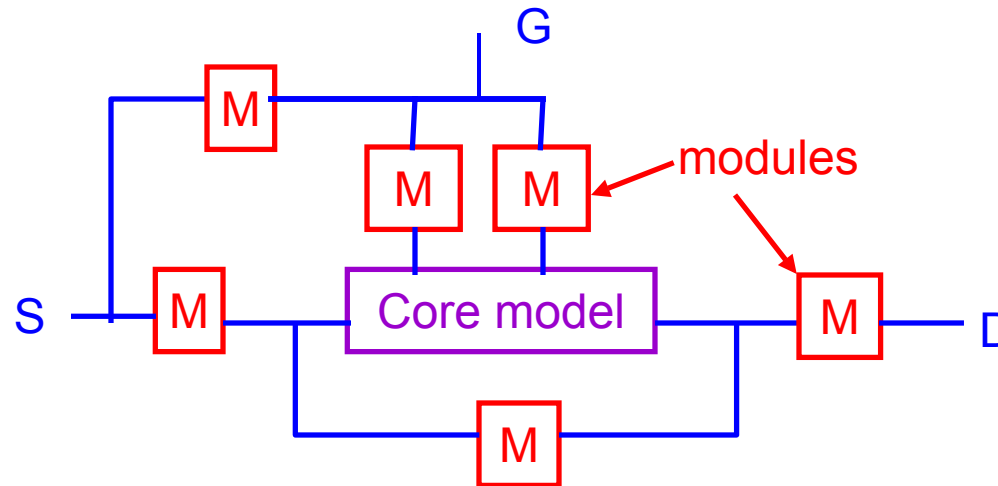
# Future BSIM direction (some thoughts)

- Have to catch up with the fast technology development
- More closely integrated to the CAD environment
- Development a fast model development platform
- Be the “Operating System” of the underlying hardware
- A more “open-source” like architecture
- Really address the issues of statistical modeling



# Model Modularization

- Model should be modularized



- The core model should be simple and represent the ideal device with nice behavior
- Not all modules are required in most simulation



# Model Modularization

- Much easier to add new effects (like LDD) and adopt to new technology
- Much easier to debug and maintain
- Allow better team management
- Provide a sustainable modeling environment
- Trade-off: more internal nodes maybe created leading to slower simulation time ( order of  $n^{1.4}$  )



# Summary

- The BSIM models follows the basic Meyer model to allow design compatibility
- BSIM4 provides a more unified solution to most device physics in current technology
- There is no perfect model, but tradeoffs to address different needs
- Modeling has been developed in an isolated fashion with the software engineering world
- Probably it is time to re-think the position of compact modeling and how it fits to the big picture

