Automatic Generation of RF Compact Models from Physics-Based Device Simulation

Serge Luryi and Andrea Pacelli

State University of New York at Stony Brook
How is RF modeling done traditionally?

Fitting microwave data...
...to a pre-conceived model

frequency: 0.5 - 25.5 GHz
Traditional approach fails in at least three cases:

- miniaturization brings about new physical phenomena not accounted for by the pre-conceived model many familiar examples
- device operation is stretched into a new regime where the pre-conceived model does not work e.g., ultra-high frequency, etc.
- one deals with the new device structure where device physicists have not done their homework example: RST devices
Goals of the Project

• Develop techniques to derive circuit models whose topology is \textit{a priori} unknown
• Abandon pre-conceived RF models
• Extract models from simulator \textit{solution files}
  
  ➢ Internal \textit{fields}, such as $n(x)$, $p(x)$, $V(x)$, $J(x)$, $T_e(x)$ ...
  
  discretized on a large grid
Generation of Lumped Elements pattern recognition problem?

When does the equivalent topology change as the device parameters are varied continuously?
How do GENERATORS emerge?

FET style

\[ I = g_m V_G \]

Bipolar style

\[ I = \alpha I_B \]
Example: let us vary $R$ by external means

$$R \rightarrow R + \delta R$$

then

$$\frac{\delta I}{\delta V_R} \text{ negative !}$$

This rather general fact, that control is associated with negative impedance may guide us into identifying generators
Graphical Illustration

normal case

complications
Variational Impedance
(gate voltage varied)

\[ \delta V_G \]

\[ \frac{d(\text{grad } F)x}{d(je)} \text{ for } V_g = 2v + dv \text{ (}= 0.05v), \text{ } V_d = 1.5v = \text{const} \]
\[ e \frac{\partial p}{\partial t} = -\nabla J_p - eR \]
\[ \nabla (e \nabla \phi) = e(n - p) \]
\[ e \frac{\partial n}{\partial t} = \nabla J_n - eR \]
Example: *pn* junction

Elements extracted from device simulation:

\[ C_n = \frac{\delta Q_n}{\delta (V_i - V_n)} \]
\[ R_n = \frac{\delta J_{vn}}{\delta (V'_n - V_n)} \]
\[ G_n = \frac{\delta J_{dn}}{\delta (V_i - V_n)} \]

Black lines: elements for minimum device functionality

Only DC solutions needed
pn junction simulation

(1st order)

Black lines: elements for minimum device functionality

2nd order: two more blocks (in neutral regions)
Example #2: Bipolar Transistor

Black lines: elements for minimum device functionality
Complex small-signal parameters

$Y_{21}$

$Y_{22}$
Example #3: Phototransistor

\[ I_2 = \beta I_1 \]

Amplified current reaches collector after delay due to the charging of emitter-base junction.
Response to light pulse

- Circuit from DC simulations

- Photogeneration is modeled by a current source in each building block
The anticipated system
(after much further work)

Device geometry (embedded)
Device simulation ("infallible")
Partitioning
Small-signal circuit (at fixed bias points)
Validation and adjustment (from measurement)
Large signal model builder
Postprocessor to device simulation

• Bring to current standards of device simulation
  😞 inclusion of non-local/hot-electron effects
  😞 automatic partitioning algorithms in 2D, 3D

• Go in step with development of device simulation art
  😊 inclusion of thermal, mechanical and magnetic effects

• Applications
  😞 critical whenever circuit topology is not a priori evident
  😞 such applications will proliferate and multiply due to miniaturization and ...
  😊 frailty of the human mind!