How to Build an SOI Compact Model Without Violating the Laws of Physics

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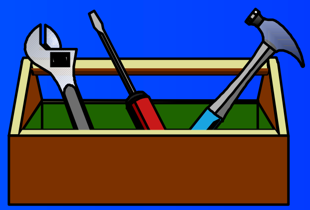

Acknowledgments

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Outline

- Model Requirements
- Methodology
- Targets
- Body Current checks
- Drain current model checks
- Implementation
- Summary

Model Requirements

- High Speed Logic
  - Requires Concurrent Design
    - Requires Model before Silicon is available
- Narrow Width Effects are Critical
- Long Channel, Analog Applications are important but not critical

Methodology

- Start with a model fit to "good" silicon
  - Global model for L and W scaling
- Generate a set of device targets
- Adjust the model to:
  - Hit the new targets
  - Preserve the IV "shape"
  - Remain physically reasonable

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Targets -- General

- Vdd -- Nominal operating voltage
- Delta L
- Delta L tolerance
- Delta W
- Tox - physical
- Tox - electrical

Targets -- Body Currents

- Diode forward current
- Diode reverse current
- Peak Impact Ionization current (as a fraction of drain current)
- Gate tunneling current - inversion
- Gate tunneling current - accumulation

Targets -- Threshold Voltages

- Linear and Saturated Vt L=long
- Linear and Saturated Vt L=nominal
- Linear and Saturated Vt L=minimum
- Body Effect L=nominal
- Temperature Sensitivity of Vt (mV/^{o}C)

Targets -- Drain Currents

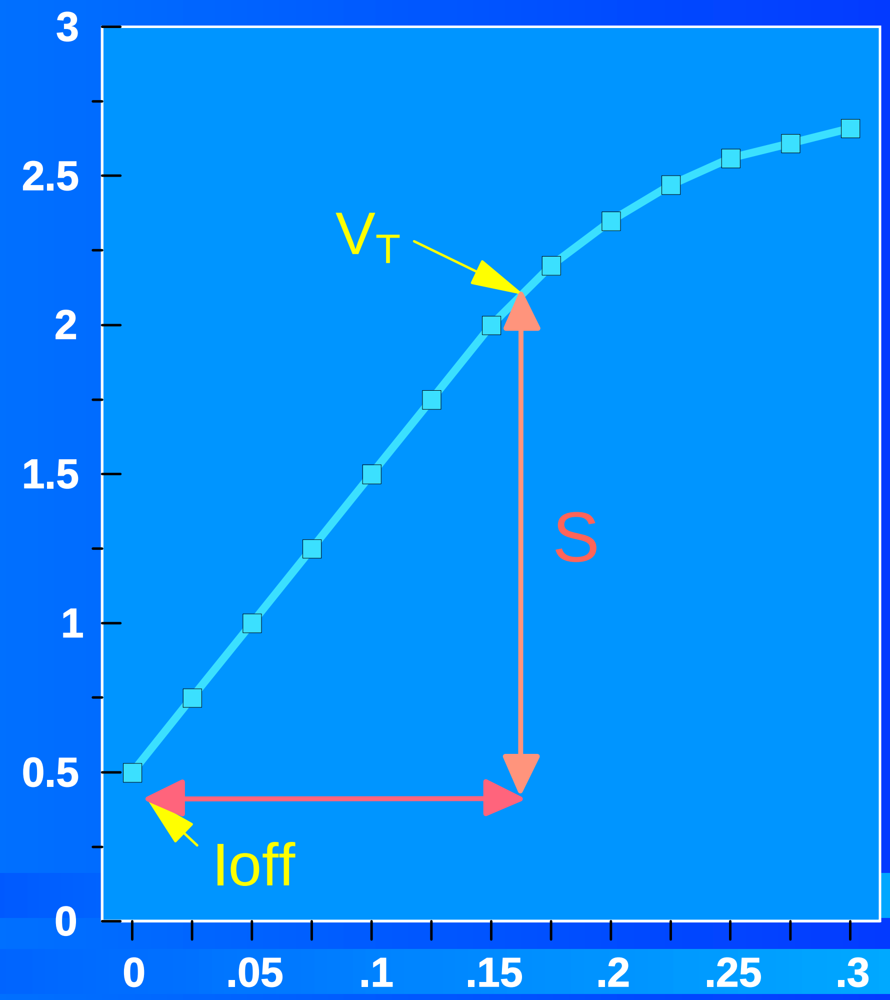
- Ion L=nominal & L=minimum
- Ioff L=minimum & L=nominal
- Linear current L=nominal
- Linear current L=minimum
- Switching current L=nominal
- Temperature Sensitivity of Ion
- Temperature Sensitivity of Linear Current
- Temperature Sensitivity of Ioff

Targets -- Narrow Channel Effects

- Linear Vt
- Saturated Vt
- Ion
- Ioff

Subthreshold Slope

- Ioff, S and Vt must all be consistent
- $110 \geq S \geq 60$ (mV/decade)
- $S_{Lmin} \geq S_{Lnom}$
- Trend of S(L) & S(T) consistent with Vt(L) & Vt(T)
- S(W) Approximately Constant



On currents

- Ion $\propto$ (Vdd-Vt)/Leff
  - Pocket implants make Ion rise more slowly than this as Leff decreases
- Ion(Weff) $\propto$ Vdd-Vt(Weff)

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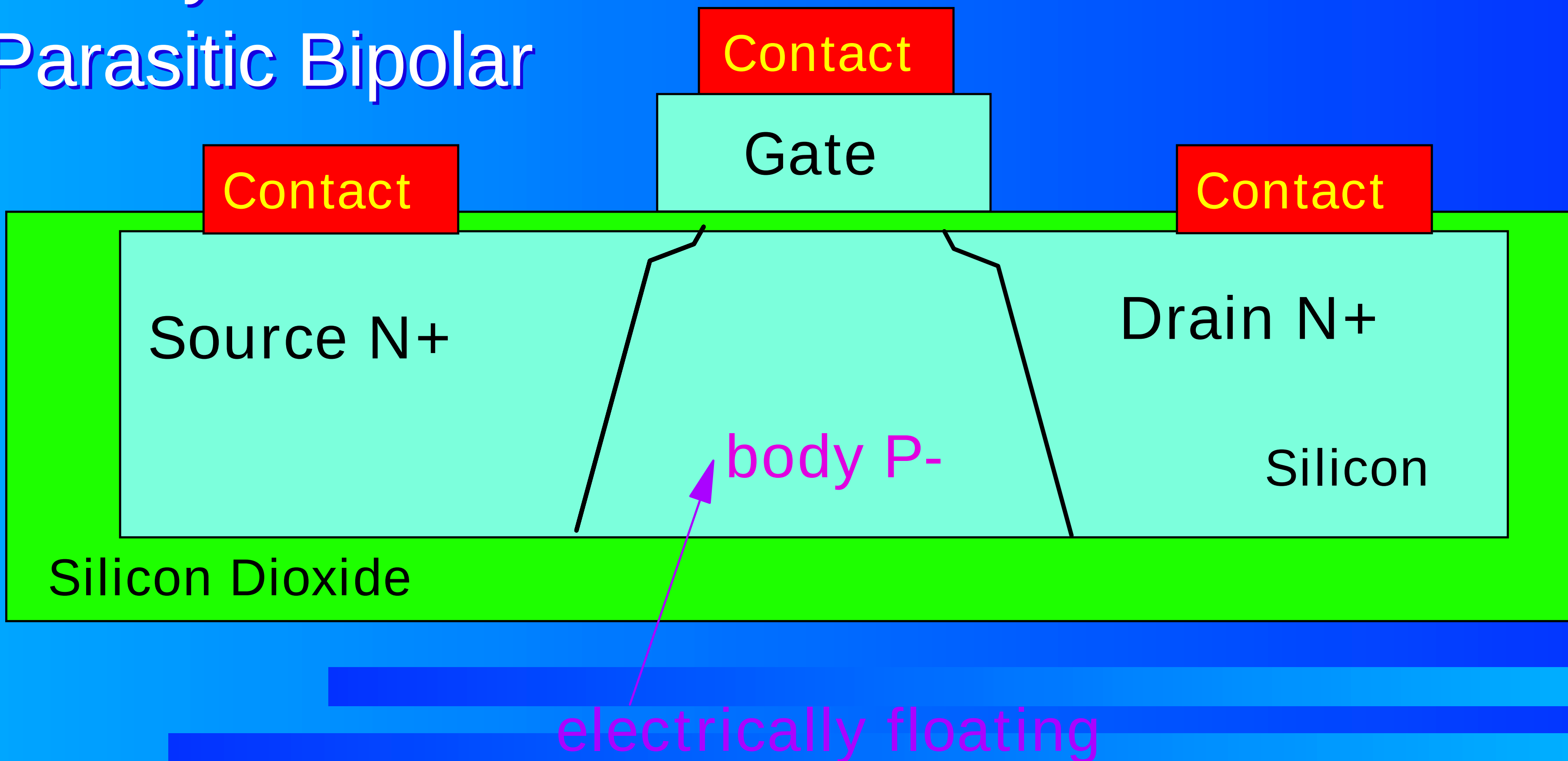
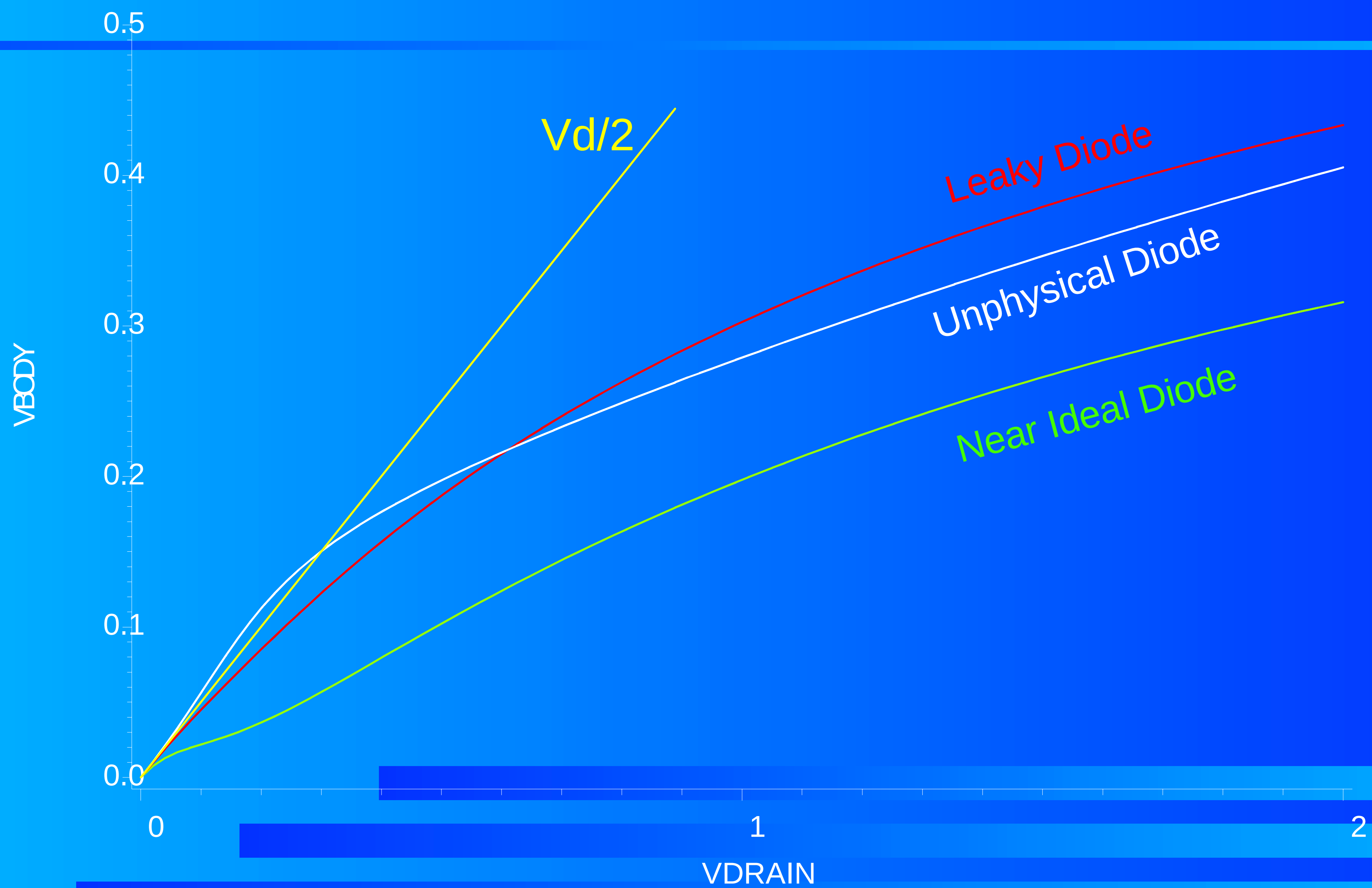
Body Voltage Controls:

- Threshold Voltage
- History Effect
- Parasitic Bipolar



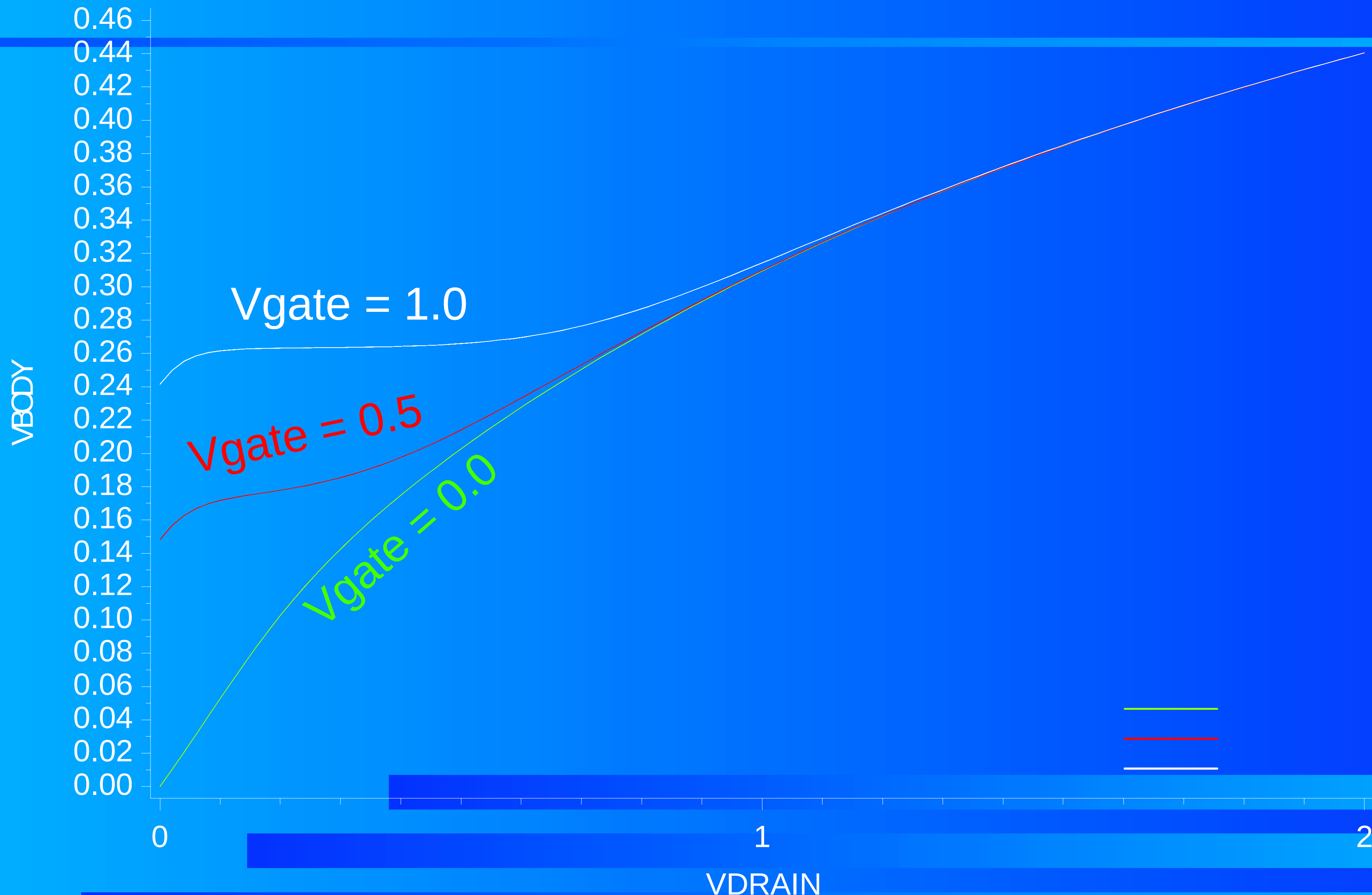
Diode only

Body voltage vs Drain voltage



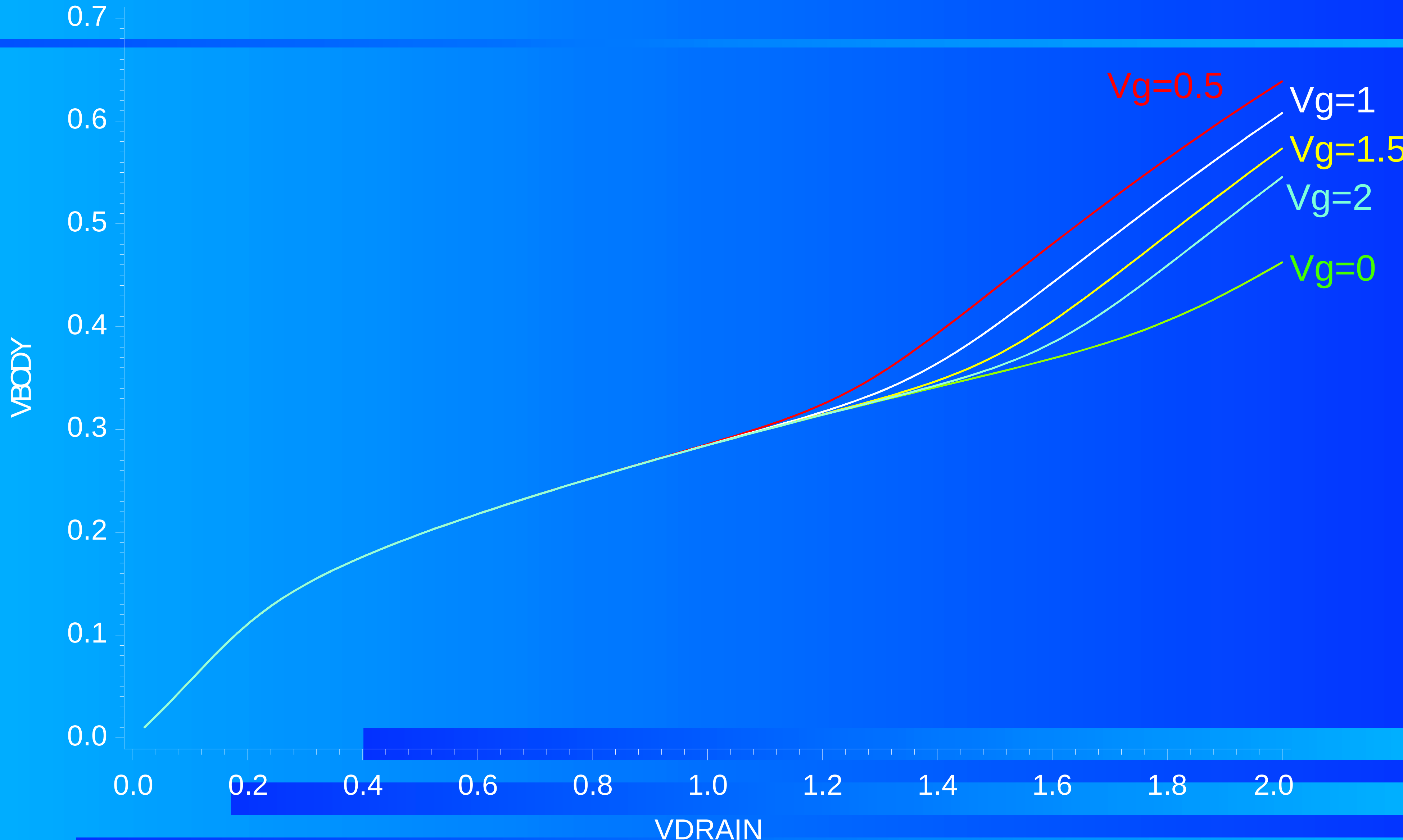
Diode and Gate currents

Body voltage vs. Drain Voltage



Diode and Impact Ionization

Body vs Drain voltage



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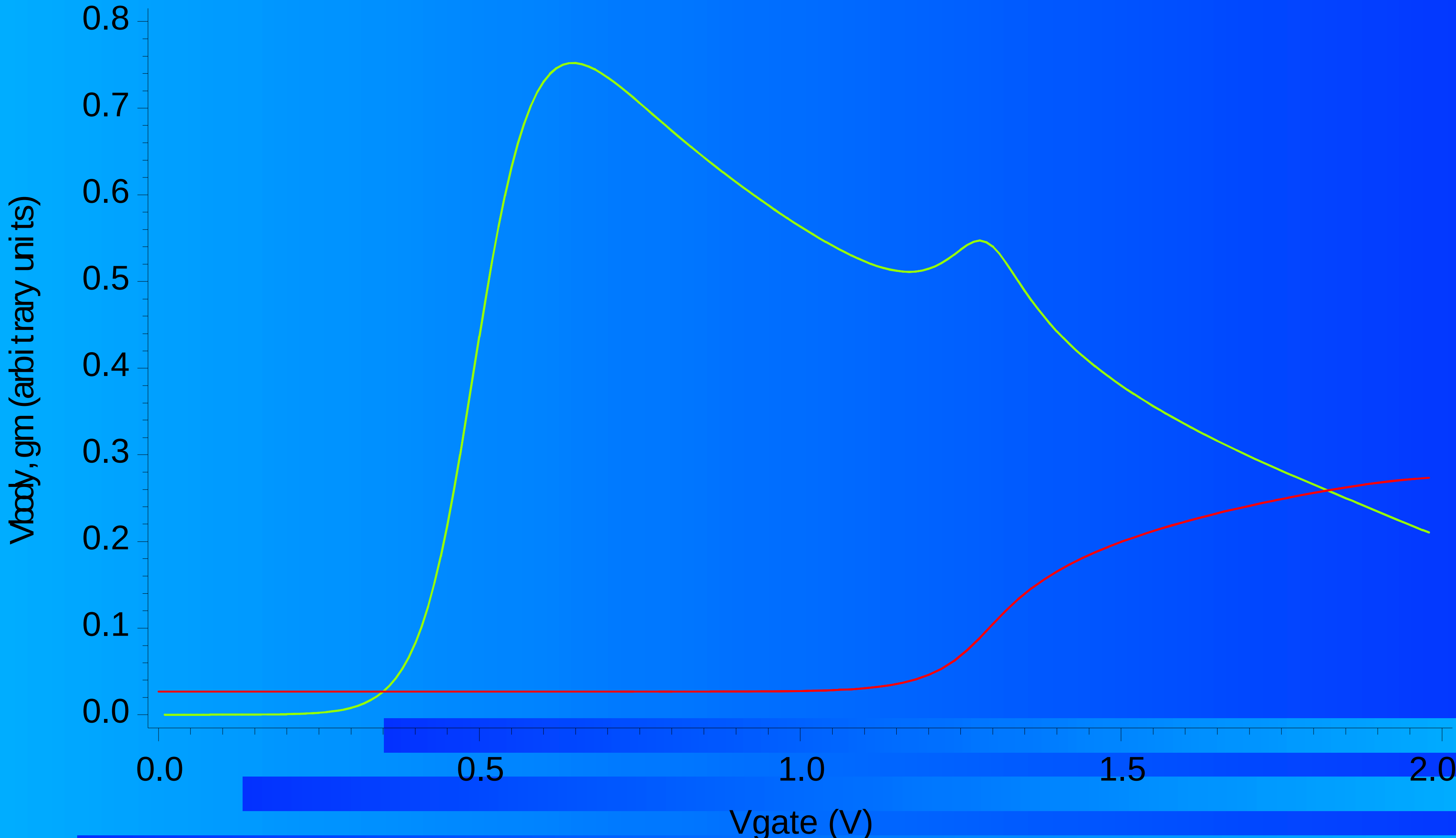
Gm, Gmbs, Gds all positive

- On long channel, linear Vg sweep gm appears negative
- gm can show a second hump due to gate current

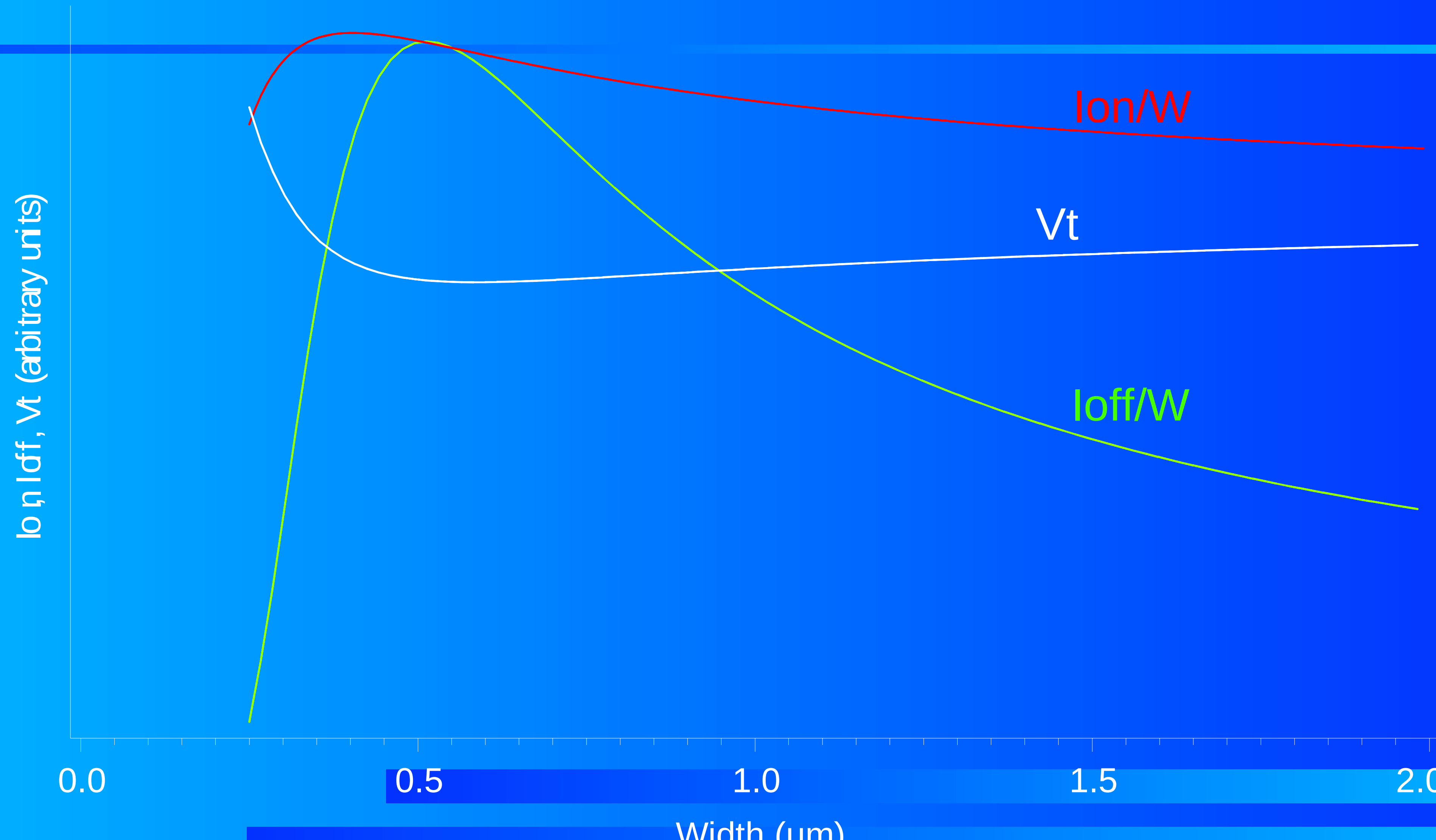
Effect of gate current on gm



Width Dependence Checks

- For very wide W
  - Vt constant
  - I/W constant
- For Narrow W
  - (Ion, Ioff, Iswitch) vs. W monotonic
  - Ion/W, Ioff/W, Iswitch/W vs W monotonic unless data says otherwise
  - Vt vs W monotonic unless data says otherwise

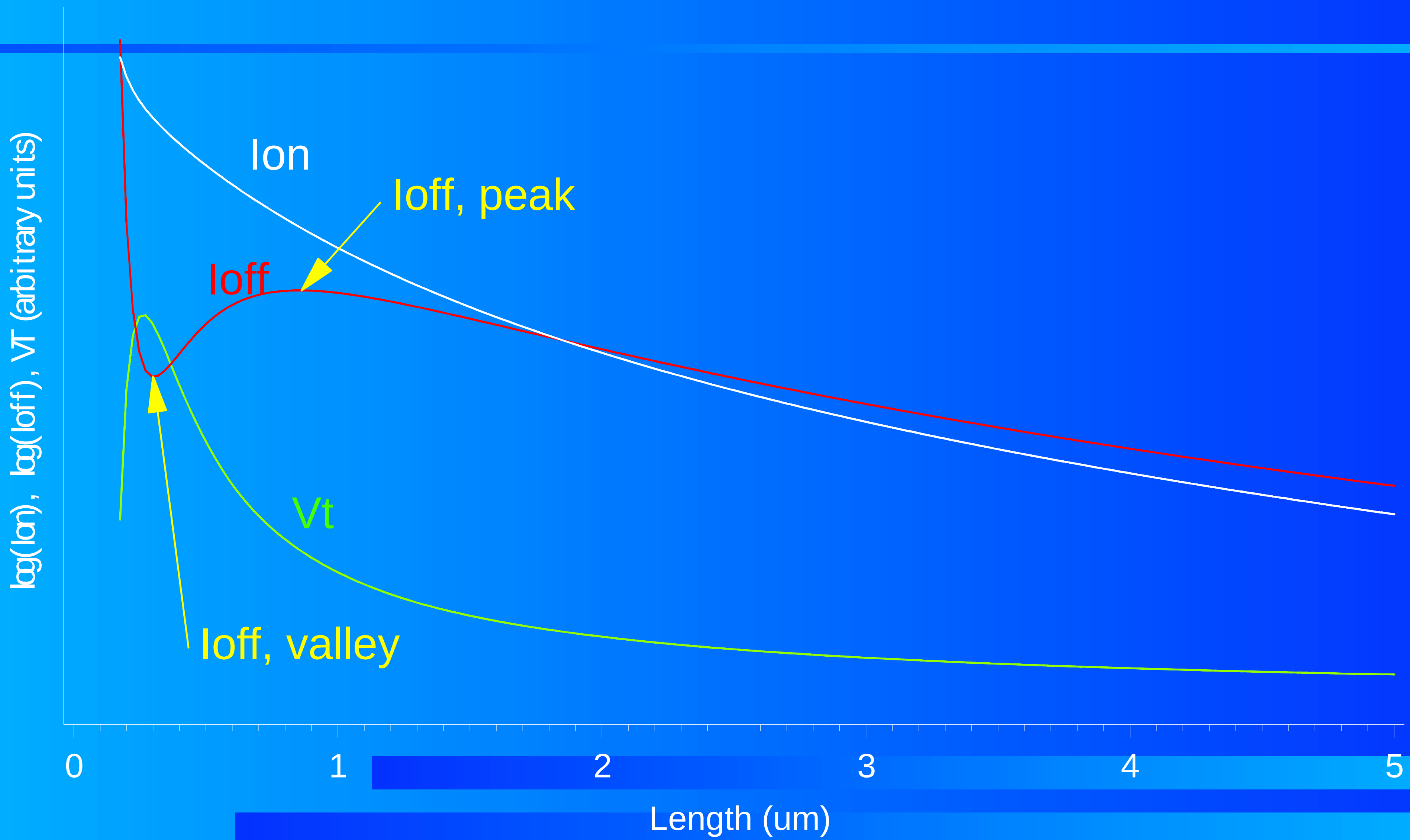
W Dependence Checks



L Dependence Checks

- Very long L
  - (Ilin, Ion) ~ 1/L
  - Vtlin, Vtsat constant
- Short L
  - No inflection in Ion curve
  - Ion $\propto$ (Vdd-Vt)/Leff
  - Ioff peak < 2*Ioff valley

L Dependence of Ioff



Implementation -- Phase I

- Targets are generated and checked
- Diode currents are adjusted to target
- Gate currents are adjusted to target
- Vbody vs Vdrain checks are performed

Implementation -- Phase II

- Vt and Id targets are fit by global optimization with constraints
  - Geometry checks
  - gm, gmbs checks
  - Vbody with Impact Ionization checks
  - IV curve shape checks
  - Minimum parameter change goal

Implementation -- Final Test

- All physicality tests are repeated on the model just before release

Summary

- This paper outlines the checks required to ensure a partially depleted SOI model built without the aid of representative hardware is physically reasonable. This allows device design and circuit design to proceed in parallel