A Unified Process-Based Compact Model for Scaled PD/SOI and Bulk-Si MOSFETs

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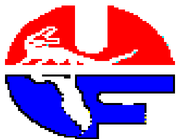
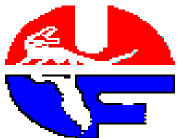
Outline

* Introduction
* Process/physics-based compact modeling
* UFPDB
* Application/demonstration
* Summary



Compact device modeling has evolved to be predominantly *empirical*:

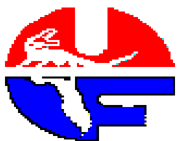
* Simple (often invalid) physics bases.
* Prodigious numbers of parameters.
* Tedious parameter-extraction methodologies.
  * Nonunique model cards.
  * No predictability.
  * No reliability.



"Moore-Like Law" for Evolutionary Compact Models*

*D. Foty, *IEEE Circuits & Devices*, pp. 26-31, July 1998.

A *revolutionary* approach to compact modeling is needed.



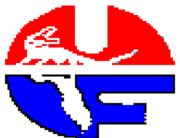
Process-Based Compact Device Modeling: Features

* Truly physics-based, with key simplifying approximations.

* Device structure-dependent, with relatively small number of parameters that relate directly to processing and physics.

* Straightforward parameter evaluation, with minimal measurement-based tuning of key parameters (like that needed for numerical device simulation).

* Predictive, enabling reliable IC TCAD, sensitivity analysis, next-generation performance projection, efficient mixed-mode device/circuit simulation, as well as reliable circuit design with strong link to technology.



Process-Based **Compact Device Modeling: Needs**

* Regional-bias (weak-, moderate-, strong-inversion, and accumulation) analyses of underlying physics.

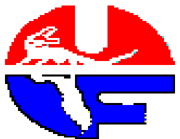
* Newton-like solutions of nonlinear equations ($\Rightarrow$ “multi-level Newton” device/circuit simulation).

* Some numerical derivatives (finite-difference approximations) for nodal-analysis Jacobian.

* Strategic use of smoothing functions (e.g., $\bar{X} = \frac{ln[1 + exp(CX)]}{C}$).

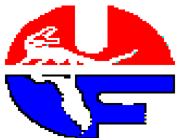
UFPDB: A Process-Based Compact MOSFET Model

* Unified for PD/SOI and bulk-Si devices.
* Charge-based.
* Retrograded (or super-haloed) channel doping.
* Source/drain extensions.
* Arbitrary (e.g., high-κ) gate dielectric.
* Strained Si-SiGe option.
* Quasi-ballistic carrier transport, with 2D field-dependent mobility.
* Short-channel (DIBL, S/D charge sharing, etc.), narrow-width effects.
* Polysilicon-gate depletion.
* Carrier-energy quantization, with exchange energy.

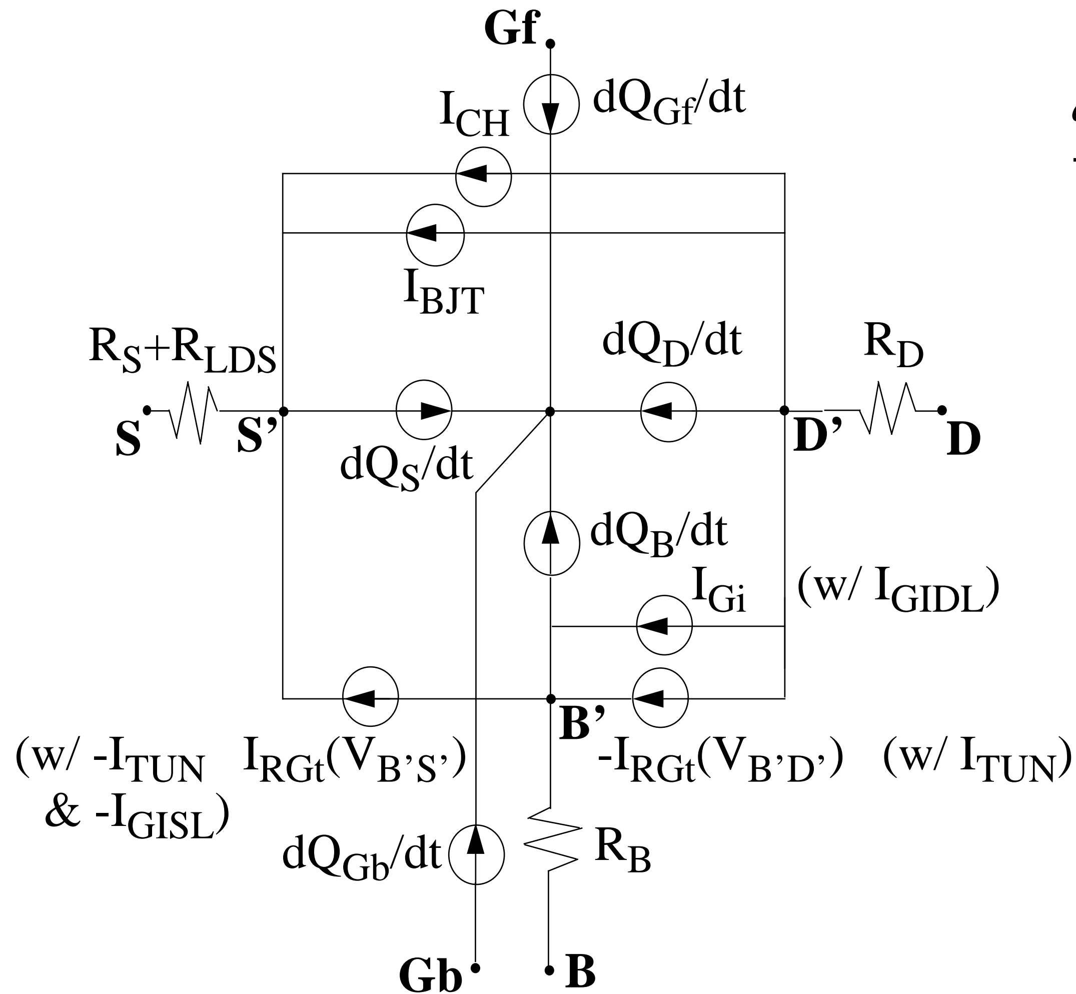


UFPDB (continued)

* Bias-dependent moderate-inversion boundaries, with spline interpolations of currents and charges.
* Parasitic lateral BJT (currents and charges), physically linked to MOSFET modeling.
* GIDL/GISL currents.
* Reverse-bias source/drain junction tunneling currents.
* Gate-body currents (w/ novel interband tunneling formalism).
* Source/drain thermal generation/recombination currents.
* Physical temperature dependences, with self-heating option.
* Physical noise modeling.
* Longer, but not excessively so, run-times.

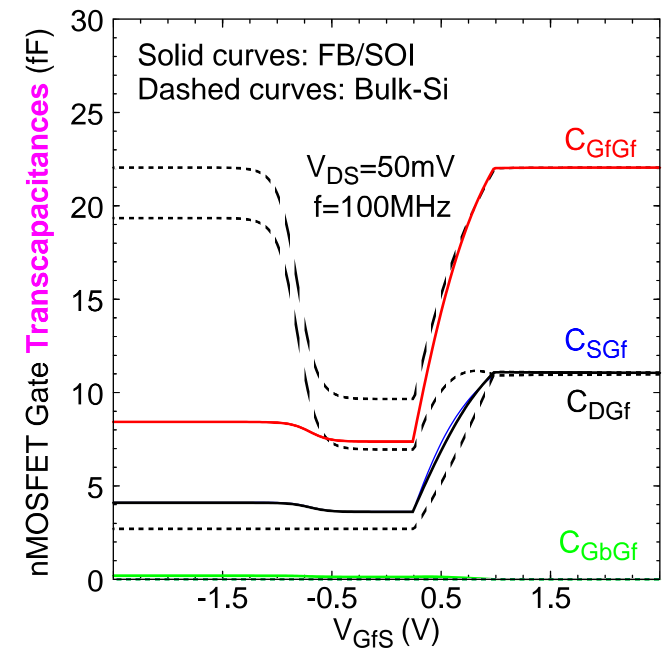


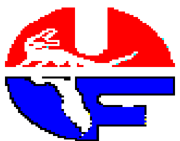
UFPDB Network Representation (in Type-I API/Spice3)



$$\frac{dQ_i}{dt} = \sum_j \frac{\partial Q_i}{\partial V_{jS}} \frac{dV_{jS}}{dt}$$

$j = D, Gf, Gb, B$





UFPDB Prediction: Transient Bipolar Effect in SOI MOSFETs*

8.0
6.0
4.0
2.0
0.0

I_{BJT} (µA/µm)

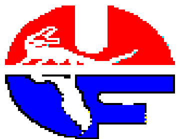
— Si source/drain
— SiGe source/drain (ΔE_g = 0.1 eV)

0 (OFF)
V_{DD}
V_{DD}
0
0
t
FB PD/SOI nMOSFET
I_{BJT}

0
1.0
2.0
3.0
4.0
5.0

Time (ns)

*M. M. Pelella, et al., *IEEE Electron Device Lett.*, May 1996.



UFPDB Unification: Two models, one small set of parameters!

B

Gf

D

S

p^+

n

p

n

n^+

n^+

p^+

p^+

p^+

t_{BOX} → ~0

Buried Oxide

body node
(4th terminal)

junction depletion charge

Q_{dSS}

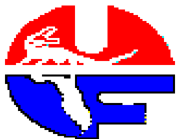
Si Substrate

Q_{dSD}

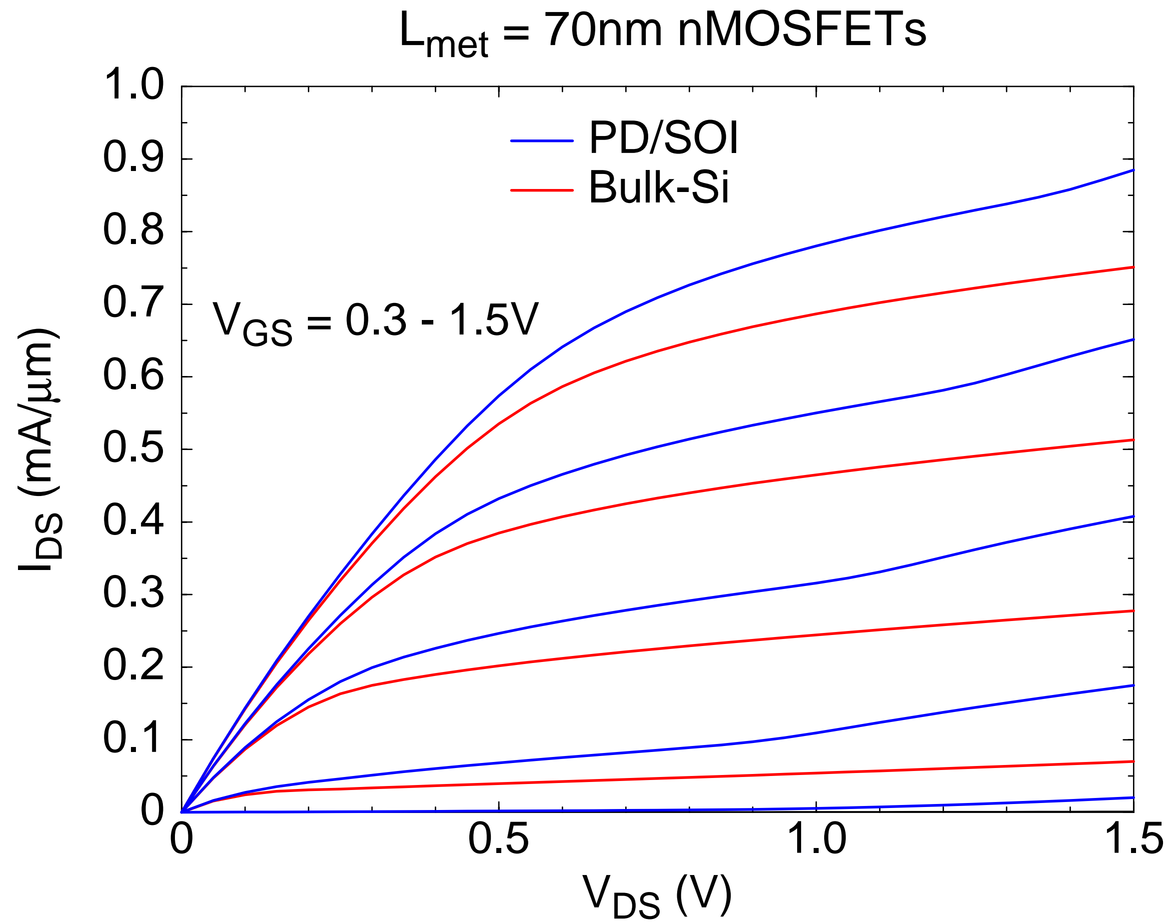
(N_{SUB} → N_{WELL})

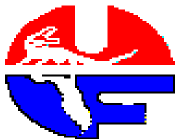
Gb

PD/SOI → Bulk-Si Option



UFPDB-Predicted PD/SOI vs. Bulk-Si MOSFET Characteristics



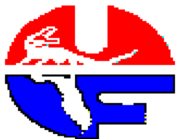


Process-Based Parameter Evaluation:
UFPDB Calibration

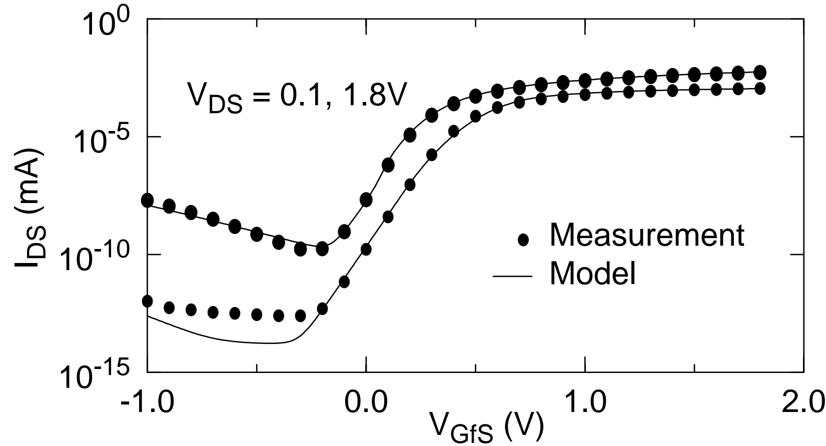
* Use knowledge of device structure/physics to define initial model card (~40 parameters, many of which are not critical); precise structure need not be known.

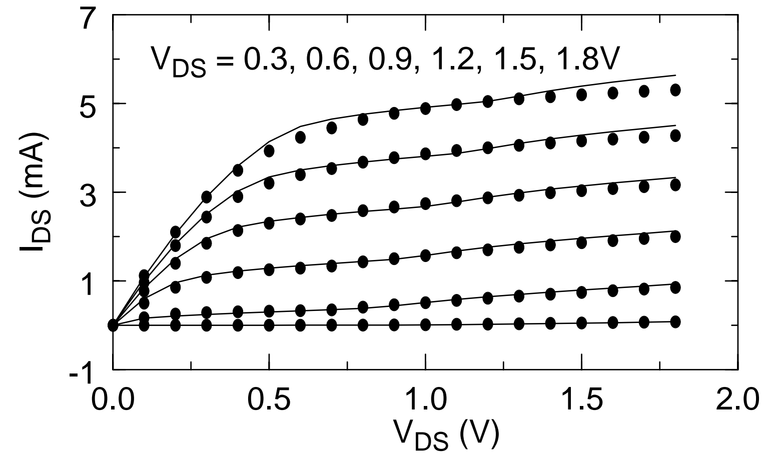
* Systematically use measured data taken from selected test devices (e.g., target- and longer-channel devices) biased in specific regions of operation (e.g., subthreshold and linear regions) to isolate and tune (~10) key parameters; copious amounts of data not needed.

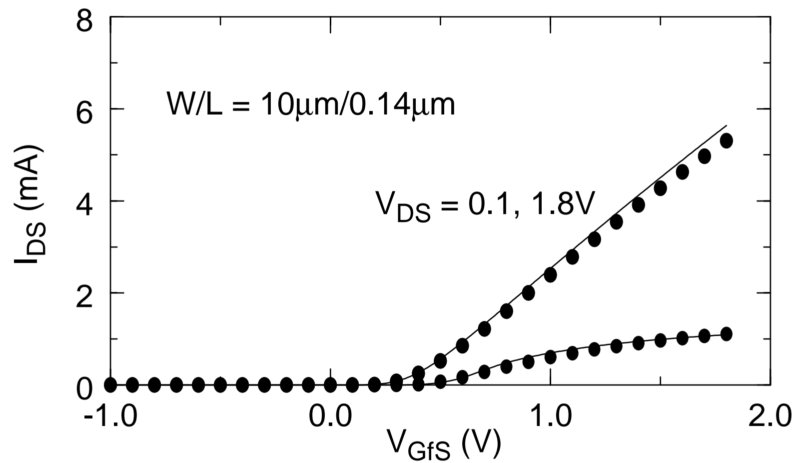
* Since parameters are process/physics-based, reasonable predictive simulations, based on initial model card, can be done when measured data is not available, e.g., in projecting next-generation performance.

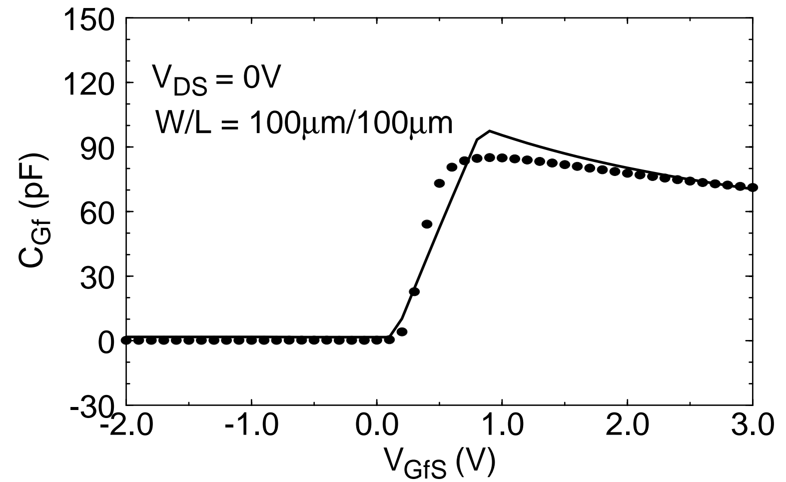


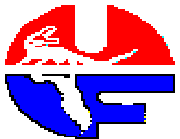
Example: 0.14μm PD/SOI nMOSFET with Floating Body











UFPDB*: Quantization and Poly Gate-Depletion Effects

FB/SOI nMOSFET (W/L = 100μm/100μm)

t_{oxf} = 2.5nm

V_{DS} = 0V

150.0
120.0
90.0
60.0
30.0
0.0

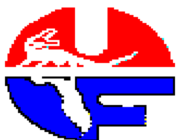
C_{Gf} (pF)

-2.0 -1.0 0.0 1.0 2.0 3.0

V_{GfS} (V)

Measured data
w/ QM and poly depletion*
w/o QM and poly depletion*

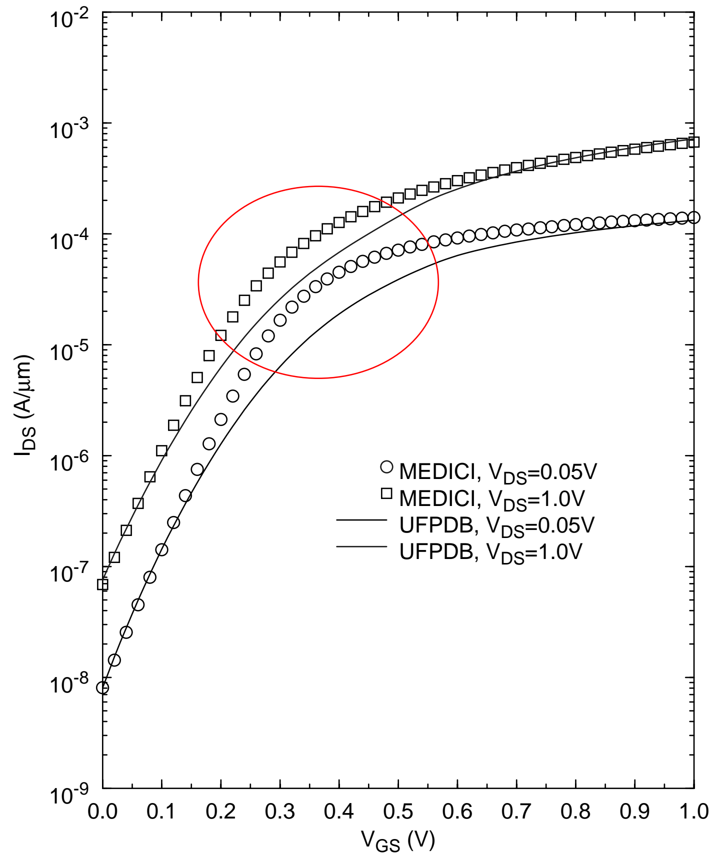
* HF AC Simulations



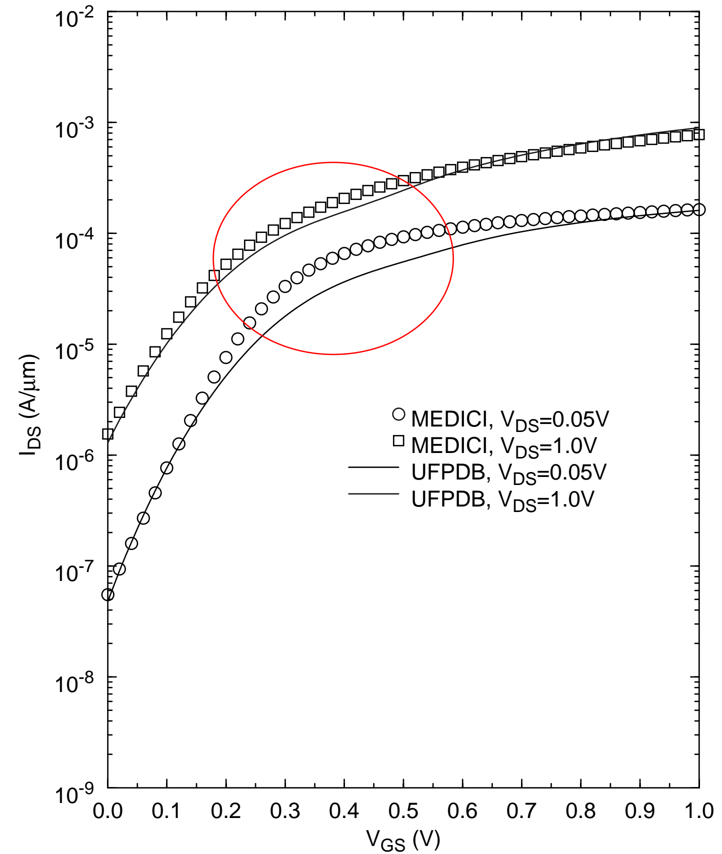
Example: Projected L_{min} Characteristics (wrt/ MEDICI)

Bulk-Si nMOSFETs

$L_{gate} = 60nm$



$L_{gate} = L_{min} = 50nm$



Calibration:

MEDICI structure

+

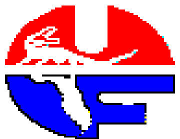
5 parameters fined-tuned.

Note:

MEDICI default mobility model for moderate V_{GS} is inappropriate.

Projection:

I_{off}, I_{on}, S predicted well.



Exemplary UFPDB Modeling

* Physical accountings for carrier-energy quantization (QM), exchange energy (EX), and the SiGe option, all of which alter the bandgap in the channel region, are linked via

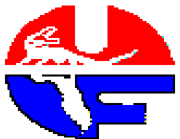
$$E_g(E_x) = E_{gi} + \Delta E_{g(QM)}(E_x) - \Delta E_{g(EX)}(E_x) - \Delta E_{g(SiGe)}$$

where E_x is the bias-dependent transverse electric field (characterized in UFPDB formalism), E_{gi} is the bulk-Si bandgap,

$$\Delta E_{g(QM)} \propto E_x^{2/3} \qquad \text{[van Dort, et al., 1994],}$$

$$\Delta E_{g(EX)} \propto E_x^{1/2} \qquad \text{[Stern, 1973],}$$

and $\Delta E_{g(SiGe)}$ is a model parameter defined by the Ge content in the strained Si-SiGe layers [People, 1986].



UFPDB-Predicted Bulk-Si vs. Si-$Si_{1-x}Ge_x$ Characteristics

L_{gate} = 60nm nMOSFETs

SiGe (w/ V_t control): **x = 0.2**

Si

V_{GS} = 0.2 - 1.0V

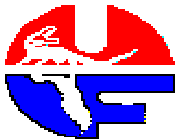
I_{DS} (mA/µm)

1.0
0.9
0.8
0.7
0.6
0.5
0.4
0.3
0.2
0.1
0.0

0.0 0.2 0.4 0.6 0.8 1.0

V_{DS} (V)

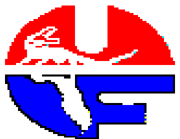
x ⇒ DEG, UO, VSAT, VO (process/physics-based model parameters)



UFPDB: V_t Control for SiGe Devices via NBL Increases

L_{gate} = 60nm MOSFETs

V_{GS} (V)										
-1.0	-0.8	-0.6	-0.4	-0.2	0.0	0.2	0.4	0.6	0.8	1.0



Exemplary UFPDB Modeling (continued)

* Physical accountings for impact ionization and quasi-ballistic transport (with velocity overshoot) are based on a simplified form of the energy-balance equation (i.e., the 2nd-order moment of the Boltzmann transport equation (BTE)):

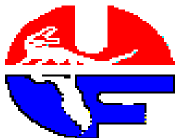
$$\frac{d}{dy}(T_c(y) - T) + \frac{(T_c(y) - T)}{(5v\tau_w/3)} = \frac{2qE_y(y)}{5k_B}$$

where T_c is the carrier temperature [defined by the kinetic energy, which defines the impact-ionization rate (α) and the carrier mobility (μ)], E_y is the electric field along the channel, and τ_w is the energy-relaxation time. With $E_y(y)$ modeled in UFPDB, the impact-ionization current is then characterized as

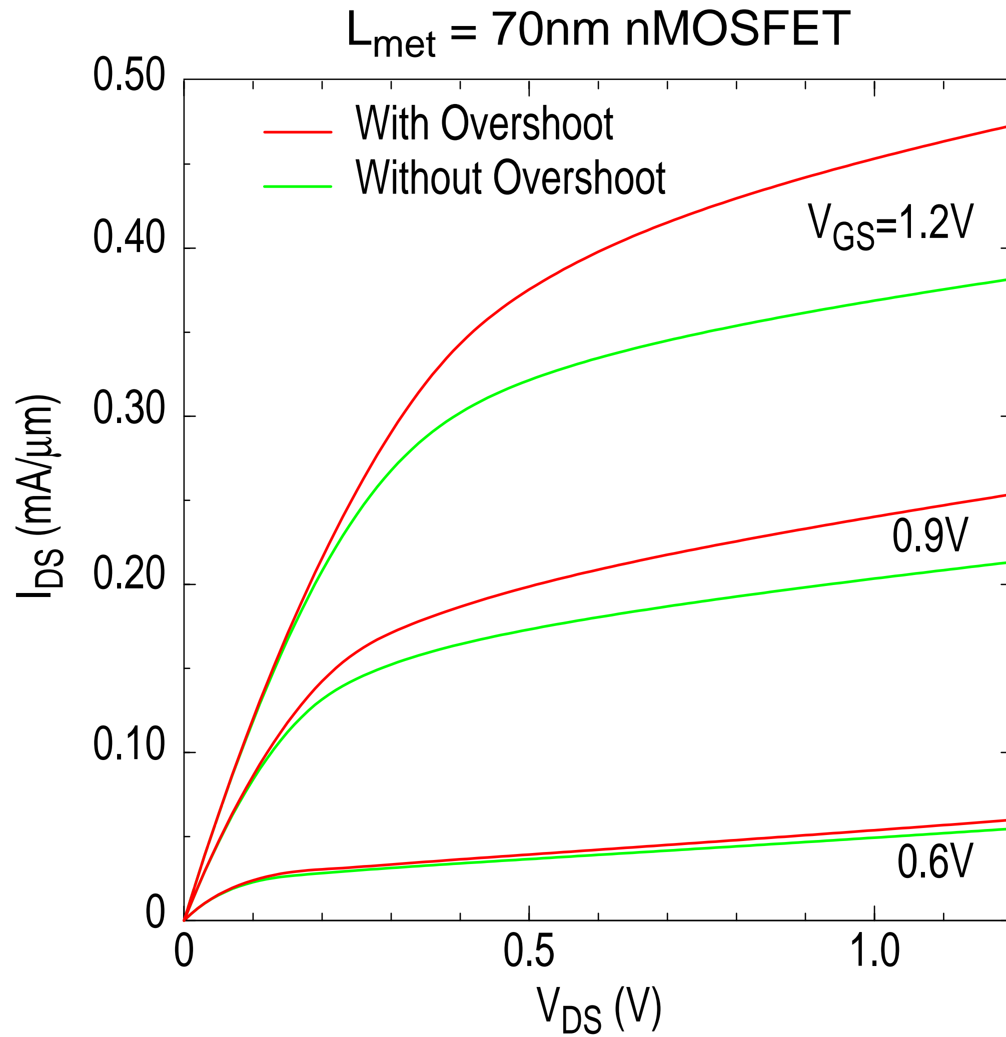
$$I_{Gi}(T_c) = \int \alpha(T_c)dy \Big|_{high-E_y\ regions}(I_{CH} + I_{BJT})$$

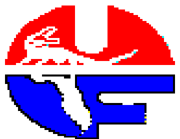
and, with the 1st-order moment of the BTE incorporated, an effective saturated drift velocity, reflecting overshoot, is defined as

$$v_{sat(eff)}(T_c) = \mu(T_c)E_y(y)\Big|_{y = L_{met}} > v_{sat} .$$



UFPDB-Predicted Benefit of Quasi-Ballistic Transport





UFPDB Application: Scaled PD/SOI vs. Bulk-Si CMOS

L_{met} = 70nm MOSFETs

I_{DS} (A/μm)

10^{-3}
10^{-4}
10^{-5}
10^{-6}
10^{-7}
10^{-8}
10^{-9}

pMOSFETs

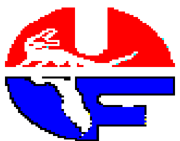
nMOSFETs

V_{DS} = 1.2V

FB PD/SOI
FB PD-V_t/SOI
Bulk-Si

-1.2 -0.8 -0.4 0.0 0.4 0.8 1.2

V_{GS} (V)



UFPDB Application: Scaled PD/SOI vs. Bulk-Si CMOS (continued)

UFPDB/Spice3-Predicted CMOS Inverter-Based Dynamic Steady-State Ring-Oscillator Delays at Room and Typical Operating Temperatures for L_{met} = 70nm FB PD/SOI and Bulk-Si Technologies

T	PD/SOI	PD-V_t/SOI	Bulk-Si
27°C	22.4ps	28.9ps	30.9ps
85°C	25.1ps	28.1ps	31.2ps

UFPDB Prediction: Floating-body PD/SOI will retain its performance advantage over bulk Si at the scaling limit (L_{gate} ~ 60nm) because of prevalent stacked logic gates and doable device design optimization, as well as high operating temperatures.

Summary

* Revolutionary, process/physics-based compact MOSFET models (e.g., UFPDB) can and should be developed for scaled CMOS.

* UFPDB utility is predictive and reliable device/circuit simulation for scaled CMOS IC TCAD as well as for circuit design, with minimal loss of computational efficiency.

* Further, UFPDB is unified for PD/SOI and bulk-Si MOSFETs, with only one small set of process-based model parameters, which can be evaluated straightforwardly based largely on device structure.

* UFPDB predicts sustained performance advantage of floating-body PD/SOI over bulk-Si CMOS to the scaling limit of both technologies (L_{gate} ~ 60nm).