Simulation Study of Non-quasi static Behaviour of MOS Transistors


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Presentation Outline

- Quasi-static operation of MOS Transistors
- Channel charge partitioning issues
- BSIM3 Non-quasi-static model
- Look-up Table (LUT) model as the “exact” QS model
- Evaluation of QS/NQS models using LUT approach
- Conclusions
Quasi-static operation of MOS Transistors
In DC case

- \( I_D = I_T \)
- \( I_S = -I_T \)
- \( I_B = 0 \)
- \( I_G = 0 \)

\( I_T \) is Transport current
In Transient case

\[ I_g = I_G + \frac{dq_g}{dt} \]

\[ I_d = I_D + \frac{dq_d}{dt} \]

\[ I_s = I_S + \frac{dq_s}{dt} \]

\[ I_b = I_B + \frac{dq_b}{dt} \]
Inversion layer charge partitioning BSIM3

\[ i_d + i_s = \frac{dq_d}{dt} + \frac{dq_s}{dt} = \frac{dq_i}{dt} \]

\[ q_d + q_s = q_i \]
\[ q_d = X_D q_i, \quad q_s = X_S q_i \]

\[ X_D + X_S = 1 \]

Charge partitioning schemes (BSIM3)

1. \( X_D = 0.5 \) and \( X_S = 0.5 \) (50/50)
2. \( X_D = 0.4 \) and \( X_S = 0.6 \) (40/60)
3. \( X_D = 0.0 \) and \( X_S = 1.0 \) (0/100)
BSIM3 NQS Model

QS assumption

\[
\frac{dQ_{ch}}{dt} = \frac{dQ_{cheq}}{dt}
\]

NQS modeling

\[
Q_{def} = Q_{cheq} - Q_{ch}
\]
\[ \frac{dQ_{\text{def}}}{dt} = \frac{dQ_{\text{cheq}}}{dt} - \frac{dQ_{\text{ch}}}{dt} \]

\[ \frac{dQ_{\text{ch}}}{dt} = \frac{Q_{\text{def}}}{\tau} \]

\[ \frac{dQ_{\text{def}}}{dt} = \frac{dQ_{\text{cheq}}}{dt} - \frac{Q_{\text{def}}}{\tau} \]
BSIM3 NQS model equivalent circuit

\[ i_D = I_D(dc) + X_D \frac{Q_{def}}{\tau} \]

\[ i_S = I_S(dc) + X_S \frac{Q_{def}}{\tau} \]

\[ \frac{dQ_{cheq}}{dt} = \frac{Q_{def}}{\tau} \]

\[ X_D + X_S = 1 \]
LUT approach

Need to calculate derivatives of the function w.r.t both the variables
LUT Approach for circuit simulations

- MOSFET is modeled as a table of terminal DC currents and charges.
- A multi-dimensional algorithm is used to interpolate the data in between the grid points.
- Implemented in a general purpose circuit simulator SEQUEL (developed at IIT-Bombay).
Simulation set-up for extracting the terminal charges
Extracting terminal charges

\[ I_x(t) = I_x(V_{BS}(t), V_{GS}(t), V_{DS}(t)) + \frac{dQ_x(V_{BS}(t), V_{GS}(t), V_{DS}(t))}{dt} \]

\[ dQ_B(V_B^0, V_G(t), V_D^0) = \frac{dQ_B(V_B^0, V_G(t), V_D^0)}{dt} = I_b(t) - \frac{I_B(V_B^0, V_G^0, V_D^0)}{dt} \]
Bulk charge extraction

\[ \frac{dQ_B}{dt} = \frac{\partial Q_B}{\partial V_G} dV_G = \frac{\partial Q_B}{\partial V_G} \left( \frac{V_{G2} - V_{G1}}{t_2 - t_1} \right) \]

\[ \int dQ_B = \left( \frac{t_2 - t_1}{V_{G2} - V_{G1}} \right) \int (I_b - I_B) dV_G \]
Transient bulk current

![Graph showing transient bulk current with different Vbs values: Vbs=-2 (brown), Vbs=-1 (blue), Vbs=0 (red). The graph includes a circuit diagram with voltage levels V_D=4.0 V, V_G=5.0 V, V_S=-2.0 V, and V_B. The x-axis represents time in microseconds (µsec) ranging from 0 to 1.]
Extracted bulk charge

![Graph showing extracted bulk charge versus gate voltage for different bias voltages. The graph plots bulk charge in $10^{-15}$ Coulombs per micrometer ($\mu$m) against gate voltage in volts (V). The lines represent different bias voltages: $V_{bs}=0.0$ V, $V_{bs}=-1.0$ V, and $V_{bs}=-2.0$ V.]}
Validation of LUT model

$V_G$  

$V_D = 4.0 \text{ V}$

$L = 2 \mu\text{m}$

$W = 1 \mu\text{m}$

Rise and fall time = 0.2 usec
Use of LUT simulator in evaluation of QS/NQS models e.g., BSIM3

• LUT model is an “exact” QS model, since no approximations are made regarding terminal currents and charges.

• Device simulation gives the “exact” NQS behaviour.
Procedure followed:

• Extract tables of terminal currents and charges using a 2-D device simulator (ISE-TCAD) => The LUT model or the “exact” QS model.
• Study terminal currents versus time for two cases (i) Vg transient, (ii) Vd transient.
• Compare the results with BSIM3 QS and NQS models.
Simulation set-up for Vg transient

\[ V_D = 4.0 \text{ V} \]

Rise and fall time = 0.2 nsec

\[ V_G \rightarrow 4 \text{ V} \]

\[ 0 \text{ V} \rightarrow \text{ transient} \]

L = 2 \mu m

W = 1 \mu m
Gate current for the Vg transient

- Input rising
- Input falling
 Bulk current for the Vg transient

Input rising

Input falling
Drain current with ISE/LUT
Drain current with LUT and BSIM3 QS

LUT (Rising input)  BSIM3 QS (Rising input)
Drain current with ISE and BSIM3 NQS

ISE (Rising input)  BSIM3 NQS (Rising input)
Simulation set-up for Vd transient

Rise and fall time=0.2 nsec

\[ V_G = 4.0 \, \text{V} \]

\[ L = 2 \mu \text{m} \]

\[ W = 1 \mu \text{m} \]
Gate current for the V_d transient

**Input rising**

**Input falling**
Bulk current for the Vd transient

Input rising

Input falling
Drain current with ISE/LUT and BSIM3

ISE/LUT

BSIM3 QS

BSIM3 NQS
Conclusions

• Use of the LUT approach as a powerful tool to evaluate QS/NQS MOSFET models
• Terminal currents for a Vg transient in QS and NQS cases are very different (when the rise/fall times are small), but for Vd transient they match closely
• BSIM3 QS model with 40/60 partitioning scheme predicts the correct QS behaviour when a Vg transient is applied
• BSIM3 QS/NQS models show difference in \( I_d \) for the \( V_d \) transient, while the exact QS/NQS results are very close.

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