

Nanotech for Investors

CROCUS Technology

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DG Crocus SA
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Crocus Boilerplate

- MRAM is the most promising new semiconductor memory technology under development.
- However, all existing MRAM implementations suffer from the same two problems: (1) an inherent instability of the storage mechanism leading to unreliability, and (2) a lack of scalability at and below 90nm.
- Crocus MRAM offers a density considerably better than all SRAM technologies, orders of magnitude improvement in write speed compared to all non-volatile technologies, an almost infinite endurance, low power, high speed, non-volatility and a simple static interface.
- These attributes makes the Crocus MRAM technology ideally suited for high density SRAM, and for all failsafe memory applications including but not limited to Battery Backed SRAM replacement, high reliability memory buffers for all applications with “context saving” requirement such as instant-on computing, network storage, routers, industrial control as well as some cellular phone applications; the common requirement for all these applications being non-volatility, fast write cycle, high density, and high reliability.
- Crocus Technologies is a VC funded new startup being spun off from the two leading French State research agencies (CEA and CNRS). With magnetic expertise second to none and 4 years of development behind it, Crocus aims to become the world leader in MRAM products and technology.
- Crocus patented architecture offers all the MRAM advantages listed above while suffering none of the downsides. Crocus extremely dense cell architecture will allow the company to market high density, high reliability non-volatile memories at speed (both read and write) comparable to mainstream SRAM.
- Crocus is implementing a mini-fab to process the magnetic layers in its products, and is engaged in active negotiations to sign an extensive joint development program and license its technology to a leading semiconductor memory company.
- Crocus recently closed its first round of financing with leading Venture firms from the US and Europe.

Jean-Pierre Braun - Intro

- Over 30 years of semiconductor and EDA experience, including 11 years as a chip designer (Thomson, National and AMI) and 7 years as a design manager (AMD, Chips and Technologies).
- Co-founder, VP and GM of Sunrise Test Systems, the leading ATPG company which was successfully sold to Viewlogic. Turn-around CEO of Escalade, a front-end EDA company which was sold to Mentor Graphics. Then interim CEO of Inapac, a Taiwanese company looking for help with its corporate strategy. Directeur General of Crocus SA since April 2006.
- Electrical Engineering degree from the Conservatoire national des Arts et Metiers. Expert sailor and enthusiastic skier.
- Jean-Pierre and his wife Annie have three children.

Market Data

The world of semiconductor memories

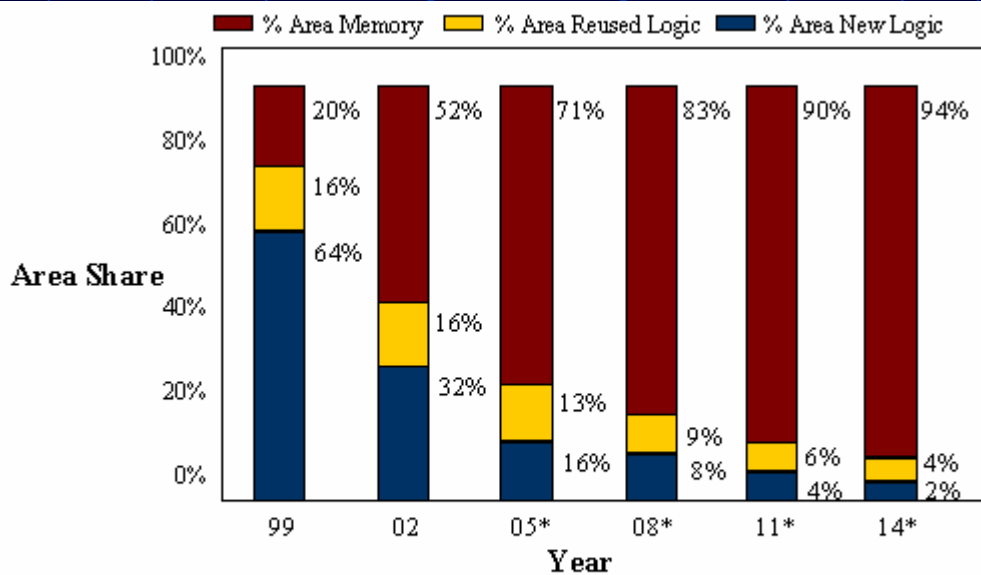
- The largest market segment in the electronics industry:
>US\$100B yearly, with double digit growth (in capacity)
- Huge “ticket of entry” for commodity game (Intel +Micron: >US\$20B for next generation Flash)
- Highly concentrated: 5 companies own 90% of the market
- Commoditization leads to killer price battles
- Home of very lucrative niches for whom can find (and fill) one.

The search for the “ultimate memory”

- High volume at low cost
 - Highly integrated ASIC and SOCs
- Mobility/ Portability
 - Low power consumption
 - Non-Volatile memory
- Instant On capability
 - Large memory size
 - Memory speed
- Ergonomics
 - Small and light terminal size
 - Components integration
- Displays
 - Low consumption
 - Non-volatile



Memory technologies face new challenges for new emerging applications



Source: SIA, ITRS 2000

* Forecast

Figure 4. System-on-a-Chip Die Area Make-Up

Existing memory technologies are not up to the challenge:

- DRAM, SRAM, Flash, cannot be embedded together
- When embedded, DRAM cell size is multiplied by 3, Flash by 8, E²PROM by 3
- Embedding memory require increase process complexity and masks levels (25 to 36) with significant cost and yield penalties

Critical requirements

Functionalities

- Non-Volatile
- High Speed write and read
- Low power consumption
- High density

Cost

- Somewhat low capital investment
- Simple manufacturing process
- Solution to multiple memory technology integration
- Compatible with existing MOS logic manufacturing infrastructure

MRAM Vs other memory technologies

	Stand- alone			eNOR Flash	MRAM
	SRAM	DRAM	NOR Flash		
Cell Size	80F ²	8F ²	10-20F ²	100F ² → 16F ²	20 ->14F ²
Access time	1ns	10ns	50ns	50ns	5-10ns
Write time	1ns	10ns	10μs-1ms	10μs-1ms	10ns
Write/Erase current	1μA	100 μA	1 mA	1mA	1.5mA
Write/Erase voltage		3V	5-10V		1-2V
Stand-by current	20 μA	100 μA	0	0	0
Compatibility				eSRAM	ALL
Additional masks	0/1	5/8	4/6	11	3

A Very Dense Memory Technology

A uniquely Fast Write NV Memory

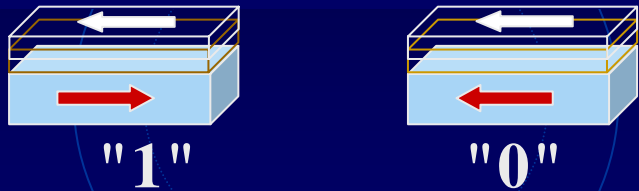
No need for high voltage

Few add-on Masks = low Add-on cost

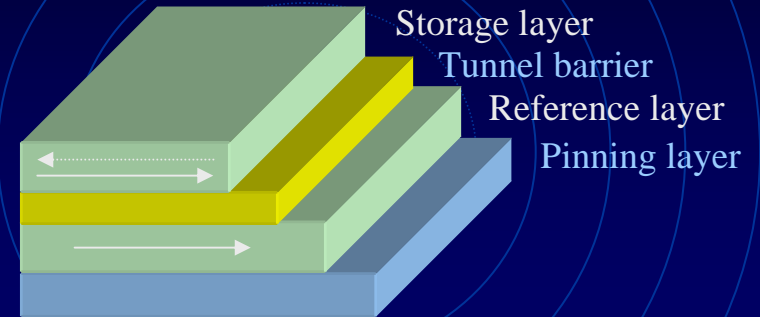
MRAM Technology

MRAM basics

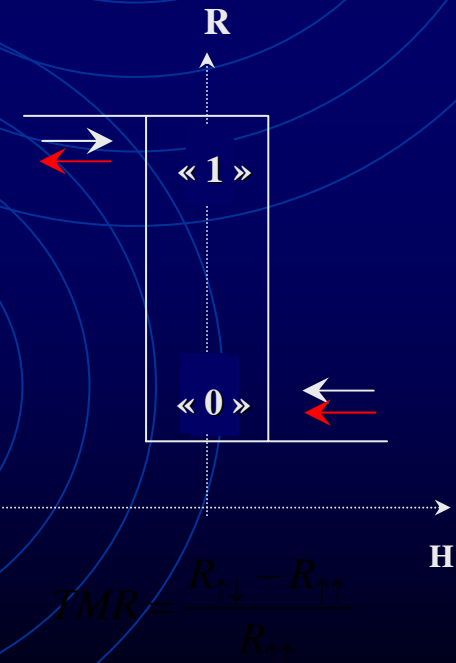
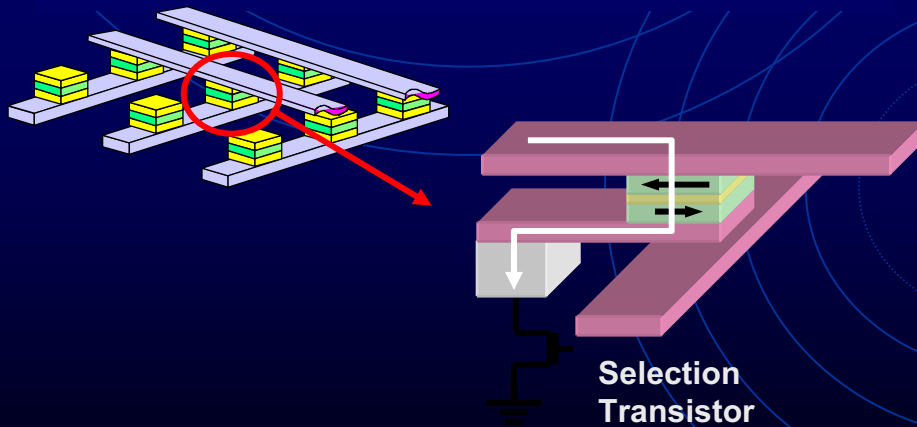
Store data by the direction (parallel or antiparallel) of magnetic layers in Magnetic Tunnel Junction (MTJ)



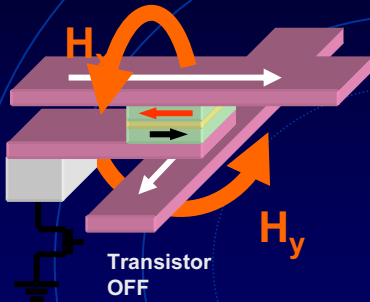
Magnetic Tunnel Junction (MTJ)



Read data by sensing the cell resistance and comparing to a reference cell



First Generation MRAM technology : Field Induced Magnetic Switching (FIMS)



Use current pulses to generate overlapping magnetic fields at word/bit line crosspoint

Current technology (FIMS) pursued by most competitors (Cypress, Infineon, NEC/TOSHIBA, IBM, Samsung...) presents severe drawbacks :

- ➡ Soft errors (write selectivity)
- ➡ Scalability

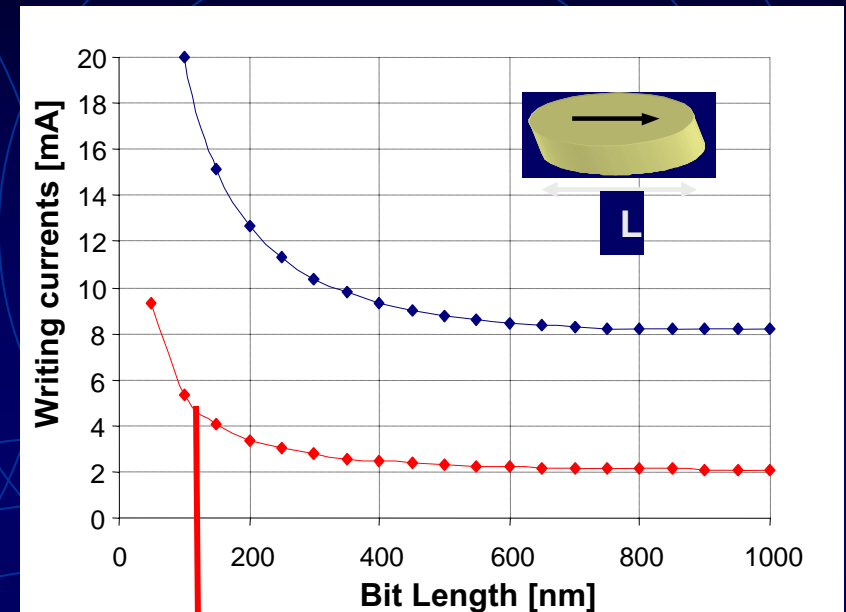
Fixes to soft errors include :

- ❖ Exotic magnetic cell shapes requiring highly expensive photolithographic equipments
- ❖ Freescale's so-called Toggle Switch, which calls for a significant penalty on power consumption

No fixes available to scalability issues (physics talk !)

All FIMS based MRAMs suffer from a major limitation resulting from their very design :

They cannot scale economically below 100nm



CROCUS

Addressed by IBM, Infineon, Cypress, Freescale,...

CROCUS Thermally assisted (TAS) writing

Crocus TAS Technology combines :

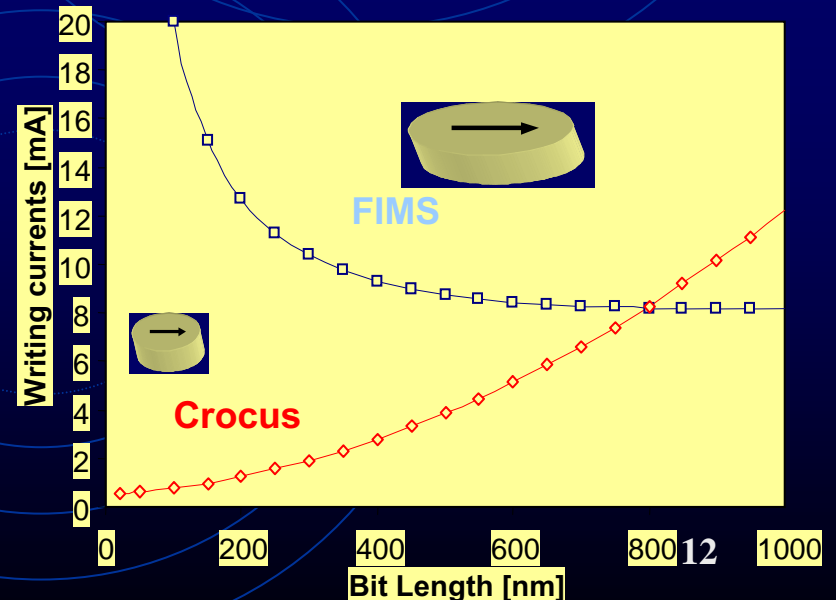
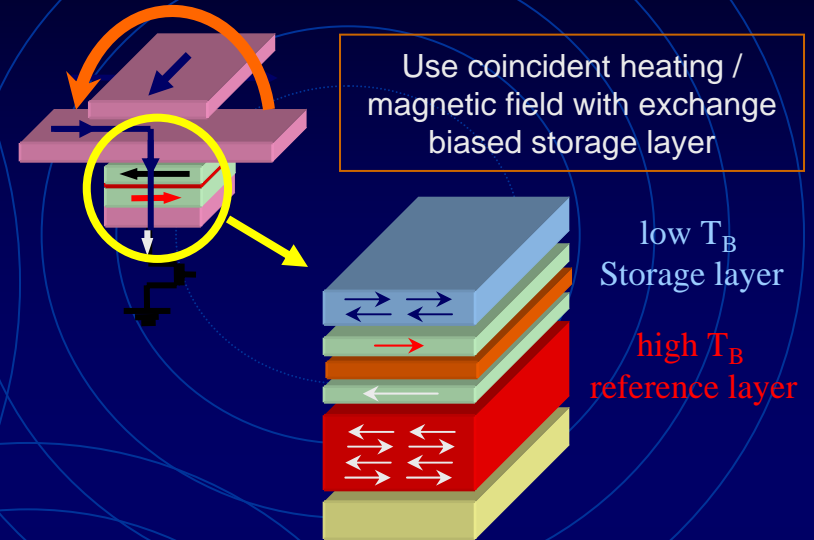
- An innovative cell selection design
- A sophisticated material technology

Solves present MRAM limitations :

- Selectivity AND full scalability

Provides additional benefits :

- Low power consumption
- No memory erasure from external field
- Circular bits for lower capital investment
- Only 3 mask levels
- Very compact structure by stacking transistor and MTJ cell

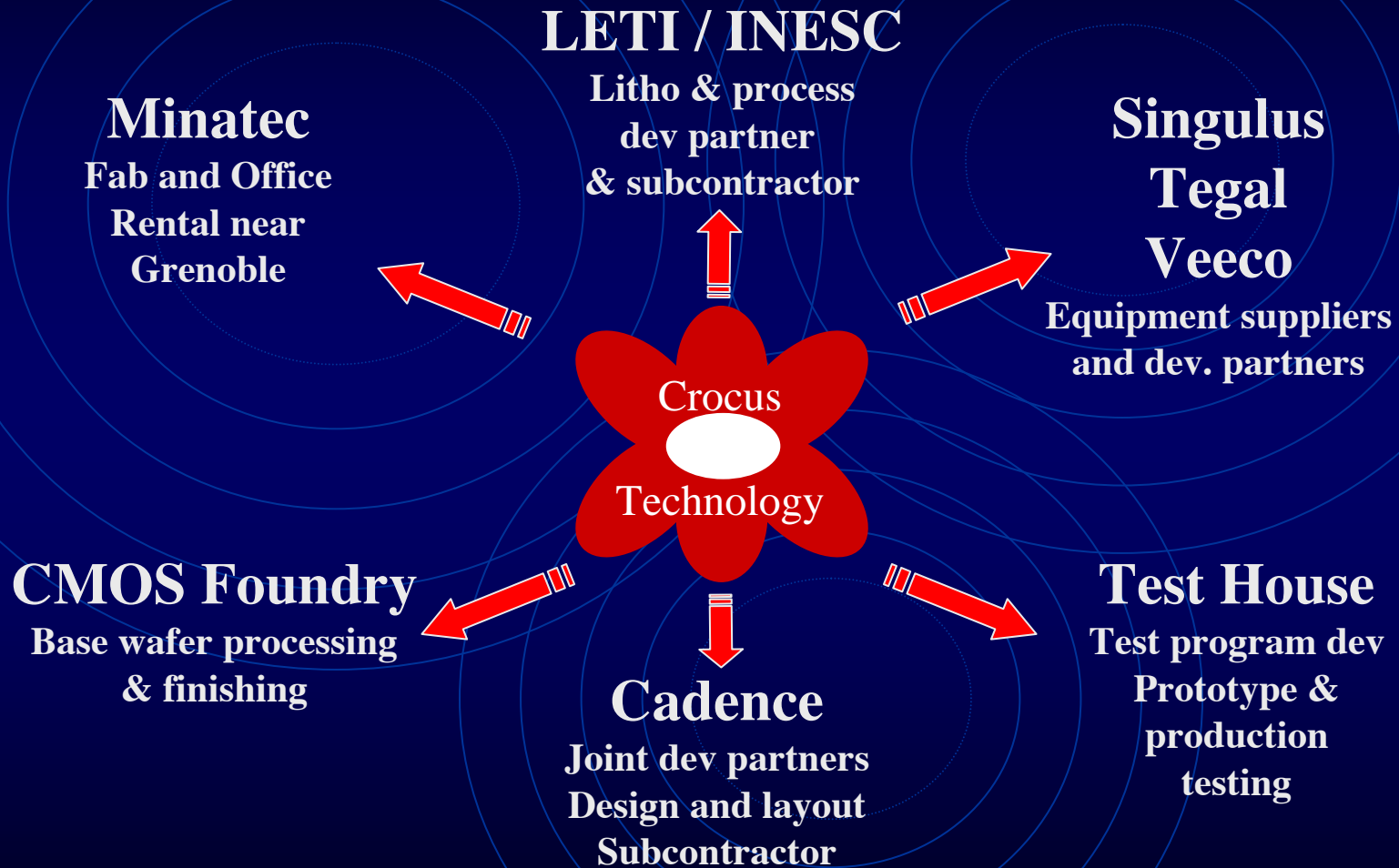


Strategic Issues

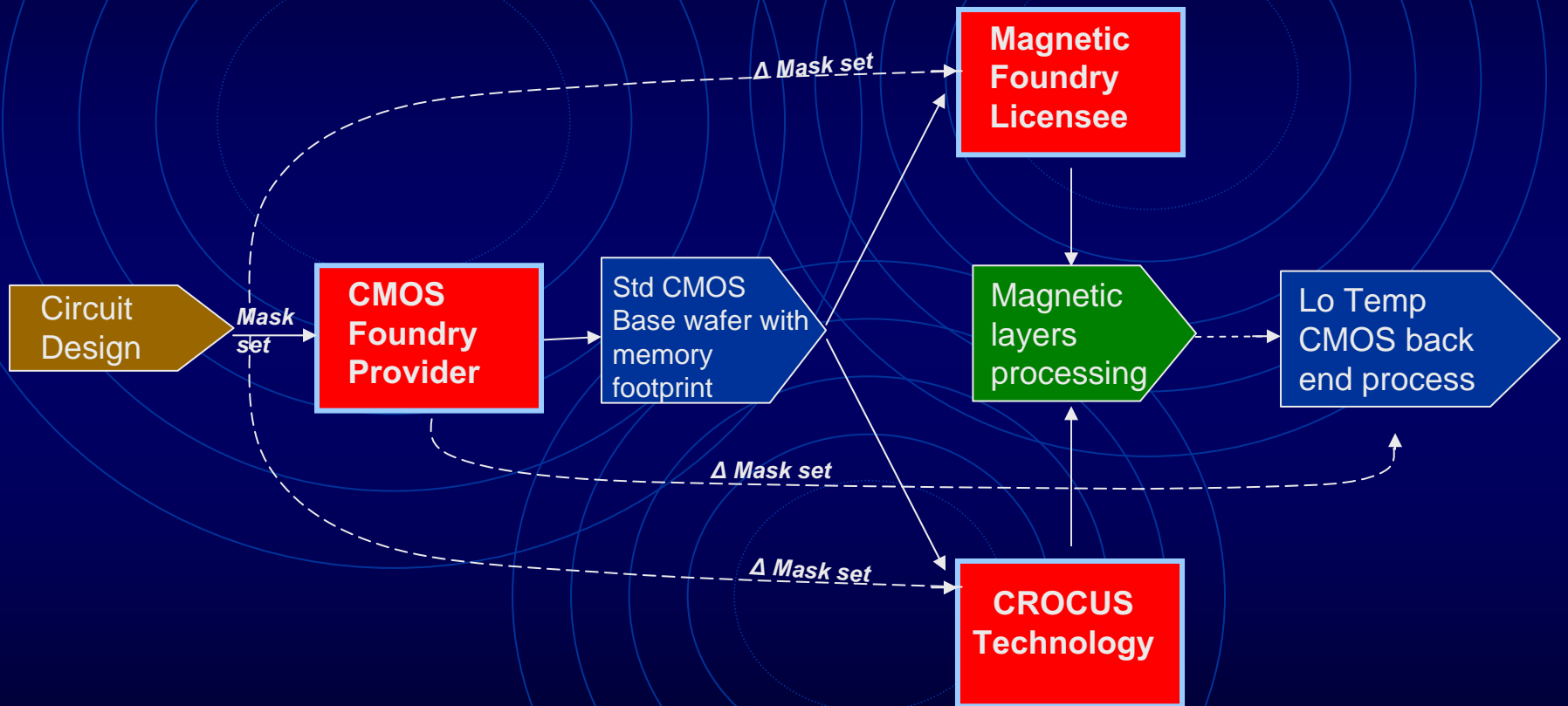
Competitive environment

- **Competitors have yet to demonstrate a working MRAM product:**
 - IBM has withdrawn from the Altis JV (Infineon still pursuing MRAM effort)
 - Micron, ST, Cypress and others have cancelled their MRAM program
 - Freescale is sampling customers but with slow, high power consumption units
 - Other competitors include: Headway, Grandis, Sony, Samsung, Toshiba, NEC
- **Threat could come from:**
 - Unexpected break through from other NVRAM technologies (PCRAM, CBRAM, FERAM, etc..)
 - Faster than expected progress on existing memory process
- **Crocus is starting later but not late: our unique patented technology will allow the company to overcome the competition**

Strategic Alliances



MRAM: A modular process



Foundry issues

- Low temperature back-end
 - Compatible with Copper process
 - Necessitates full process review
- Contamination fear
 - Agree on encapsulation scheme
- Flexibility
 - Release wafers after metal 1, take them back for finishing
- Quality
 - Test of unfinished, unconnected array of transistors
 - Non standard wafer sort, repair

Crocus “mini fab”

- Initial manufacturing of “magnetic layers” *
 - 200mm capable
 - At T0: Deposition, Etching and Annealing only (€4.7M)
 - At T0 +24: SiO₂ processing + Charact (€3.3M)
 - At T0+36: Stepper + Test (€10M)
 - Likely to be superseded by foundry coop. program
 - 100% R&D use initially going down to 25% after 4 years
- Q2 Y5: first production wafers from licensees

Marketing Strategy

- Fabless Product Company
 - À la Qualcomm, Sandisk, etc..
- Licensing model:
 - À la Infineon:
 - Turn key license of process + fab set up + product
 - Cash upfront + royalty + wafer supply for sale under licensor label
- Potential licensees:
 - Memory companies: Samsung, Intel, etc...
 - ASIC foundries (embedded): TSMC, SMIC, etc..
 - IP library providers: ARM/Artisan, Virage, etc.. 19

Licensing time scale

- T0 + 18
 - Approach potential Memory and Foundry licensees based on memory test chip results
- T0 + 27
 - Sign first licensee after first commercial product characterization
- T0 + 39
 - Licensee production worthy with full manufacturing capability (10 people for a year licensing team)
- T0 + 45
 - First Licensees wafers available for sale (note that we took another 6 months margin in the budget spreadsheet)

From that time on, almost all commercial wafers will come from licensees allocations.

- **A Round**
 - Total first round of 14M Euros on a fully diluted pre-money valuation of ~10M Euros
 - 7M Euros at close of documents (1st tranche)
 - 7M Euros upon successful completion of Milestone 1: full process integration (2nd tranche, end of 3rd quarter)
- **B Round**
 - 12 to 15M Euros at end of Y2Q2
 - Based on successful characterization of 256kb SRAM*
- **C Round**
 - 12 to 15M Euros at end of Y3Q3
 - Based on successful customer sampling of 16Mb SRAM*
 - Will allow the company to reach cash break even in Y4Q3

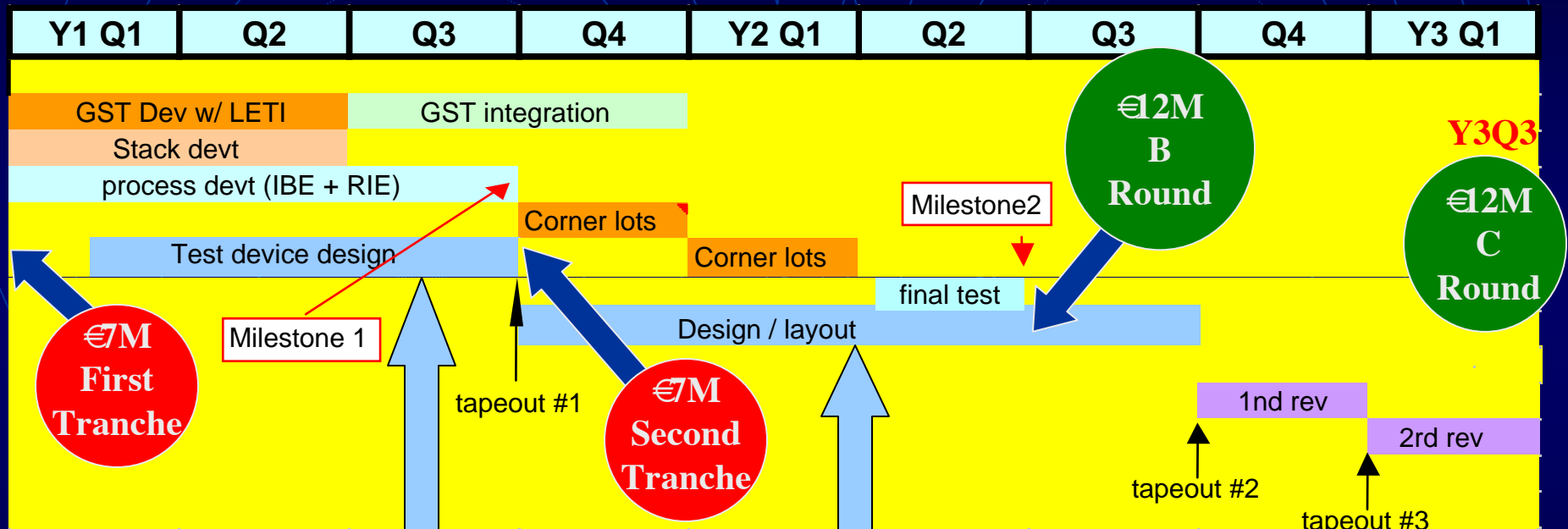
Crocus Technology holds unique assets in the pursuit of its business objectives

- **Strong and internationally experienced management team**, both with large company and start-up background
- **Exclusive access to the MRAM IP from CEA/CNRS** joint R&D world class effort, together with an Advanced Research Agreement for follow-on technology generations
- The proximity and ease of **access to world leading customers** in its targeted market segment: Thomson, Nokia, Logitec, Gemplus, Thales, Philips, STM,...
- Opportunity to **operate in one of Europe most developed microelectronic environment and the world center for magnetic research: Grenoble**
- **A syndicate of Tier one Venture Capitalists from Europe and Silicon Valley** with successful semiconductor investment history
- **A network of French and European level contacts** with authorities in order to access financial and technical public R&D funding and industrial support

A strong team

- **Chairman : Jacques Noels (MSEE)**
 - >30 years experience with SC and electronic industry including 17 at TI
 - CEO of Thomson SC and co-creator of STM
 - CEO of Nokia Consumer Electronics, member of Nokia Operating Board
- **CEO : Jean-Pierre Braun (MSEE)**
 - >30 years experience in EDA and Semiconductor industry including 25 in Silicon Valley
 - CEO of 2 EDA and one Semiconductor company
 - 25 years in design, design management, business development and corporate management
- **CTO : Jean-Pierre Nozieres (PhD)**
 - 20 years experience in Public Research and applied magnetic technology to industry
 - 2 years at IBM –Almaden (USA) Research laboratory (first spin valve magnetic heads)
 - 6 years as L. Neel Laboratory in CNRS managing a team of PhDs and assuming coordinating the work of 14 R&D Centers on magnetic nanostructures
 - Applied Magnetic (USA)R&D Director for read heads
 - Spintec Laboratory Director (CNRS)
- **Operations: Thierry Chavigner**
 - 16 years of experience in semiconductor industry including 13 at IBM Corbeil
 - 4 years Industrial Engineering Manager, member of IBM WW Equipment Selection Committee
 - 2 years as Head of New Product Prototyping fabrication
- **CFO: Laurence Fayand (CPA, MBA)**
 - 2 years at Ernst & Young
 - 9 years at HP in cost accounting and as European Services Controller

Initial schedule



A 3 by 3 array of 256kbit SRAM memories with full addressing, pads, control and decode. Each one of the 9 memories will allow variations in sizes and geometries

A full functionality hi speed 16Mbit SRAM ready for customer sampling. This first design will be pin to pin compatible with an application specific SRAM TBD

Milestone 3
End of Y3Q2:
Successful sampling
of 1st
commercial
product

CROCUS Mission Statement

- *Crocus Technology's mission is to become the dominant supplier of MRAM products and technology. This mission will be achieved through the following complementary strategies:*
 - To demonstrate conclusively that Crocus technology overcome all of today's competing MRAM's roadblocks;
 - To develop a series of stand alone memory chips aimed at specific SRAM and Flash market segments, then to qualify these as hard macros for implementation as embedded memory blocks in SoC's.
 - To add embedded MRAM in SoC's to the company's marketing and sales focus once the required yield and quality levels are established to consistent, acceptable levels;
 - To leverage Crocus French development fab and the LETI / SPINTEC partnership to continuously develop breakthrough technologies
 - To seek foundry partnerships early on from leading ASIC foundries worldwide and to enable them in the MRAM business through licensing and technology transfer deals;