A Setup for Automatic MOSFET Mismatch Characterization under a Wide Bias Range

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UFSC – LCI – May 2007 *WCM2007*

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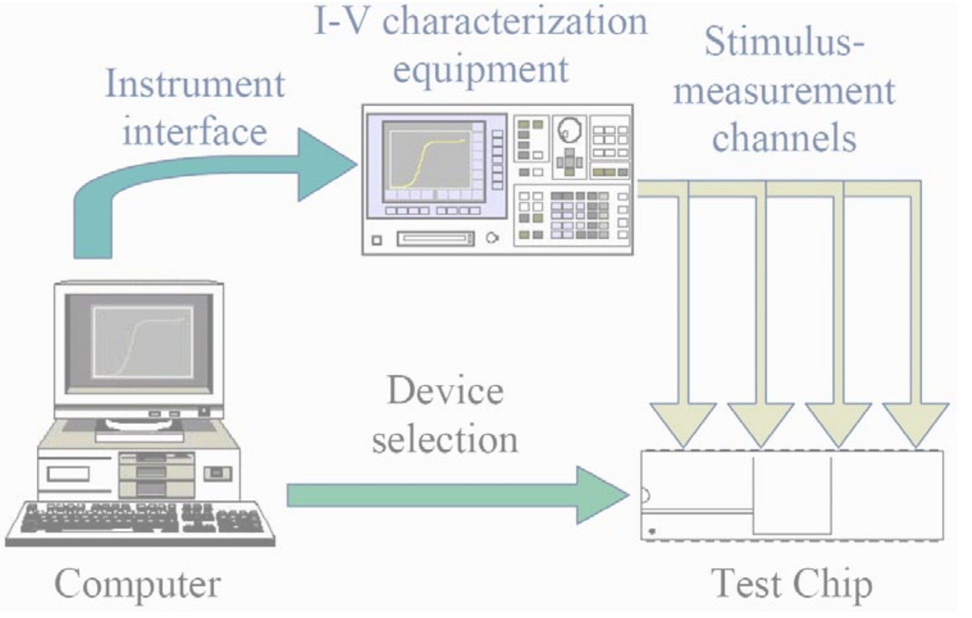
Outline

- MOSFET dc characterization setup
- The Test Circuit
- Our Mismatch Model
- Experimental Results
- Conclusions

Introduction

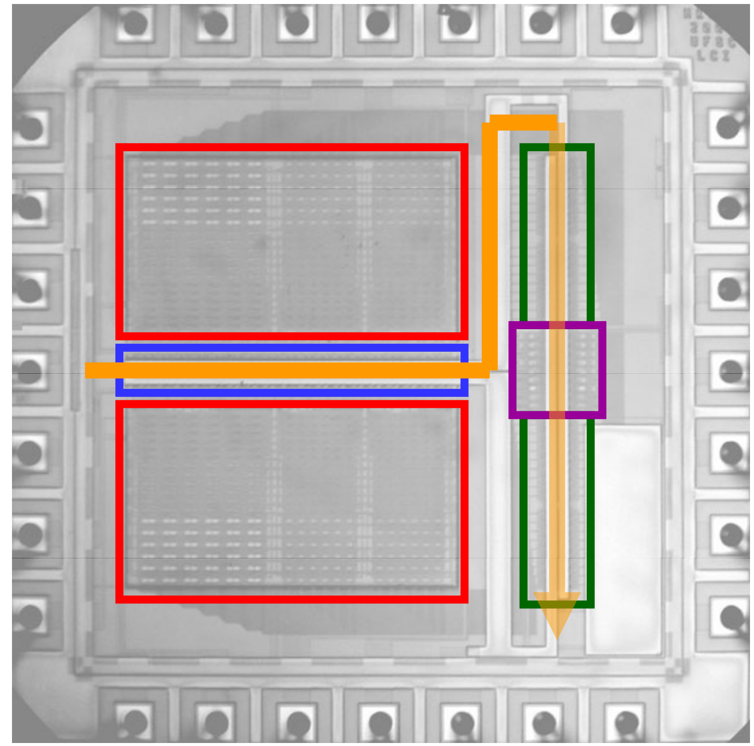
MOSFET DC CHARACTERIZATION SETUP

- **Test Chip:** N and PMOS arrays of identical test transistors ⇒ DC statistical characterization; many geometries and bias
- **I-V Characterization Equipment:** current-voltage stimulus-measurement units (SMU), control system and communication interface
- **Computer:** SMU's bias sequencing, data storage and test device selection



The Test Circuit

- fabricated in:
  - TSMC **0.35** (λ = 0.25µm)
  - TSMC **0.18** (λ = 0.10µm)
- geometries:
  - *scaled W: 3λ, 12λ and 48λ*
  - *scaled L: 2λ, 8λ and 32λ*
- 9 NMOS and 9 PMOS arrays
- 36 pairs of identical transistors/ array
- differential pooling measurement
- inversion-level biasing
- 81-bit serial-programmable shift-register (selection switches control)
- 28-pad 1.5 mm square chip



- ❑ NMOS and PMOS test arrays
- ❑ drain switches + 36-bit register
- ❑ gate switches + 36-bit register
- ❑ 81-bit programming data path
- ❑ reference switches + reference transistors + 9-bit register

Our Mismatch Model

Using ACM model, drain current mismatch can be written as

$$\frac{\sigma_{I_D}^2}{I_D^2} = \frac{1}{WL}\left[\frac{N_{oi}}{N^{*2}}\frac{1}{i_f - i_r}\ln\left(\frac{1+i_f}{1+i_r}\right) + A_{I_{SQ}}^2\right] \quad ; \quad N^* = \frac{-Q'_{IP}}{q} = \frac{nC'_{ox}\phi_t}{q}$$

- N_{oi}: effective number of impurities per unit area, in the depletion region
- A_{ISQ}: accounts for variations in the specific current ($I_{SQ} = ½\mu C'_{ox} n\phi_t^2$)
- N^*: number of carriers per unit area, in the inversion region, at pinch-off

This expression relates mismatch to:

- bias, through source and drain inversion levels (i_f, i_r)
- device geometry (W, L)
- technology (N_{oi}, A_{ISQ}, N^*)

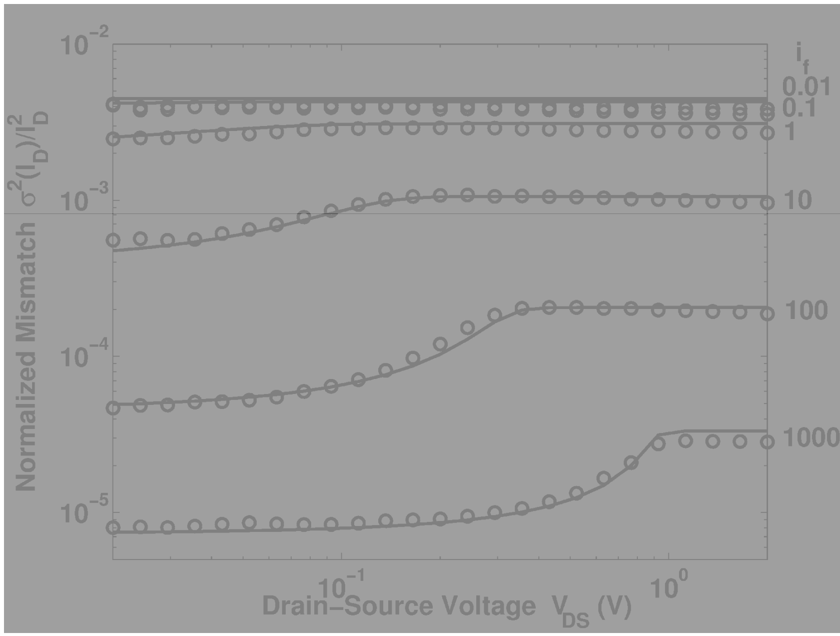
$$A_{VT}^2 = \frac{q^2}{C'^2_{ox}} N_{oi} \quad ; \quad A_\beta = A_{ISQ}$$

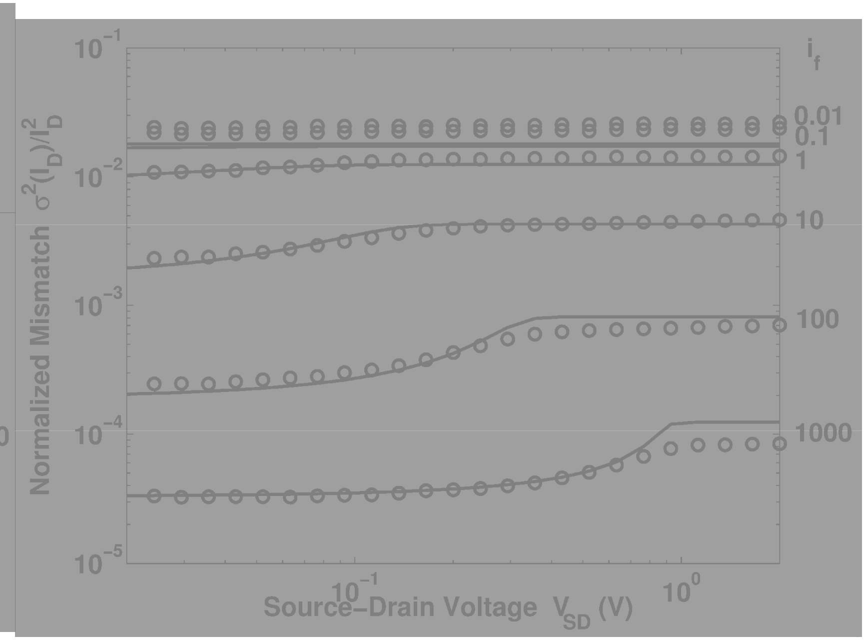
From ACM long channel model

$$I_D = I_F - I_R = I_S(i_f - i_r) \quad ; \quad I_S = \tfrac{1}{2}\mu C'_{ox} n\phi_t^2 \frac{W}{L}$$

Experimental Results – TSMC 0.35

NMOS **W=3 µm L= 2 µm** PMOS





Circles: *test chip measurements*
Solid lines: *our mismatch model*
i_f: *forward inversion level*

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Conclusions

- "Low cost" test setup for statistical MOSFET measurement was presented
- Force-sense stimuli increase accuracy (reduction of signal path effects)
- "Average over (2) measurement units" technique reduces errors due to instrument mismatch
- On-chip switching allowed us to measure more than a thousand transistors using a reduced number of connection pads