
Workshop on Compact Models, NSTI NANOTECH 2007
Santa Clara, California, May 21-24, 2007

**Design-oriented Characterization and Parameter
Extraction Methodologies for the EKV3 MOSFET Model**

Matthias Bucher
Technical University of Crete (TUC), Greece

Antonios Bazigos
NTUA, Athens, Greece

Dimitrios Diamantakos
Technical University of Crete (TUC), Greece

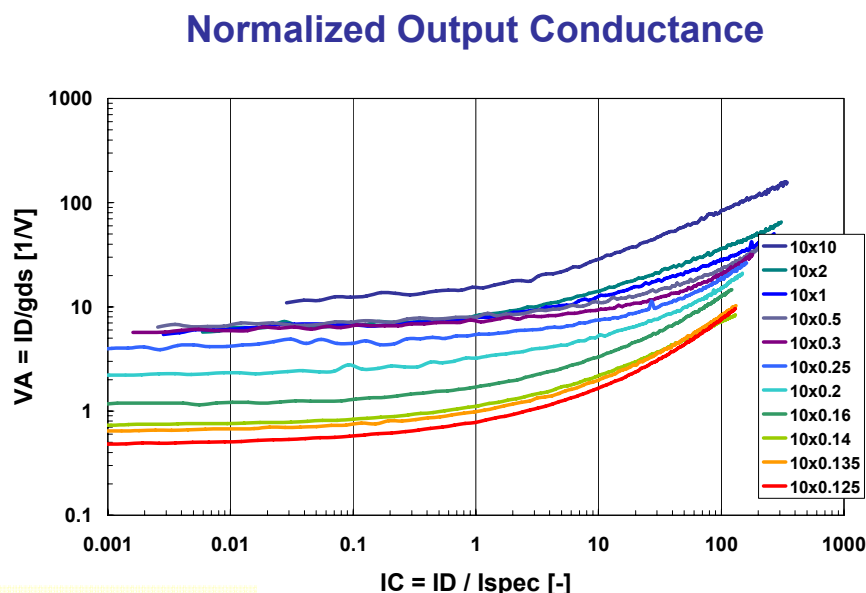
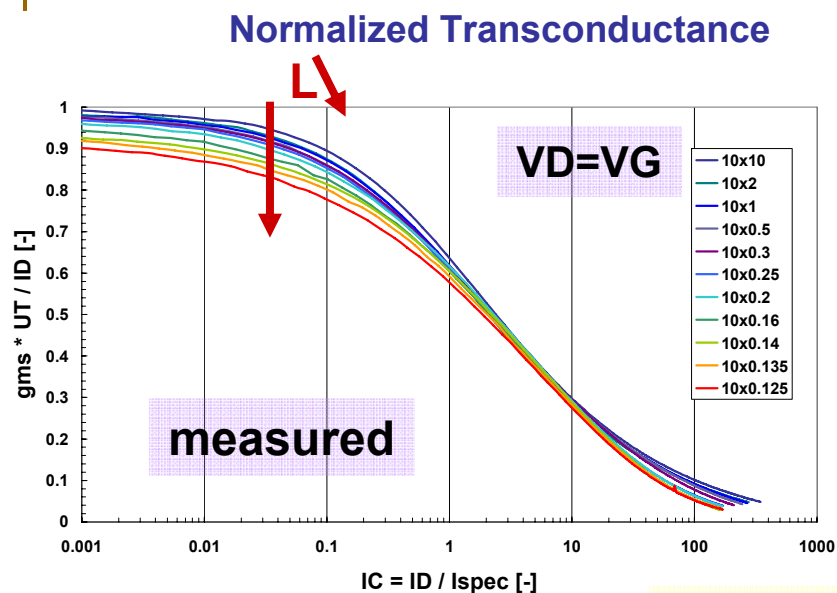
François Krummenacher
EPFL, Switzerland



Outline

- ❖ Moderate inversion in advanced CMOS
 - ✓ Modeling \leftrightarrow characterization
 - \leftrightarrow circuit design
- ❖ Characterization / Parameter extraction methods for EKV3
- ❖ Current Status of EKV3
- ❖ Conclusions

Moderate inversion – low- frequency



Inversion Coefficient



Moderate Inversion

Moderate Inversion

$$\frac{g_{ms} \cdot U_T}{I_D} = G(IC) = \frac{1}{\frac{1}{2} + \sqrt{\frac{1}{4} + IC}}$$

$$IC = \frac{I_D}{I_{SPEC}}$$

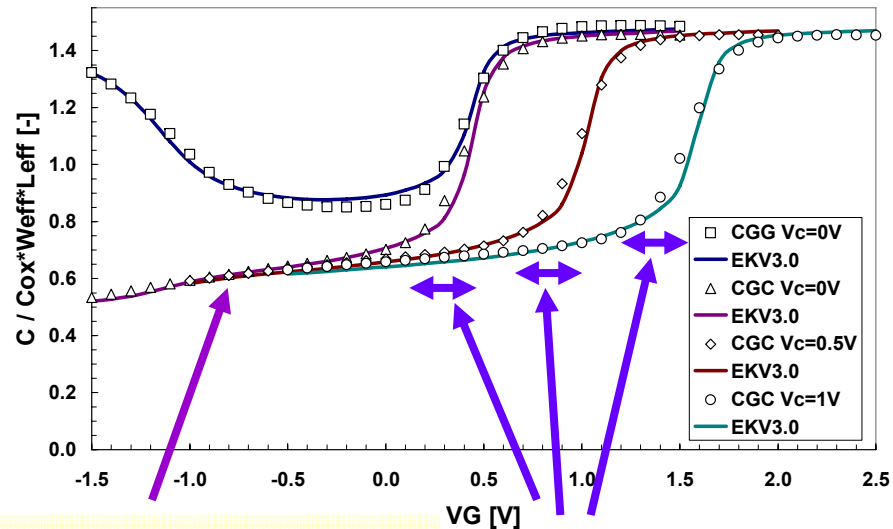
$$I_{Spec} = 2nU_T^2 \mu C'_{ox} \frac{W}{L}$$

Specific Current

- ❖ Normalization factor for drain current: **Ispec**
- ❖ Normalized gm and gds vs. **IC** and L
- ❖ Anomalous scaling of output conductance in WI

Moderate inversion – high frequency

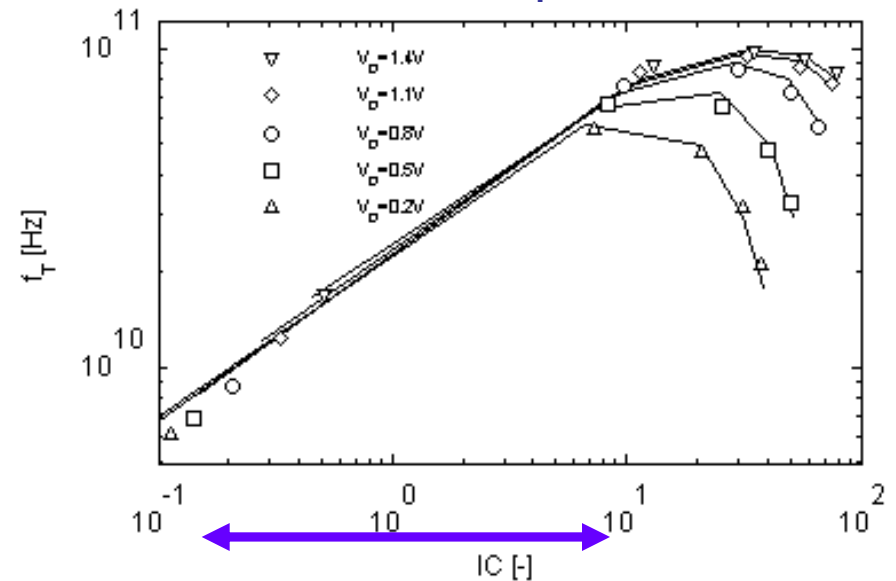
CV characteristics of MOSFETs



Overlap & fringing caps.
(do NOT scale with L)

Moderate Inversion

Transit Frequency f_T of MOSFETs



Moderate Inversion

Moderate Inversion in MOSFETs – highly important for analog/RF IC design

- ❖ Good trade-off among gain, speed, linearity, noise, matching
- ❖ Low-medium saturation voltage, Series resistance effect negligible
- ❖ Reduced impact of mobility effects (vertical field) and velocity saturation

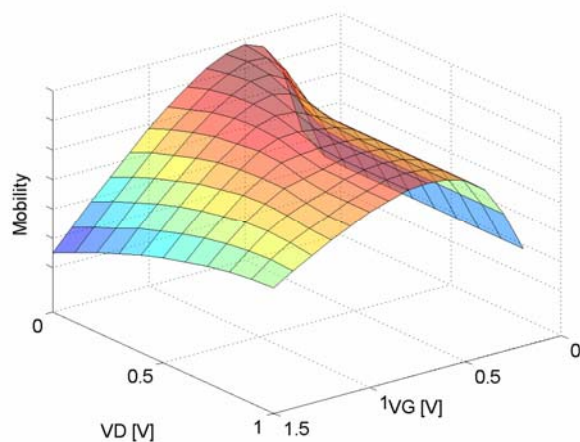
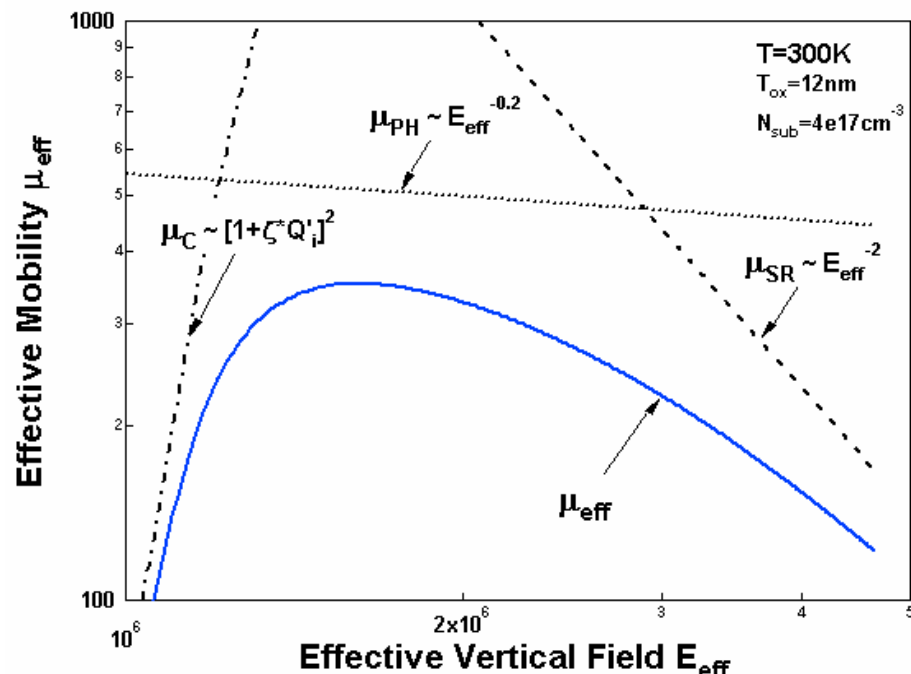
EKV3 model review

- ❖ Due to CMOS scaling, ICs operate more and more in moderate and weak inversion
- ❖ Design methods and models are required
 - ‘classical’ methods don’t cover moderate inversion
- ❖ EKV3 is a Compact MOS Transistor Model dedicated to Analog/RF IC design
 - ✓ Developed as a successor of EKV2.6 (since 1997)
 - ✓ Charge-based approach – close to physics and design
 - ✓ Special attention to analog/RF IC design requirements
 - ✓ Covers essential effects down to 65nm CMOS
 - ✓ Scaling over Technology – Width – Length – T – Bias
 - ✓ EKV3 available for implementation to CAD vendors.

EKV3 – charge model basics

- ❖ Basis of charge model development is surface potential equation & inversion charge linearization
 - ✓ Same parameters as surface potential model
 - ✓ Preserves the essence of a surface potential model.
- ❖ Extensions for CV:
 - ✓ Vertical non-uniform doping
 - ✓ Polydepletion
 - ✓ Quantum effects
- ❖ Extensions of IV:
 - ✓ Charge-based vertical field mobility
 - ✓ Charge-based velocity saturation
 - ✓ Charge-based CLM
 - ✓ Gate tunnelling

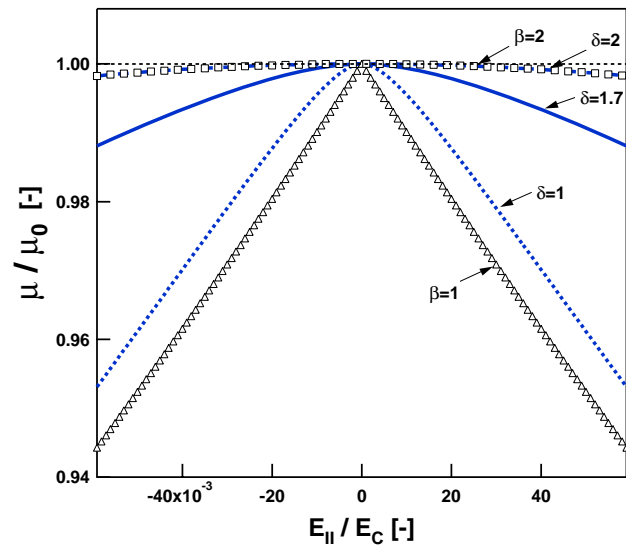
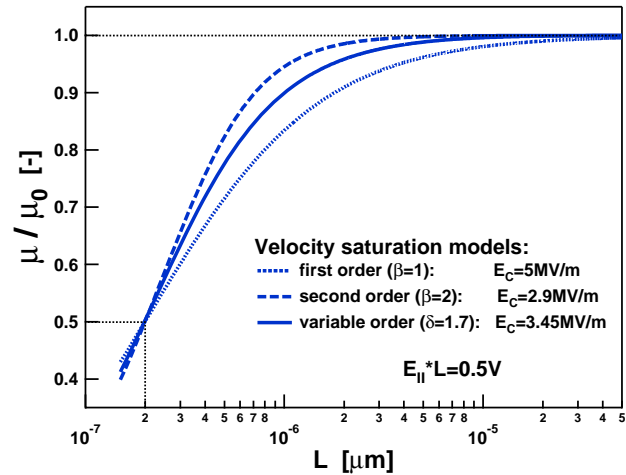
EKV3 mobility modeling



- ❖ Effective-field based mobility modeling
 - ✓ Surface-roughness scattering (high vertical field)
 - ✓ Phonon-scattering intermediate field strengths
 - ✓ Coulomb scattering effects (low vertical field; particularly at very high N_{sub} , low T)
- ❖ 5 parameters in all:
 - ✓ $E0$, $E1$, ETA , THC , ZC
- ❖ Local mobility is integrated along the channel

$$E_{eff} \propto Q_b + \eta \cdot Q_i$$

EKV3 velocity saturation/CLM modeling



- ❖ *Variable-order* (1st-2nd), charge-based velocity-field relationship
 - ✓ *Continuous* at $V_D=V_S$
 - ✓ Requires 2 parameters:
 - UCRIT, DELTA [1..2]
 - ✓ Modulates mobility mobility scaling with channel Length

- ❖ Charge-based channel length modulation (CLM) model.
 - ✓ *Continuous* at $V_D=V_S$
 - LAMBDA

EKV3 model scaling effects

- ❖ RSCE, INWE, combined short&narrow-channel effects
- ❖ DIBL, charge-sharing
- ❖ Halo/Pocket implant effects
 - ✓ including @long channel
- ❖ Bias-dependent overlap & inner fringing capacitances
- ❖ Bias-dependent series resistance
- ❖ Geometry & temperature scaling
- ❖ Parasitic effects modeling
 - ✓ Layout dependent stress
 - ✓ Edge conduction
 - ✓ Gate tunneling
 - ✓

Phenomena covered by EKV3

Modelled effect	Related Parameters / Comments
Physical Modelling of Charges Including Accumulation Region Polysilicon Depletion, Quantum Mechanical Effects	COX(TOX), PHIF, GAMMA(NSUB), VTO(VFB), GAMMAG(NGATE)
Bias-Dependent Overlap Capacitances	LOV, GAMMAOV(NOV), VFBOV
NQS	[Channel Segmentation]
RF Model External Sub-Circuit	[Appropriate Scaling of RG, RSUBS with W, L and NF]
Mobility (Reduction due to Vertical Field Effect) Surface Roughness-, Phonon-, Coulomb Scattering	KP(U0), E0, E1, ETA ZC, THC
Impact Ionization Current	IBA, IBB, IBN
Gate Current (IGS, IGD, IGB)	KG, XB, UB

Phenomena covered by EKV3

Modelled effect	Related Parameters / Comments
Longitudinal Field Effect Velocity Saturation, Channel Length Modulation	UCRIT(VSAT), LAMBDA, DELTA
Reverse Short Channel Effect	LR, QLR, NLR
Inverse Narrow Width Effect	WR, QWR, NWR
Drain Induced Barrier Lowering	ETAD, SIGMAD
Source and Drain Charge Sharing	LETA, {LETA2}, WETA
Halo/Pocket implant effects	LETA0
Edge Conduction	WEDGE, DGAMMAEDGE, DPHIEDGE
Geometrical Effects, Width scaling	Various Parameters (DL, WQLR, ...)
Noise Flicker Noise, Short-Channel Thermal Noise, Induced Gate and Substrate Noise	AF, KF
Temperature Effects	Various Parameters
TOTAL	<140

EKV3 parameter set

* Flags

+ SIGN = 1
+ TG = -1

* Scale parameters

+ SCALE = 1.0
+ XL = 0.0
+ XW = 0.0

* Cgate parameters

+ COX = 8.58E-3
+ GAMMAG = 18.4
+ AQMA = 0.0
+ AQMI = 0.0
+ ETAQM = 0.75

* Nch. parameters

+ VTO = 400.0E-3
+ PHIF = 450.0E-3
+ GAMMA = 300.0E-3
+ XJ = 30.0E-9
+ NO = 1.025

* Mobility

+ KP = 390.0E-6
+ E0 = 438.0E+6
+ E1 = 159.0E+6
+ ETA = 0.57
+ ZC = 1.0E-6
+ THC = 0.0

* Charge sharing

+ LETA0 = 1.0E+6
+ LETA = 1.3
+ LETA2 = 0.0
+ WETA = 1.0
+ NCS = 0.5

* DIBL

+ ETAD = 0.75
+ SIGMAD = 1.0

* RSCE

+ LR = 100E-9
+ QLR = 580E-6
+ NLR = 100.0E-3
+ FLR = 2

* INWE

+ WR = 80.0E-9
+ QWR = 500.0E-6
+ NWR = 12.0E-3

* Series resistance

+ RLX = 170.0E-6

* Overlap & fringing

+ LOV = 25.0E-9
+ GAMMAOV = 5.0
+ VFBOV = 0.0
+ KJF = 150.0E-12
+ CJF = 300.0E-3

* Long-ch. gds degr.

+ PDITS = 2.58E-6
+ PDITSD = 0.91
+ PDITSL = 0.0
+ FPROUT = 1.85E+6
+ DDITS = 0.1

* Matching par.

+ AVTO = 0.0
+ AKP = 0.0
+ AGAMMA = 0.0

* Vsat & CLM par.

+ UCRIT = 5.0E+6
+ DELTA = 1.5
+ LAMBDA = 0.5
+ ACLM = 0.85

* Geometrical par.

+ DL = -16.7E-9
+ DLC = -23.0E-9
+ LL = 0.0
+ DW = -45.3E-9
+ LDW = 0.0

* Gate current

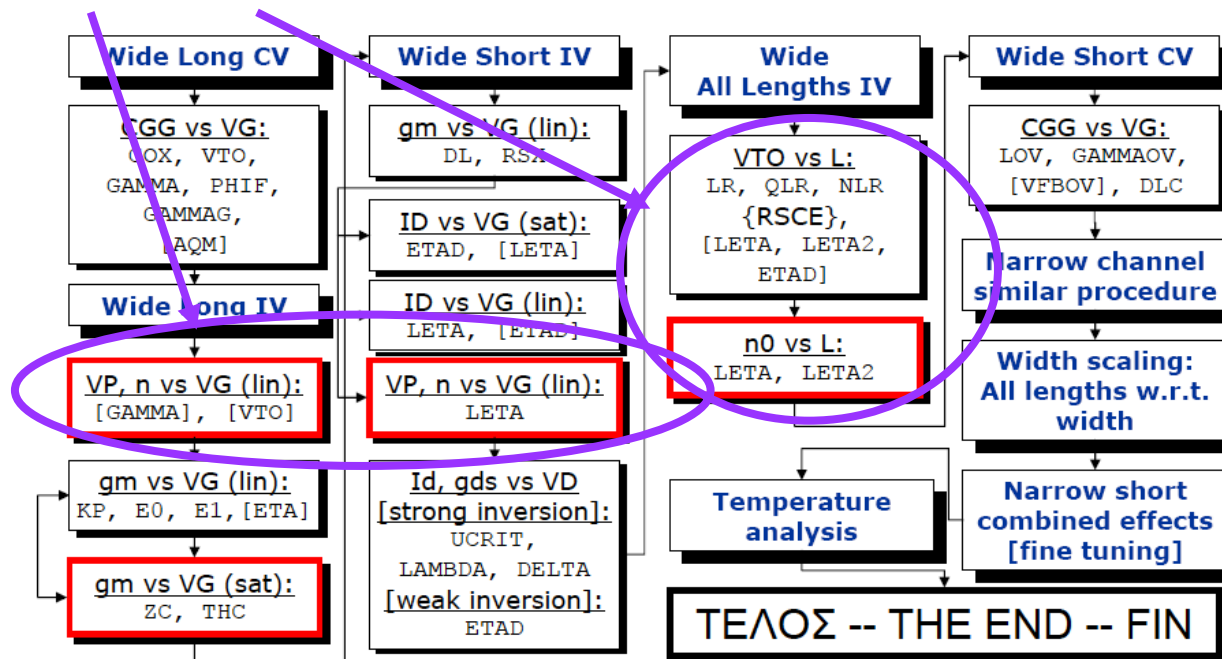
+ KG = 50.0E-6
+ XB = 5.5
+ EB = 21.0E+9
+ LOVIG = 40.0E-12

* Temperature par.

+ TNOM = 30.0
+ TCV = 600.0E-6
+ BEX = -1.6
+ TE0EX = -4.15
+ TE1EX = 0.0
+ TETA = 2.0E-3
+ UCEX = 1.2
+ TLAMBDA = 0.15
+ TCVL = 0.0
+ TCVWL = 0.0
+ WDL = 0.0
+ LLN = 1.0
+ DWC = 0.0

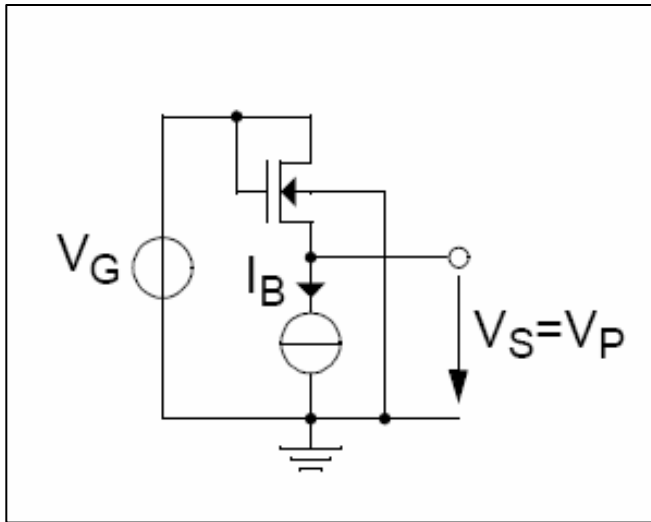
EKV3 parameter extraction sequence

Parameter Extraction in Moderate Inversion

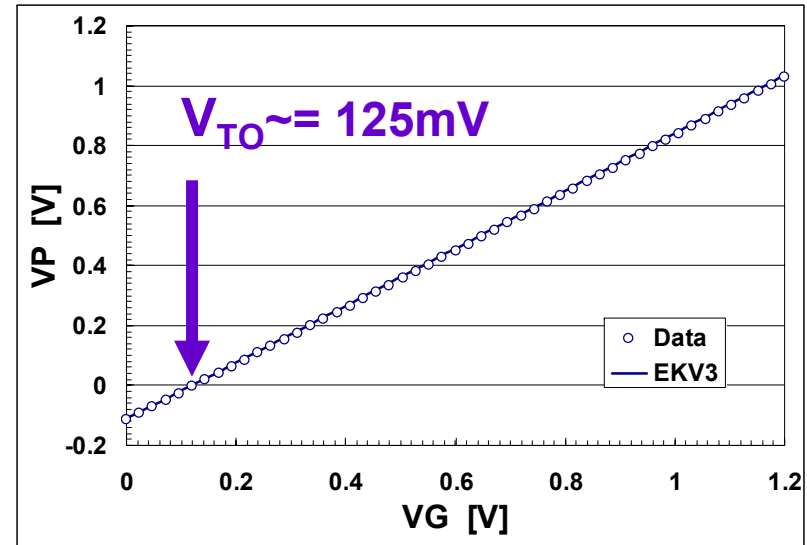


- ❖ Use conventional IV & CV data
- ❖ Sequence: CV, then wide/long IV, wide/short IV, narrow/long IV, narrow/short IV, T.
- ❖ IF specific measurements can be made, use Pinch-off voltage technique
- ❖ Has been implemented in IC-CAP (Agilent)

Pinch-off voltage measurement in MI

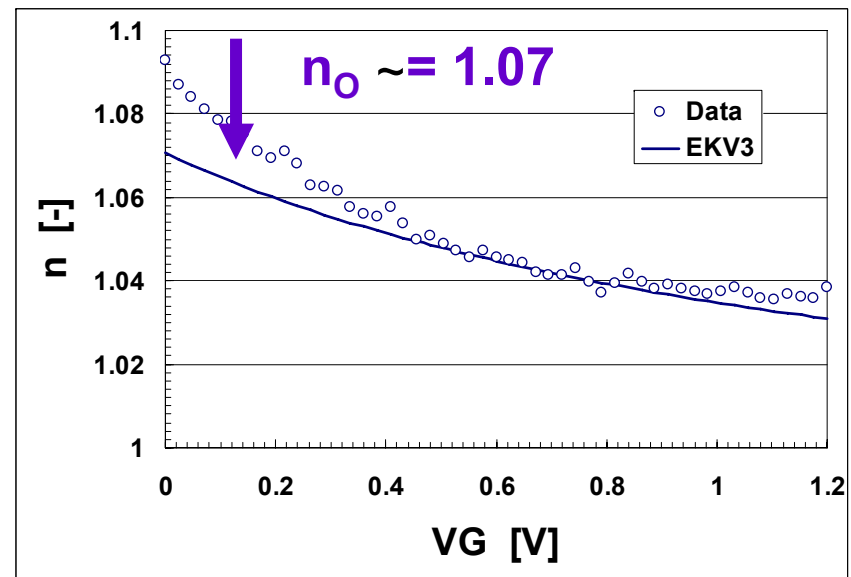


$W = 2\mu\text{m}, L = 0.5\mu\text{m}$

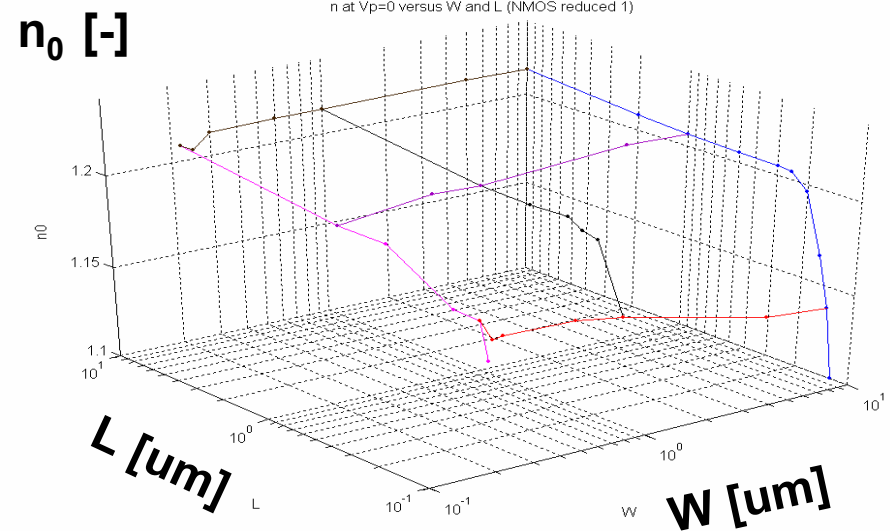
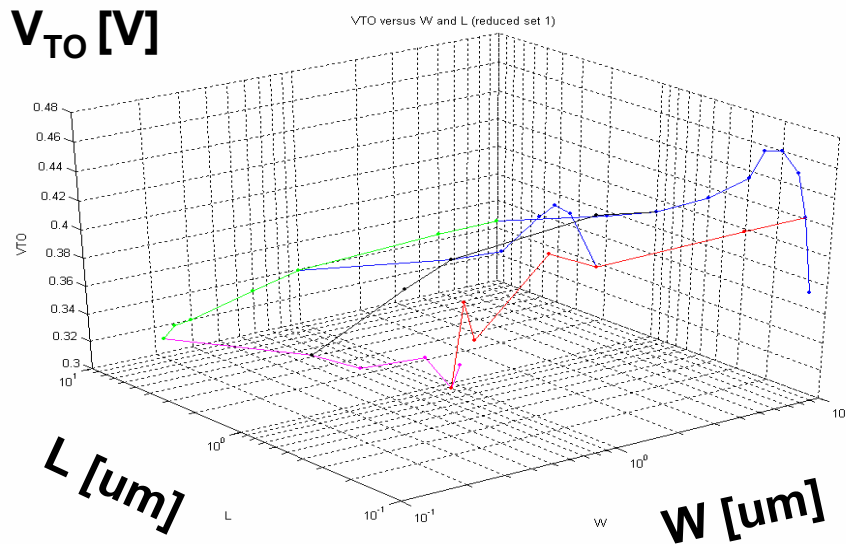


$I_B \approx 0.6 \cdot I_{\text{spec moderate inversion}}$

- ❖ $V_P = 0\text{V}$ corresponds to $V_{TO} = 125\text{mV}$, $n_0 \approx 1.07$
- ❖ Substrate effect (GAMMA) and other substrate parameters (PHIF) can be extracted as well



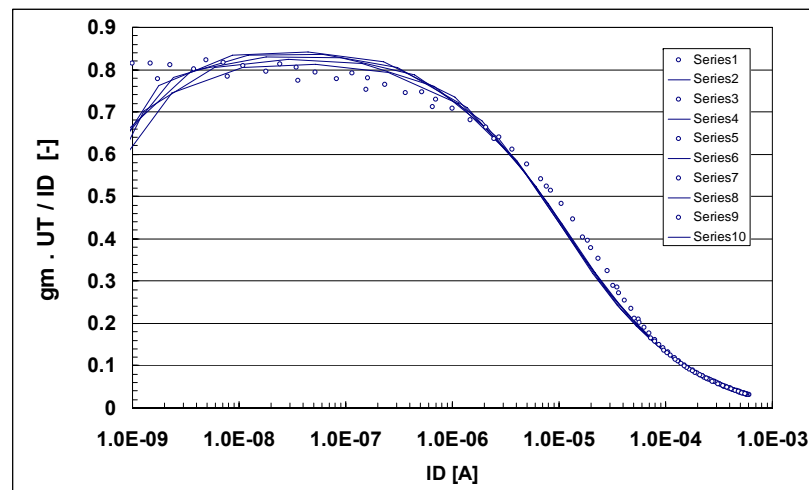
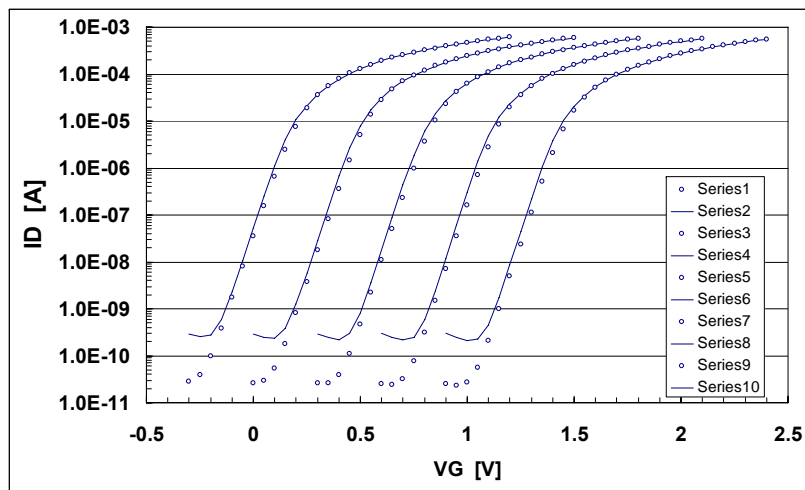
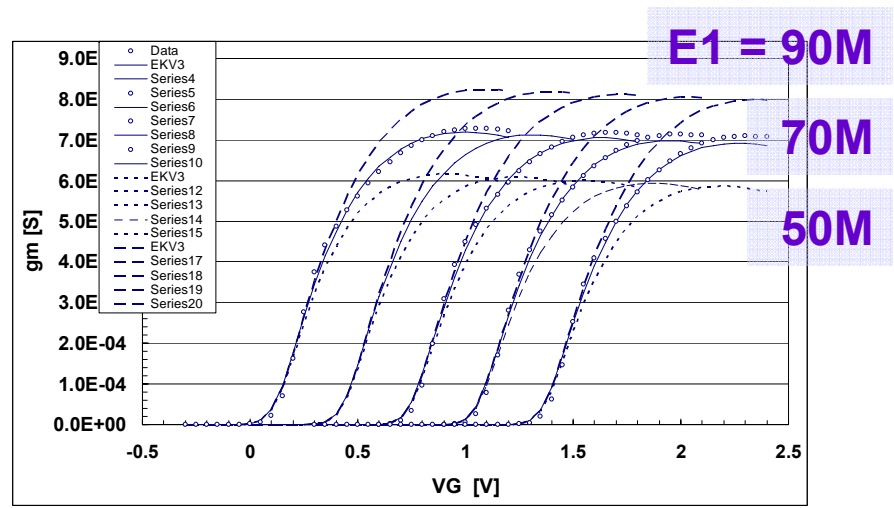
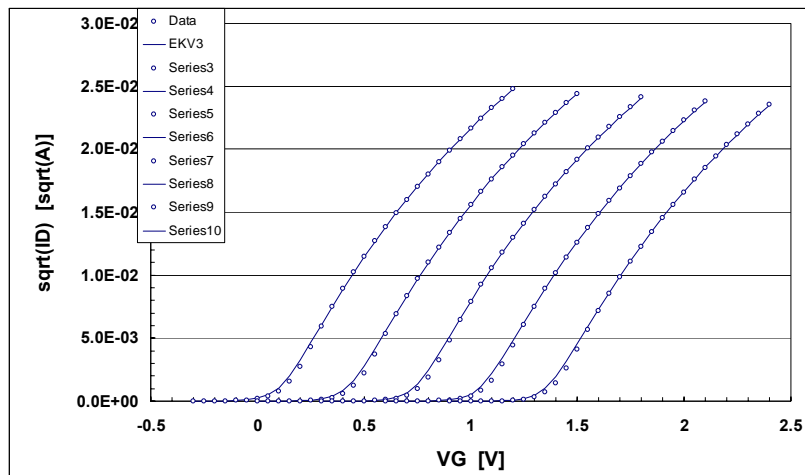
V_{TO} and n_0 vs. W , L



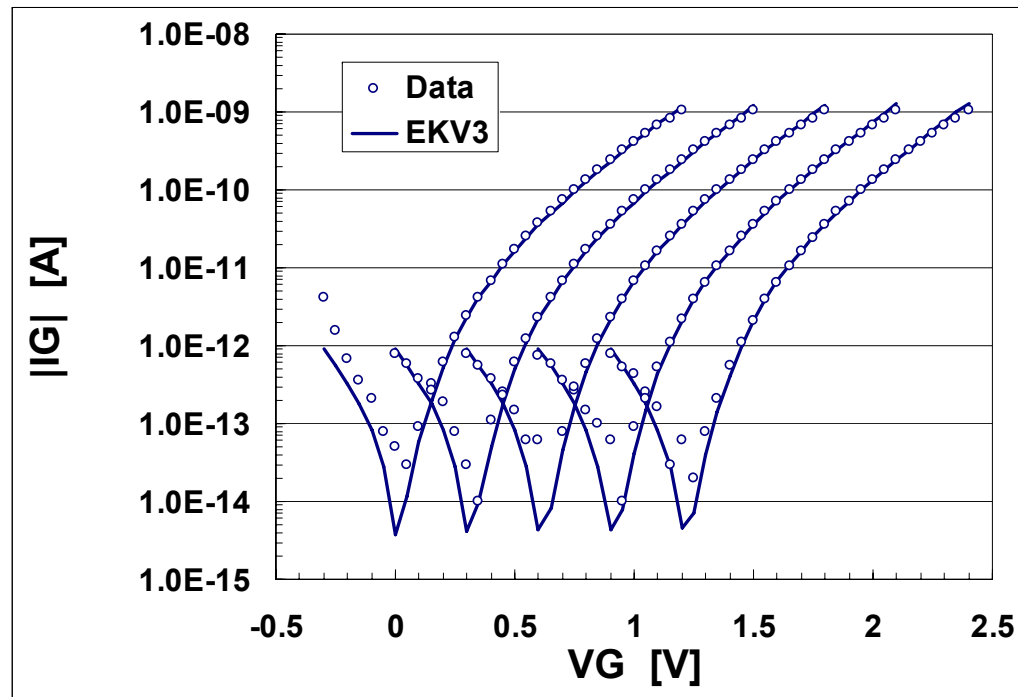
- ❖ Threshold voltage V_{TO}
 - ✓ vs. L shows known reverse short-channel effect (RSCE)
 - ✓ Less pronounced RSCE @ narrow channel.
- ❖ Slope factor n_0
 - ✓ vs. L : n_0 reduced due to charge-sharing, DIBL
 - ✓ vs. W : almost unaffected.

EKV3 – ID-VG

W = 2um, L = 0.5um



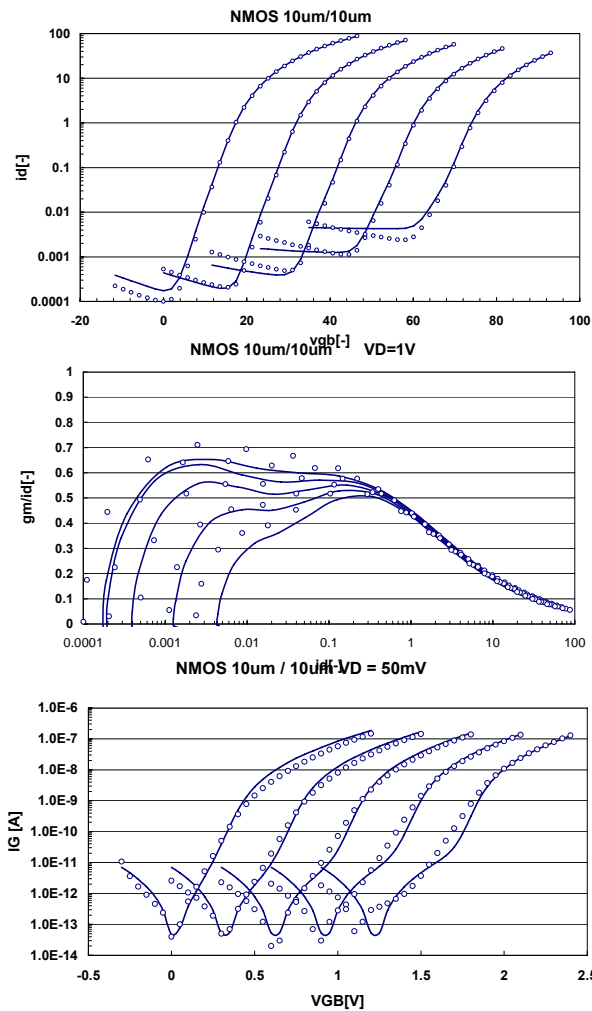
EKV3 – Gate current



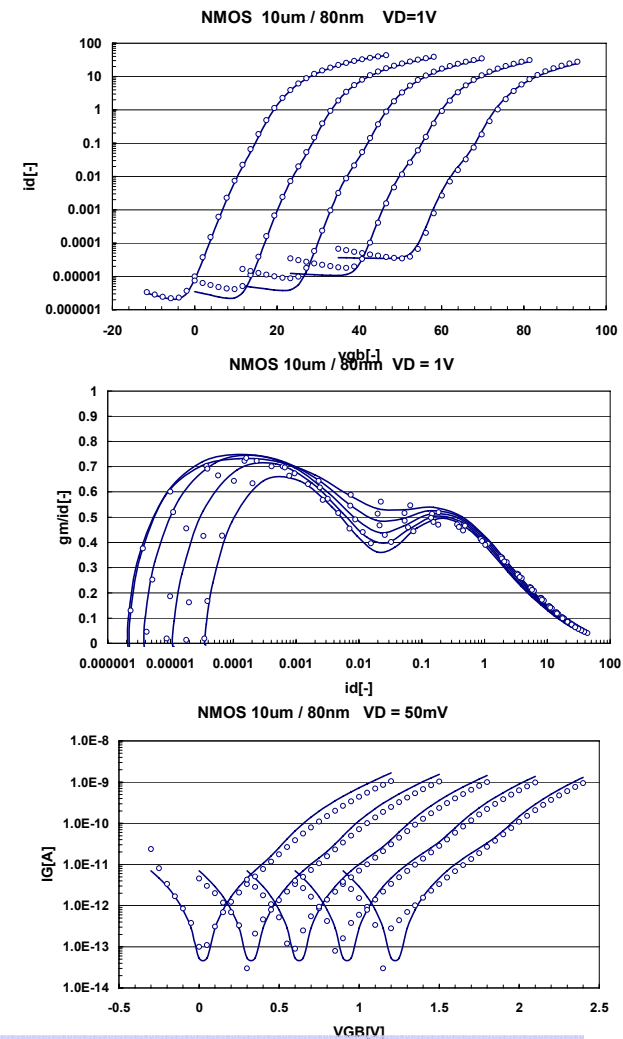
- ❖ All the tunneling current components are included
- ❖ Extract tunneling current coefficients K_G , X_B , U_B

EKV3 – STI edge conduction effect

W = 10um, L = 10um

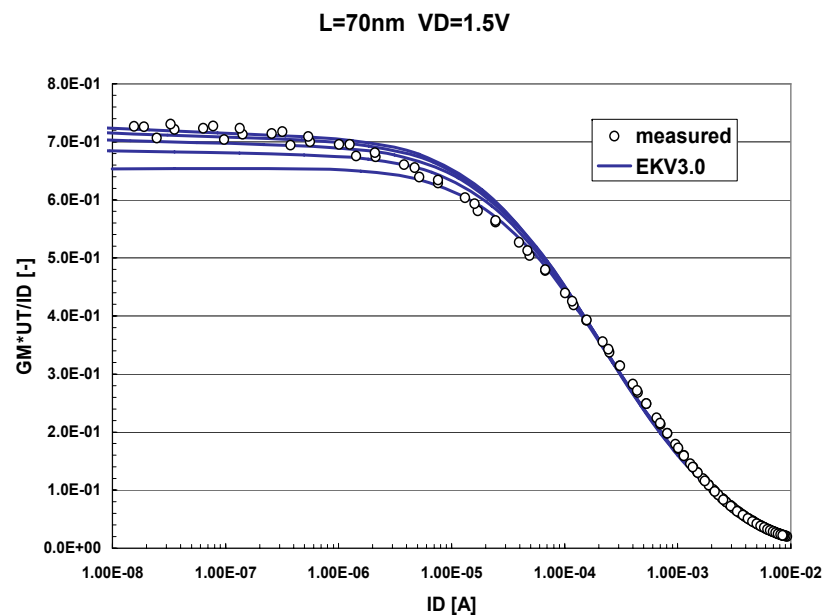
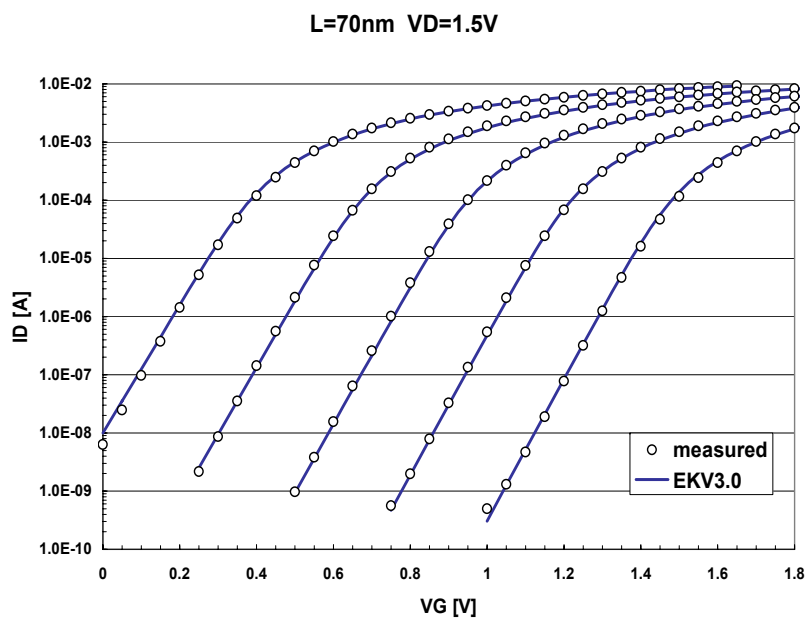


W = 10um, L = 80nm



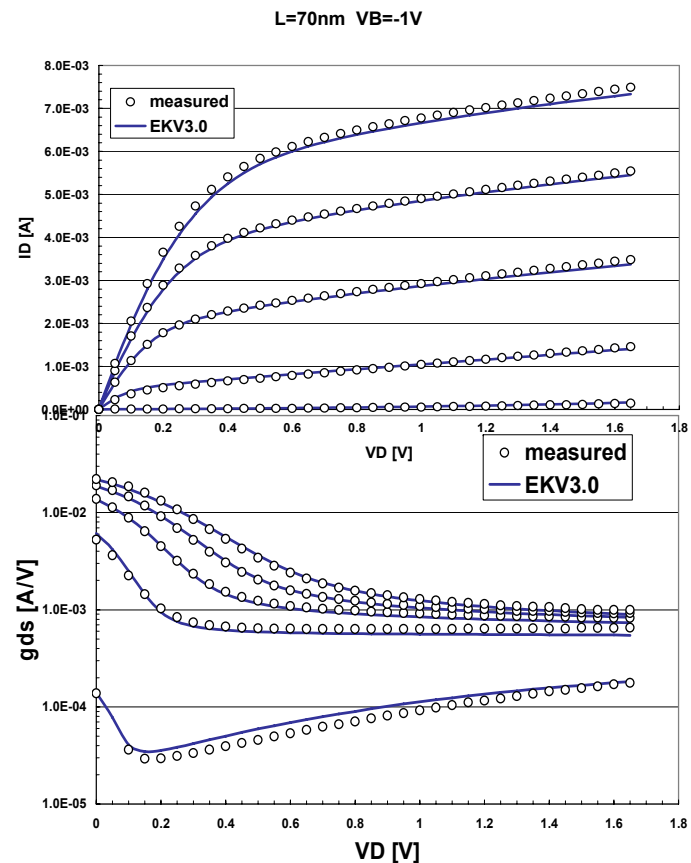
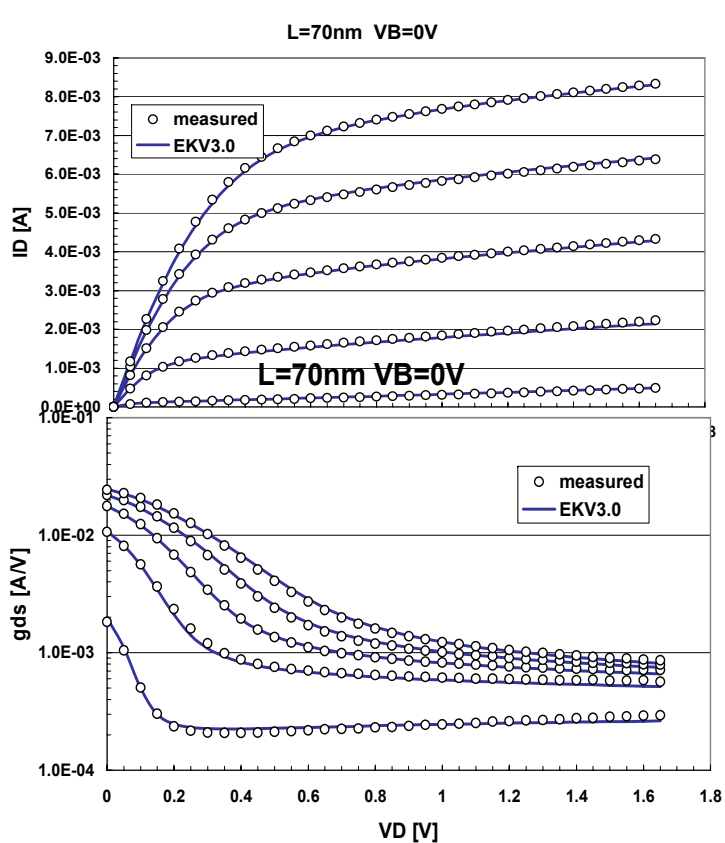
Edge conduction effect on I_D - V_G , g_m/I_D - I_D , and I_G - V_G

EKV3 short-channel



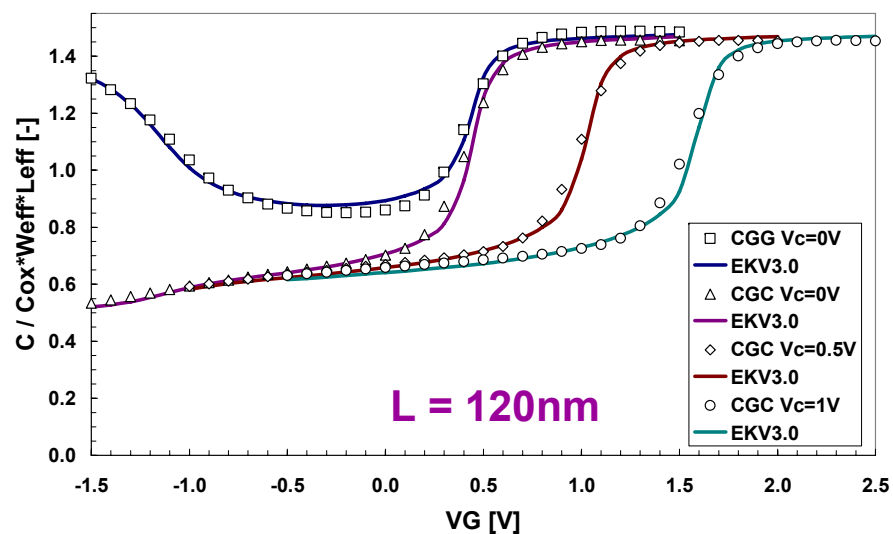
- ❖ Correct weak & moderate inversion behavior
 - ✓ Smoothness and correct asymptotic behavior
 - ✓ Correct weak inversion slope and DIBL modeling
- ❖ Transconductance-to-current ratio vs. drain current (log. axis)

EKV3 short-channel



- Illustrates combination of: DIBL, CS, velocity saturation, CLM modeling @ $L_{\text{gate}} = 70\text{nm}$

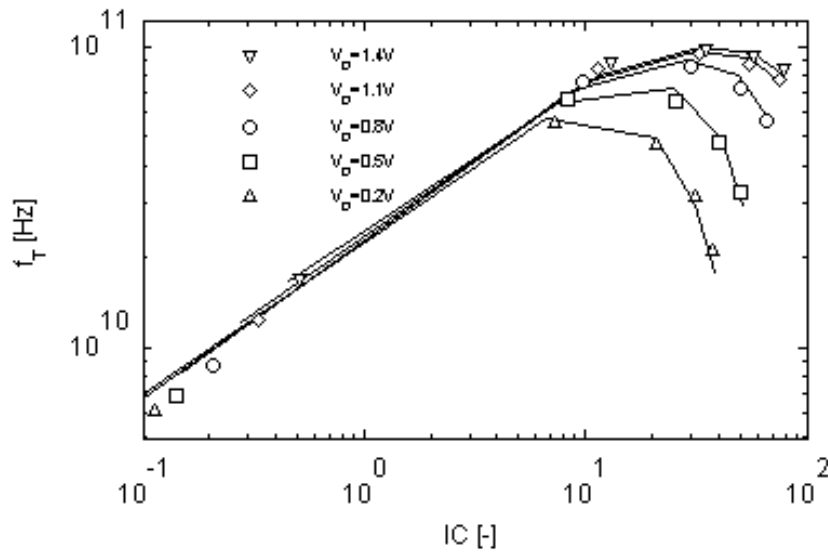
EKV3 CV modeling



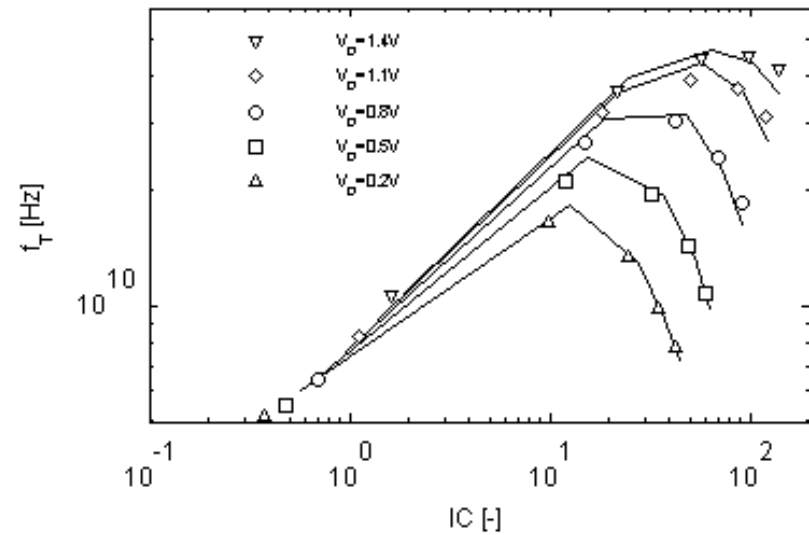
PHIF / Φ_f	400mV
C_{ox} (T_{ox})	12mF/m ² (2.9 nm)
V_{TO} (V_{FB})	250 mV (-900mV)
GAMMA	200 mV ^{-1/2}
GAMMAG	7 V ^{-1/2}
GAMMAOV	2.5 V ^{-1/2}
LOV	20 nm
VFBOV	0 V

- ❖ Continuous model, symmetric and good reciprocity
- ❖ Extension to cover depletion/accumulation
- ❖ Bias-dependent overlap & inner fringing capacitance
- ✓ LOV, GAMMAOV(NOV), VFBOV, CJF, KJF

EKV3 RF Modeling



NMOS, L = 110nm



PMOS, L=110nm

- ❖ f_T versus IC in 110nm CMOS
- ❖ Highest f_T is reached at $IC \sim 10-30$ (!)
- ❖ EKV300.02 model

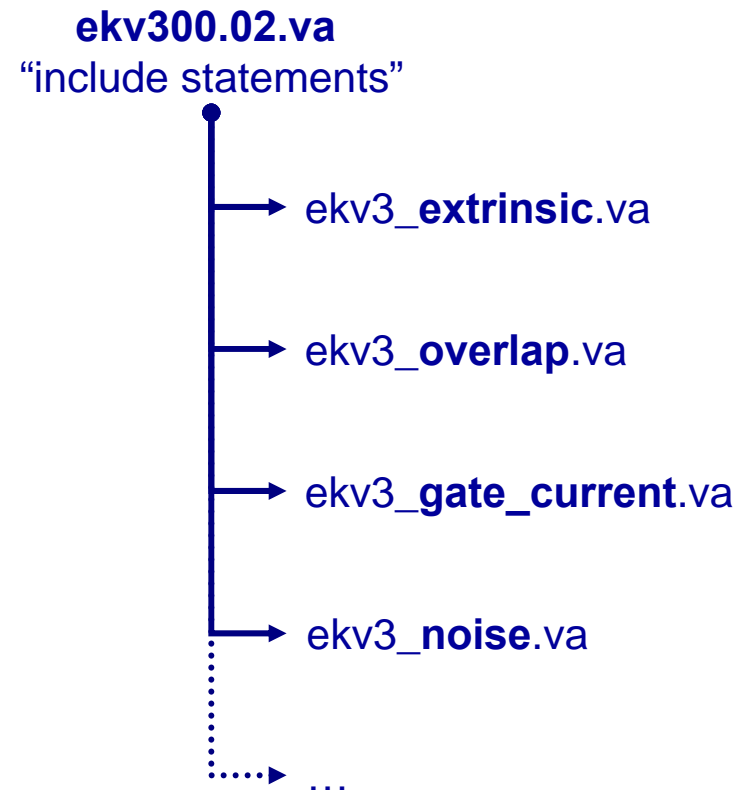
Current Code Status: EKV300.02

- ❖ EKV3 model code release:
 - ✓ 300.02: April 2007 (current version)
 - ✓ 300.01: October 2006
 - ✓ 300.00: March 2005
- ❖ Improvements in 300.02
 - ✓ STI effect on mobility and threshold voltage
 - Important for scaling of MOSFETs with RF layout
 - ✓ Noise Model: Corrections and Improvements
 - Nyquist test: Pass (Ananda Roy, EPFL)
 - ✓ Other minor improvements
 - Convergence issues

Verilog-A Code Structure

❖ The Verilog-A Code of EKV3.0

- ✓ Hierarchical Structure
 - 18 files
 - one main file
 - many smaller
 - In Total: 83KB
- ✓ Compatible with (*at least*) ELDO, ADS, SPECTRE, ADMS, ...
- ✓ Used as the Reference Code for all Model Implementations
 - ADMS provides “standard” C-code Various Simulators.



EKV3 Implementation Status

- ❖ EKV3 Verilog-A code compatible with ADMS v2.2.4
 - ✓ Tested with XML Interface for SPICE3
 - ✓ Different XML Interfaces for Different Simulators
- ❖ ELDO (Mentor Graphics):
 - ✓ Target: July 2007 (test version).
- ❖ Smash (Dolphin Integration):
 - ✓ Target: July 2007.
- ❖ Spectre (Cadence):
 - ✓ NDA to be signed.
- ❖ ADS (Agilent):
 - ✓ Tiburon Interface used for actual EKV3 design kits.
 - ✓ Early EKV3 version in GoldenGate, to be updated.

Developments in EKV3.1

- ❖ More flexible mobility modeling of short-channel transistors.
- ❖ Improved modeling of output conductance of long-channel halo-implanted devices.
- ❖ Improved vertical Non-Uniform Doping.
- ❖ Extended accounting for layout-dependent stress effects.
- ❖ Noise model enhancements.
 - ✓ Improved Accounting for carrier heating/velocity saturation in induced gate noise.
 - ✓ Refined scaling of $1/f$ noise model equations & parameters.
- ❖ Statistical aspects / device matching.
 - ✓ Refined matching models for ID
 - ✓ Accounting for IG current matching

EKV3 Summary

- ❖ EKV3: a design-oriented, charge-based, compact model for analog/RF IC design.
 - ✓ EKV300.02 Verilog-A code, available to CAD vendors.
 - ✓ Implementations ongoing in ELDO (Mentor) and Smash (Dolphin).
 - ✓ ADS/GoldenGate (Agilent), Spectre (Cadence) in discussion.
- ❖ Relation to advanced analog/RF IC design.
 - ✓ Characterization methods based on design needs.
 - ✓ Small-signal characterization method vs. IC & L.
 - ✓ Pinch-off voltage method.
 - ✓ Simple model structure & parameter extraction.
 - ✓ Example validations on 110nm, 90nm CMOS.
 - ✓ Extensions in EKV3.1: emphasis on RF, noise, and advanced technology scaling aspects.

Acknowledgments

- ❖ All EKV Team, esp.
 - ✓ Wladek Grabinski, for Web-site and Verilog-A support
 - ✓ Jean-Michel Sallese, Ananda Roy, ChristianENZ, for R&D contributions

- ❖ Contact: **Prof. Matthias Bucher**
Electronics Laboratory
ECE Dept.
Technical University of Crete
Polytechniupolis
73100 Chania, Crete, Greece
phone: +30 28210 37210
fax: +30 28210 37542
bucher@electronics.tuc.gr
<http://www.electronics.tuc.gr>

